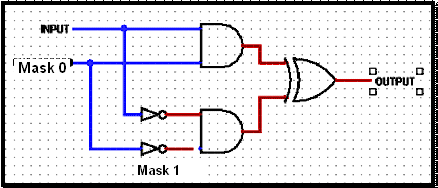
**TASK # 1:**

Implement following circuit into MIPS Assembly Language using AND,OR& XOR instructions.****

SOURCE CODE:

.data

input: .asciiz "\n Enter Value: "

Result: .asciiz "\n Result is: "

.text

.globl main

main:

li $t0,0x00000000

li $t1,0xffffffff

la $a0,input

li $v0,4

syscall

li $v0,5

syscall

move $t2,$v0

and $t3,$t2,$t0

not $t4,$t2

not $t5,$t0

and $t6,$t4,$t5

xor $t7,$t3,$t6

la $a0,Result

li $v0,4

syscall

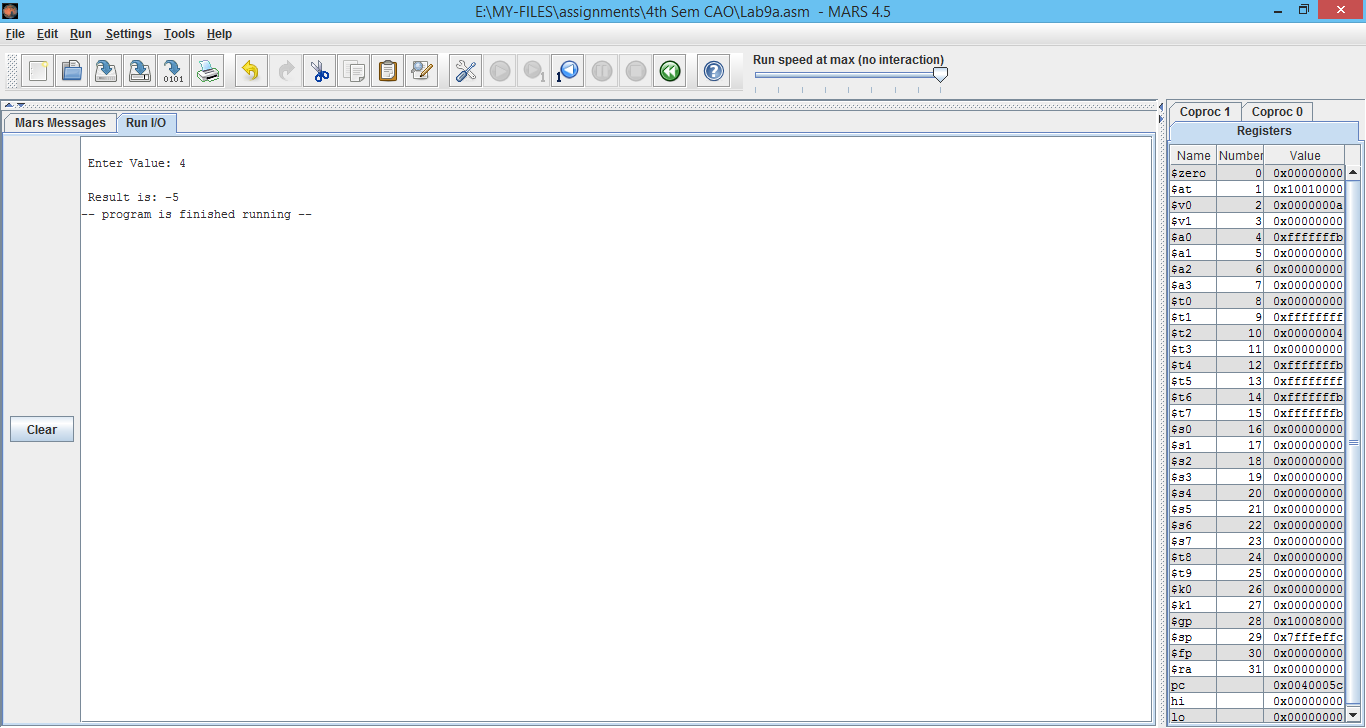
move $a0,$t7

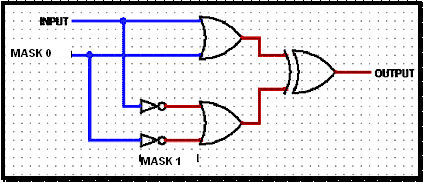
li $v0,1

syscall

li $v0,10

syscall

OUTPUT:

**TASK # 2:**

SOURCE CODE:

.data

input: .asciiz "\n Enter Value: "

Result: .asciiz "\n Result is: "

.text

.globl main

main:

li $t0,0x00000000

li $t1,0xffffffff

la $a0,input

li $v0,4

syscall

li $v0,5

syscall

move $t2,$v0

or $t3,$t2,$t0

not $t4,$t2

not $t5,$t0

or $t6,$t4,$t5

xor $t7,$t3,$t6

la $a0,Result

li $v0,4

syscall

move $a0,$t7

li $v0,1

syscall

li $v0,10

syscall

OUTPUT:

