Evaluation of High-Speed Universal Shift Register with 4-bit ALU

Group # 2***

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***Abstract*— This paper contains information about the universal shift register. In the early stages of this paper, this paper introduces different types of flip flops and calculates the delay. After that, different types of flip flops are used to make a universal shift register and measured the high-speed universal shift register by using a timing diagram. In addition, a complete memory system was designed at the end of this paper. To complete the memory system, a universal shift register was added with 4-bit Alu and as a result, a memory storage device has been created by this following method which is facile, more accurate, and, high speed in its own characteristics.**

***Index Terms*—Universal Shift Register, 4-bit ALU, Full adder, 4*1 Multiplexer, TGMS D flip-flop.**

I. Introduction

Flip flops can store or hold a single bit of binary data (0 or 1). However, several flip flops are required to store several bits of data. The register is a device that stores such information. A flip flop array is a set of flip flops used to hold multiple bits of data. The data contained in these registers can be transferred or shifted via shift registers. By using clock pulses, the bits contained in such registers can be made to shift within the registers and in/out of the registers. A high-speed shift register can shift data in low latency so it is very beneficial and desired.

It is able to attain extremely little latency in data processing by using an emerging notion of high speed in VLSI architecture. As a result, high-speed design can increase the performance of all of the preceding design stages. A system can have two types of timing errors: hold time violations and setup time violations. When an input signal changes too soon just after the clock's active transition, a hold time violation occurs. In a setup time infraction, the signal arrives too late and misses the time because it should advance. The arrival time of the signal can vary related to variation in input data, circuit activities, temperature and voltage variations, and so on.

For high-speed shift registers, high-speed flip flops are required. Therefore, various types of flip flops have been tested in this project, high-speed flip flops have been explored and comparisons have been made between all of them. The lower the data shift delay of the universal shift register, the higher the speed. ALU has also been designed and added to the universal shift register to complete the system and observe different ALU microoperations wthe ith data shifting process.

II. Literature Review

A. Rajaram, P. Premalatha, R. Sowmiya has designed a system of high-speed shift register using single clock pulse method. This study proposes a new shift register design based on a single clock pulse with Hold Mode (HM-FF) and without Hold Mode (WHM-FF) Flip Flop. This approach is designed for the Xilinx Virtex 6 family and delivers a reasonable speed boost. When compared to the present method, it gives a 41.9 percent reduction in latency and their future work is related with Future work is related to power optimization and area overhead of the implementation using this design [1]. Irudaya Praveen, Ravi, Kannan has invented 2GHz High Performance Double Edge Triggered D-Flip Flop Based Shift Registers In 32NM CMOS Technology. Data is stored on both the rising and falling edges of a clock signal in Double Edge Triggered Flip Flops. Although system specifications control the clock frequency, using DET flip-flops can reduce the clock frequency to half of its original value while maintaining the same data throughput. As a result, DET flip-flops consume less power, making them ideal for low-power applications. The performance of the DETFF-based shift registers is evaluated by analyzing the average power, latency, and PDP at various clock frequencies [2].

III. BASIC IDEA OF PROJECT

This is the figure of a universal shift register, where S0 and S1 are the selected pins that are used to select the mode of operation or shift right operation, or parallel mode. Pin-D of the first 4×1 Mux is fed to the output pin of the first flip-flop. Pin-C of the first 4X1 MUX is connected to serial input for shift right. In this mode, the register shifts the data towards the right. Similarly, pin-B of 4X1 MUX is connected to the serial input for shift-left. In this mode, the universal shift register shifts the data towards the left. M1 is the parallel input data given to the pin-3 of the first 4×1 MUX to provide parallel mode operation and store the data in the register. Similarly, remaining individual parallel input data bits are given to the pin-3 of related 4X1MUX to provide parallel loading. F1, F2, F3, and F4 are the parallel outputs of Flip-flops, which are associated with the 4×1 MUX [3].

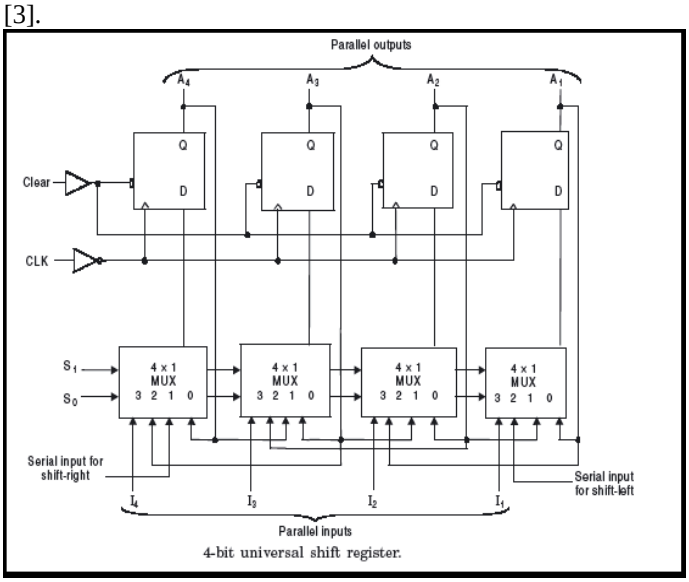

Fig. 1. Universal Shift Register

Here 4-bit ALU is connected with the universal shift register so that the system looks like the memory system as a result, it can do 8 micro-operation and can store data with the help of the universal shift register which is the main theme of this project.

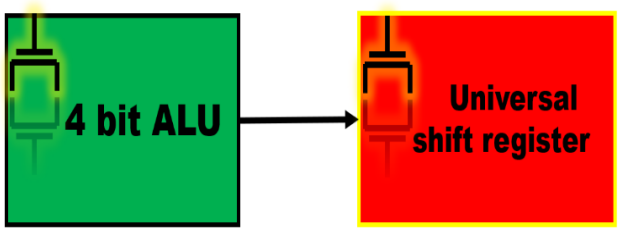

Fig. 2. Schematic of 4-bit ALU with Universal Shift Register

IV. SOFTWARE IMPLEMENTATION FOR HIGH-SPEED UNIVERSAL SHIFT REGISTER

A Universal shift register is bidirectional. That is, it is a register having both right and left shift capabilities, as well as parallel load capability. As a result, all shift register operations are possible in a single circuit. For designing the universal shift register, there are flip-flops, and a 4*1 multiplexer is required. A multiplexer is a combinational logic circuit that generates the output from only one input at a time. The select input lines decide which signals govern which input will be reproduced at the output end. Four-to-one (4:1) MUX is used when there are four inputs and only one is selected to link with the output. Multiplexer controls the operation of the universal shift register according to the below truth table:

Table 1: Truth table for 4*1 multiplexer

S1	S0	Operations
0	0	No Change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

Here, S1 and S0 is the control pin of the multiplexer. When both become 0,0 then the path 0 (D) is connected to the output. As well, for 0,1 a path 1 (C) is connected to the output, for 1,0 a path 2(B) is connected to the output, and for 1,1 a path 3(A) is connected t the output. According to the circuit in no change operation, the data rotates in a certain cycle and will continue to show the same initial value. In the Shift right operation, the data will continue to shift from left to right one by one for the per clock pulse. In shift left operation, the data will continue to shift from right to left one by one for the per clock pulse. In parallel load operation, all bit data will be loaded at the same time and provide output by a single clock pulse. Now, it is time to see how flip-flop works. Flip-flop works according to the below truth table:

Table 2: Truth table for Flip-Flop

Clk	D	Qn
0	x	Qn
1	0	0
1	1	1

From the truth table, it can be seen that when data is provided according to the data, the output is stored. Now, different types of flip-flops will be discussed to evaluate the high speed:

A. D Flip-Flop based Universal Shift Register

The D flip-flop is an edge-triggered device that transfers input data to Q when the clock's edge rises or falls. The D flip-flop is timed or clocked flip-flop with a single digital input denoted by the letter 'D.' When a D flip-flop is timed or clocked, its output corresponds to the state of 'D.' D and Clk are the only inputs on the D Flip Flop. The D inputs are routed to the S input accurately, and its complement is routed to the R input. The destination is obtained by the D flip flop from its ability to manage data in its internal store.

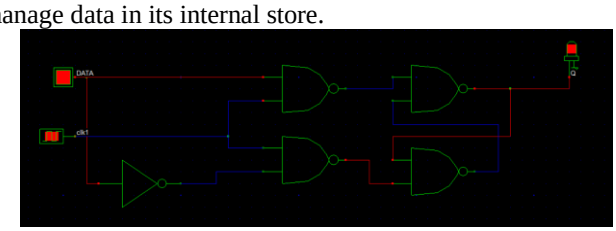

Fig. 3. D Flip Flop

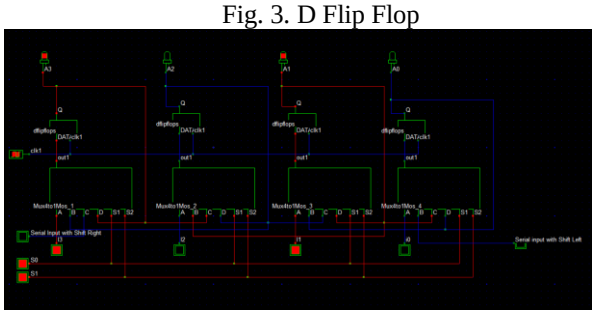

Fig. 4. D flip flop based Universal Shift Register

According to the universal shift register circuit, the D flip flop-based shift register is designed. The parallel loading and output are shown in figure 4.

B. Dynamic TGMS based Universal Shift Register

TGMS stands for transmission-gate-based master-slave. In this work, the dynamic TGMS or D-TGMS flip-flop is evaluated to attain high speed, however, it is susceptible to clock overlap. Transmission gates and MOS transistors are used to build the D-TGMS flip-flop. It has a lower delay than other flip-flop topologies. Furthermore, the energy per transition and clock energy of D-TGMS are also lower than those of NAND, mC2MOS, and C2MOS. This flip-flop fails if the clocks overlap for an extended amount of time. The detailed operation of D-TGMS is shown in figures 5 & 6.[4]

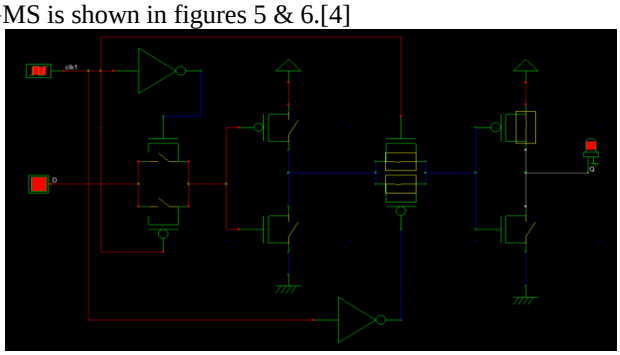

Fig. 5. Dynamic TGMS Flip Flop

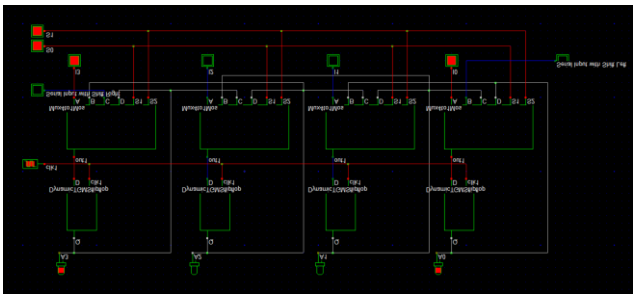

Fig. 6. Dynamic TGMS based universal shift register

According to the universal shift register circuit, the TGMS-based shift register is designed. The parallel loading and output are shown in figure 6.

C. MTSPC double-edge triggered flip flop based Shift Register

MTSPC stands for modified true single-phase clocked. True Single-Phase Clock (TSPC) is a high-speed universal dynamic flip-flop. To halt toggling of the intermediate nodes, the MTSPC D flip-flop requires one more PMOS than TSPC. It is commonly used in digital design. According to the proposed MTSPC DFF architecture, whenever the path to the ground is ON, pre-charging node B should be halted to avoid toggling. A simple solution that works, in this case, is to add a PMOS transistor that stops the pre-charging phase from occurring without compromising the flip-overall flop's functionality. The proposed MTSPC DFF not only consumes less power but also has a greater maximum frequency of oscillation for high performance. [5]

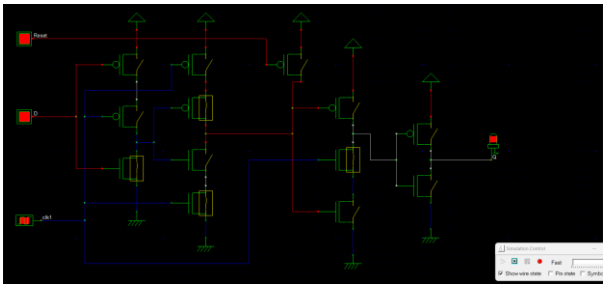

Fig. 7. MTSPC double-edge triggered flip flop

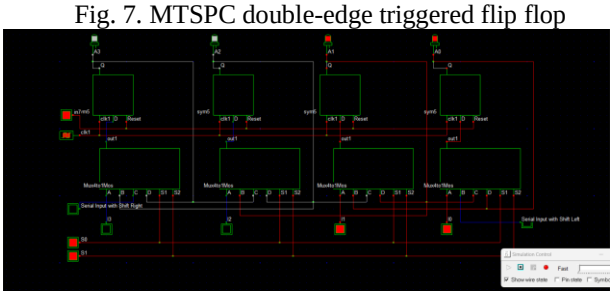

Fig. 8. MTSPC based Universal Shift Register

According to the universal shift register circuit, the MTSPC flip flop-based shift register is designed. The parallel loading and output are shown in figure 8.

D. TGMS D Flip-Flop based Universal Shift Register

TGMS stands for transmission-gate-based master-slave but it is not dynamic. Figure 9 depicts a Transmission Gate Based Master-Slave D Flip Flop. The TGs T1 and T2 serve as latches in the master and slave sections, respectively, while an inverter generates inverted and non-inverted clock signals CLK and CLKB locally. As indicated in Figure 1, feedback is delivered from the output node to a specific internal node in the master stage to make the flip-flop static in nature. This feedback is used with the knowledge that the forward path has exactly two inversions. In comparison to traditional static designs, the feedback approach used in the design is completely different. This design decreases the number of transistors and TGs in the critical path, resulting in maximum performance and symmetrical delays. [6]

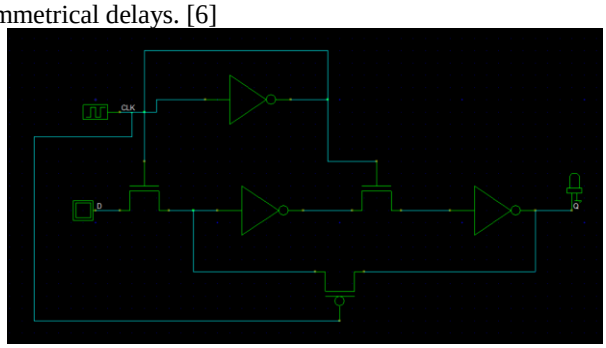

Fig. 9. TGMS D Flipflop

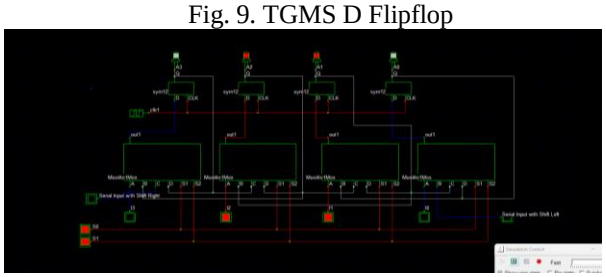

Fig. 10. TGMS D flipflop based Universal Shift register

V. Software Implementation for Universal Shift Register with 4-bit ALU

An arithmetic-logic unit is a portion of a central processing unit that performs arithmetic operations and logic operations on the operands of computer instruction words. The ALU has direct input and output access to the processor controller, main memory (RAM in a personal computer), and input/output devices. [4] So, in this portion of the project, an attempt has been made to design a complete system. That means, by this design, it will be able to do some microoperations in the ALU and then able to see how the data shifted. In 4-bit ALU there are four full adders and four 4*1 multiplexers used. Inverters are used in side B to invert the value for subtraction operation. Full Adder is an adder that takes three inputs and outputs two results.

Select			In	Output	
S_1	S_0	C_{in}	Y	$D = A + Y + C_{in}$	Microoperation
0	0	0	B	$D = A + B$	Add
0	0	1	B	$D = A + B + 1$	Add w/carry
0	1	0	B	$D = A + \overline{B}$	Subtract w/borrow
0	1	1	B	$D = A + \overline{B} + 1$	Subtract
1	0	0	0	$D = A$	Transfer A
1	0	1	0	$D = A + 1$	Increment A
1	1	0	1	$D = A - 1$	Decrement A
1	1	1	1	$D = A$	Transfer A

Fig. 10. 8 operations of ALU

The first two inputs are A and B, and the third is an input designated as Carry-in. The output carry is denoted as C-OUT, and the normal output is denoted as S or Sum. There are 8 micro-operations that can be possible with this ALU. The operations can be controlled by the control pin of the multiplexer. The micro-operations are:

The whole system design is shown below:

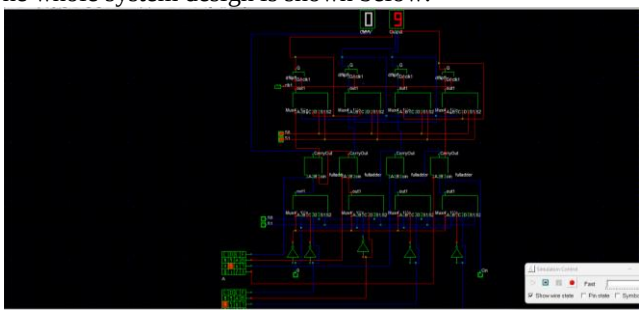

Fig. 12. 4-bit Universal Shift Register with ALU (addition)

VI. RESULTS AND DISCUSSION

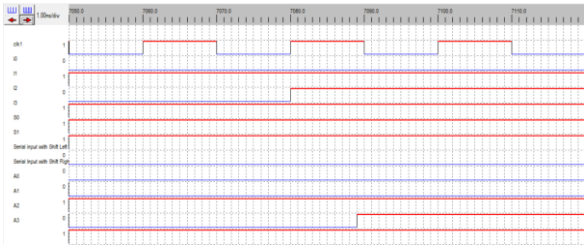

Fig. 13. Time Diagram of D flip flop based universal shift register

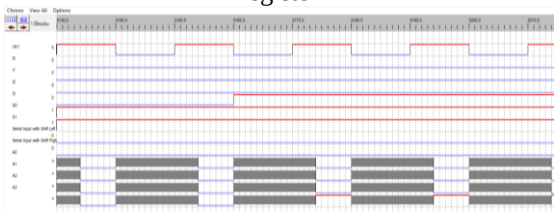

Fig. 14. Dynamic TGMS shift Register Time Diagram

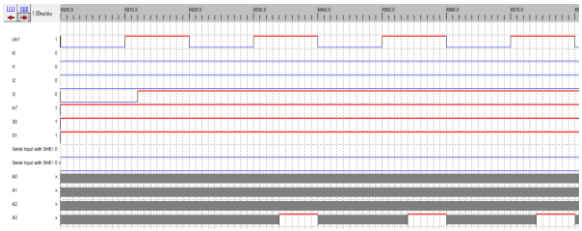

Fig. 15. MTSPC based Universal Shift Register Time Diagram

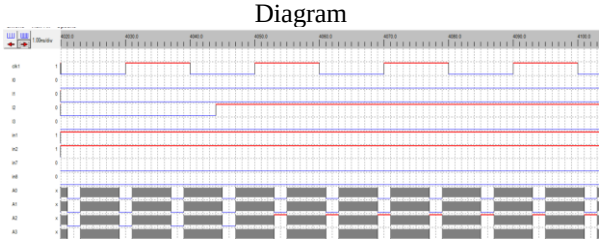

Fig. 16. TGMS D flip flop-based timing diagram

The time diagrams are shown here for all universal shift registers. The per division is for 1ns. From those, it can be possible to define the delay based on the input and output response.

Table 3: Delay Comparison for Different Flip Flop

Universal Shift registers	Speed (Delay=output time-input time)
D flip flop based	9ns
Dynamic TGMS	14 ns
MTSPC double-edge triggered	22 ns
TGMS	9 ns

From the table and figure, it can be seen that the D flip flop and TGMS flipflop-based shift register have less delay compared to the other flipflop. Though the difference is not so much like dynamic TGMS flip flop is very closer to TGMS and D flip flop. MTSPC has other some advantages but it has a higher delay than others.

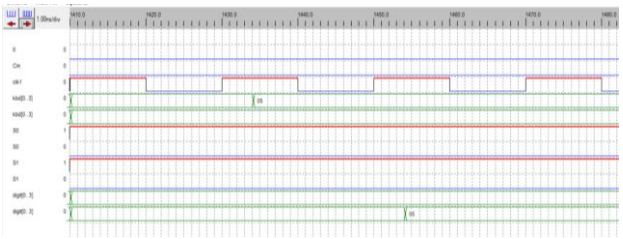

Fig. 17. Time Diagram for ALU (input)

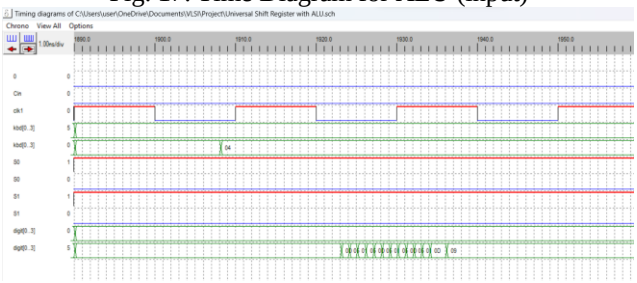

Fig. 18. Time diagram for ALU (for input & output)

After adding ALU with the D flip flop-based universal shift register, it can be seen that the delay is increased little a bit. But it is stills not so much. ALU was added to the TGMS flip flop-based universal shift register but the delay became double in this perspective. So, overall D flip flop is a better choice but TGMS is also faster.

VII. FUTURE WORK

Though few types of flip flops have been compared throughout the project still there are many scopes available for increasing the speed of flip flops. If there is a chance to implement artificial intelligence with this memory system, it will become more facile, faster, and better in nature. After that, we can invent a system, which Will have less consumption of power but speed will be the same. As a result, it will become helpful for the country's economy. In the future, we can

implement fewer area-based flip flops like TGMS in the memory device so that speed becomes high and the area becomes less.

VIII. CONCLUSION

This paper was all about designing a memory system like a universal shift register was added with 4-bit ALU. As a result, a memory device has been created which can store data easily. After that, to make universal shift registers faster different types of flip flops were compared, and got our desired result. In summary, d flip flop and TGMS has less delay compared with other flip flops. Less delay means faster. So, we successfully created this project.

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