# RZ/A: Use of serial flash with double data rate (DDR) transfer

Last Updated:08/05/2020

Question:

Use of serial flash with double data rate (DDR) transfer

Answer:

It describes each RZ/A series group.

When using the serial flash memory as DDR transfer with the RZ/A series, we recommend Macronix serial flash memory.

Please contact Macronix for recommended devices if necessary. Since the electrical characteristics depend on the terminal capacity of the serial flash memory, the wiring length on the board, the layout, etc., please consider the following values as a guide.

(Power supply voltage: 3.0 to 3.6V, Operating temperature : -40 to +85)

RZ/A2M group

When using the clock(QSPI0_SPCLK) frequency of 66MHz, it is possible to connect a serial flash memory that satisfies the following timings.

Clock Low to Output Valid (tCLQV/tV) : Max 5ns

Output Hold Time (tCLQX/tHO) : Min 1ns

Data In Setup Time (tDVCH/tSU) : Min 2ns

Data In Hold Time (tCHDX/tHD) : Min 1ns

RZ/A1L, RZ/A1LU, RZ/A1LC group

RZ/A1L and RZ/A1LC do not support DDR transfer.

Regarding the RZ/A1LU, when using the clock(SPBCLK) frequency of 66.66MHz, it is possible to connect a serial flash memory that satisfies the following timings.

Clock Low to Output Valid (tCLQV/tV) : Max 5ns

Output Hold Time (tCLQX/tHO) : Min 1ns

Data In Setup Time (tDVCH/tSU) : Min 2ns

Data In Hold Time (tCHDX/tHD) : Min 1ns

RZ/A1H, RZ/A1M group

When using the clock(SPBCLK) frequency of 50MHz, it is possible to connect a serial flash memory that satisfies the following timings. It is impossible for RZ/A1H and RZ/A1M that the clock(SPBCLK) frequency is over 50MHz.

When setting the SPBCLK frequency to 50MHz, it is necessary to input 10MHz from EXTAL, and the maximum CPU frequency is 300MHz.

Clock Low to Output Valid (tCLQV/tV) : Max 5ns

Output Hold Time (tCLQX/tHO) : Min 0ns

Data In Setup Time (tDVCH/tSU) : Min 2ns

Data In Hold Time (tCHDX/tHD) : Min 1ns

Suitable Products

RZ/A1LU

RZ/A1M

RZ/A1H

RZ/A2M

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