**Abstract:**

This project is about designing a 7*5 two's complement multiplier using the modified Baugh-Wooley approach. We used the static CMOS approach at the logic level and SCN3M technology at the IC layout.

At Logic design Phase, We used Logisim to simulate our design and verify its proper operation including proper number of test vectors.

At Layout Phase, We used the given CUSCLIB cells to build new cells such as Full adder, Half adder, AND, etc. Then we used these cells to build the layout of the multiplier with/without PADs. After checking the design rules, We simulate our layout to verify its proper operation including the same test vectors used in the logic design phase. Then we calculated the Max. frequency hence found out the dynamic power at this frequency.