7 Register mapping

The table given below provides a listing of the 8-bit registers embedded in the device and their respective addresses.

Table 17. Register address map

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
Reserved	*Table 16*	--	00-0E	--	--
WHO_AM_I_G	*Table 16*	r	0F	000 1111	11010100
Reserved	*Table 16*	--	10-1F	--	--
CTRL_REG1_G	*Table 16*	rw	20	010 0000	00000111
CTRL_REG2_G	*Table 16*	rw	21	010 0001	00000000
CTRL_REG3_G	*Table 16*	rw	22	010 0010	00000000
CTRL_REG4_G	*Table 16*	rw	23	010 0011	00000000
CTRL_REG5_G	*Table 16*	rw	24	010 0100	00000000
REFERENCE_G	*Table 16*	rw	25	010 0101	00000000
Reserved	*Table 16*	--	26	--	--
STATUS_REG_G	*Table 16*	r	27	010 0111	output
OUT_X_L_G	*Table 16*	r	28	010 1000	output
OUT_X_H_G	*Table 16*	r	29	010 1001	output
OUT_Y_L_G	*Table 16*	r	2A	010 1010	output
OUT_Y_H_G	*Table 16*	r	2B	010 1011	output
OUT_Z_L_G	*Table 16*	r	2C	010 1100	output
OUT_Z_H_G	*Table 16*	r	2D	010 1101	output
FIFO_CTRL_REG_G	*Table 16*	rw	2E	010 1110	00000000
FIFO_SRC_REG_G	*Table 16*	r	2F	010 1111	output
INT1_CFG_G	*Table 16*	rw	30	011 0000	00000000
INT1_SRC_G	*Table 16*	r	31	011 0001	output
INT1_TSH_XH_G	*Table 16*	rw	32	011 0010	00000000
INT1_TSH_XL_G	*Table 16*	rw	33	011 0011	00000000
INT1_TSH_YH_G	*Table 16*	rw	34	011 0100	00000000
INT1_TSH_YL_G	*Table 16*	rw	35	011 0101	00000000
INT1_TSH_ZH_G	*Table 16*	rw	36	011 0110	00000000
INT1_TSH_ZL_G	*Table 16*	rw	37	011 0111	00000000
INT1_DURATION_G	*Table 16*	rw	38	011 1000	00000000
Reserved	*Table 15*	--	00-04	--	--

Table 17. Register address map (continued)

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
OUT_TEMP_L_XM	Table 15	r	05	000 0101	output
OUT_TEMP_H_XM	Table 15	r	06	000 0110	output
STATUS_REG_M	Table 15	r	07	000 0111	output
OUT_X_L_M	Table 15	r	08	000 1000	output
OUT_X_H_M	Table 15	r	09	000 1001	output
OUT_Y_L_M	Table 15	r	0A	000 1010	output
OUT_Y_H_M	Table 15	r	0B	000 1011	output
OUT_Z_L_M	Table 15	r	0C	000 1100	output
OUT_Z_H_M	Table 15	r	0D	000 1101	output
Reserved	Table 15	--	0E	000 1110	--
WHO_AM_I_XM	Table 15	r	0F	000 1111	01001001
Reserved	Table 15	--	10-11	--	--
INT_CTRL_REG_M	Table 15	rw	12	001 0010	11101000
INT_SRC_REG_M	Table 15	r	13	001 0011	output
INT_THS_L_M	Table 15	rw	14	001 0100	00000000
INT_THS_H_M	Table 15	rw	15	001 0101	00000000
OFFSET_X_L_M	Table 15	rw	16	001 0110	00000000
OFFSET_X_H_M	Table 15	rw	17	001 0111	00000000
OFFSET_Y_L_M	Table 15	rw	18	001 01000	00000000
OFFSET_Y_H_M	Table 15	rw	19	001 01001	00000000
OFFSET_Z_L_M	Table 15	rw	1A	001 01010	00000000
OFFSET_Z_H_M	Table 15	rw	1B	001 01011	00000000
REFERENCE_X	Table 15	rw	1C	001 01100	00000000
REFERENCE_Y	Table 15	rw	1D	001 01101	00000000
REFERENCE_Z	Table 15	rw	1E	001 01110	00000000
CTRL_REG0_XM	Table 15	rw	1F	001 1111	00000000
CTRL_REG1_XM	Table 15	rw	20	010 0000	00000111
CTRL_REG2_XM	Table 15	rw	21	010 0001	00000000
CTRL_REG3_XM	Table 15	rw	22	010 0010	00000000
CTRL_REG4_XM	Table 15	rw	23	010 0011	00000000
CTRL_REG5_XM	Table 15	rw	24	010 0100	00011000
CTRL_REG6_XM	Table 15	rw	25	010 0101	00100000
CTRL_REG7_XM	Table 15	rw	26	010 0110	00000001