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BACHELOR THESIS

Building a "Router on a chip" using Freescale's t1040 platform

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Bucharest, 2014

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Chapter 1

Introduction

This is just a demo file. It should not be used as a sample for a thesis.

TODO:
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1.1 Project Description

1.2 Background

This thesis presents the **MySuperProject**.

1.3 The Problem

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1.4 The Solution

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Introduction: -length= ??(probabil pana in 4 pagini)

* Background: - state of the art - utilitatea routerelor de genul - context / routere / ce exista pe piata - cam 1 pagina?

* The problem - ce probleme au solutiile existente - 0.5 - 1 pagini?

* The solution - ce fac eu - ce am in plus, de ce e mai bun - foarte sumar - cam 1 pagina

Main body: -length= ? (20-30 pagini)

* The Freescale Platform - hw specs - detalii generale arhitectura - ce face bine, de ce e bun pentru un astfel de proiect - 4 pagini?

* Characteristics - ce functionalitati are - prezentat in subcapitole separate fiecare parte (TODO) - poate intra mult, deci poate chiar 10

* Architecture: - scheme - altceva???

* Scenarii de folosire: - small office router - lightweight hosting - TODO: mai gaseste chestii de bagat

* Performante: - maybe?

Chapter 2

The t1040 platform

This chapter offers details on the hardware used in this "Router on a chip". The first section offers hardware specifications necessary when comparing this platform to other commercial routers, the second section offers general details on the specific architecture used when building the platform, and the last section evaluates the strengths and weakneses of the hardware in order to asses better the final performance of this application

2.1 HW specs

The t1040 platform hosts a quad core processor and targets the low-end sector through it's price accesibility and low power consumption. The e5500 cores are based on the Power architecture, have a maximum frequency of 1.4Ghz and host a 256KB L2 cache each.

An important feature for this aplication is the presence of the 3 levels of instructions: user, supervisor and hypervisor. This allows the processor to cooperate with a hypervisor, enabling hardware virtualisation and extending the application scenarios that can be run.

The RAM memory is DDR3 and the platform support a maximum throughput of 1600MT/s. DMA is dual four channel

TODO:
reread the above paraghraph

On the connectivity side, included are 2 Serial ATA(SATA 2.0) controllers, enhanced secure digital host controllers (SD/MMC/eMMC), 2 USB2.0 ports with integrated PHYs, 4 PCI-express ports, controllers for NAND and NOR flash memory and 4 UART ports.

TODO:
Poate e mai bine ca lista??

The networking connectivity includes 5 Gbps Ethernet MAC ports (with support for SGMII and QSGMII interfaces) and a hardware Gigabit Ethernet switch with 8 ports.

2.2 General arch details

Being a Communications Processor T1040 offers facilities for speeding up packet analysis, clasification and distribution, by offloading them in hardware

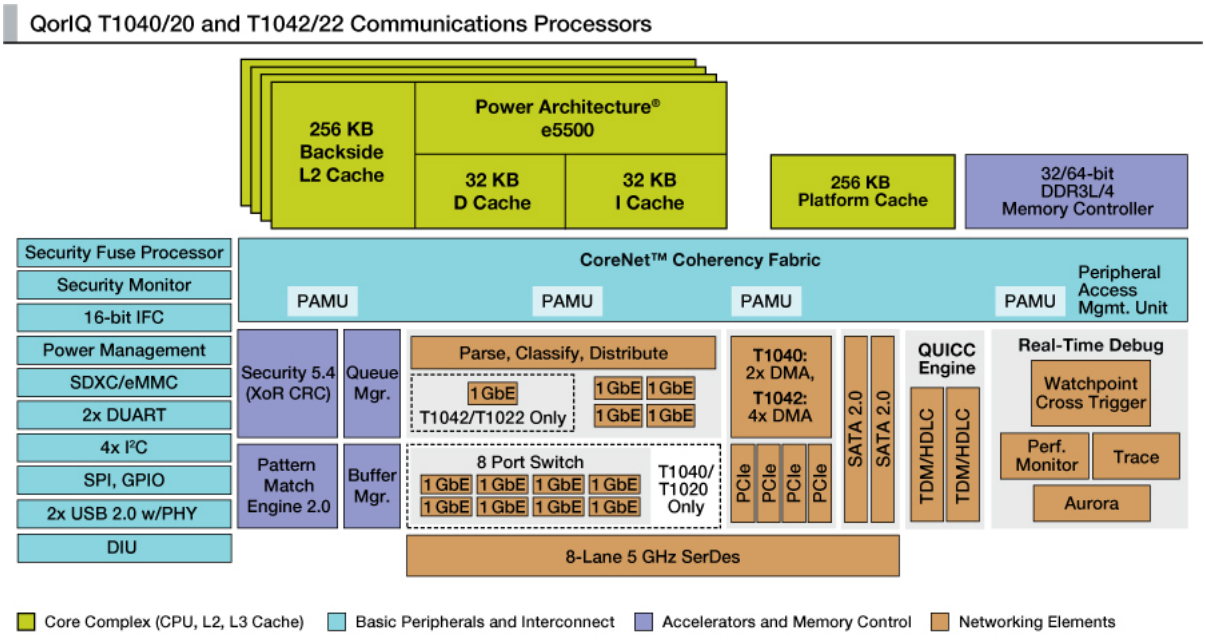

Figure 2.1: T1040 diagram

We can also have citations like [1].

2.3 Why is it good for what we need

Chapter 3

Features

This is just a demo file. It should not be used as a sample for a thesis.

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3.1 LAN switching

3.2 Wireless network

3.3 Wireless/LAN bridging

3.4 HW firewall

3.5 Easy administration / Webmin

3.6 HW/SW routing

3.7 NAT

3.8 SW services

Chapter 4

Architecture

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4.1 ?????

Chapter 5

Usecases

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5.1 Use 1

5.2 Use 2

5.3 Use 3

5.4 Use 4

5.5 Use 5

Bibliography

[1] International Organization for Standardization. Iso/iec 26300:2006 open document format. http://std.dkuug.dk/keld/iso26300-odf/is26300/iso_iec_26300:2006_e.pdf, December 2006.