

# Rajshahi University of Engineering & Technology

Course No: CSE 2204

Course Title: Sessional based on CSE 2203

Submitted To:

<p>Md. Zahirul Islam Lecturer Department of Computer Science and Engineering Rajshahi University of Engineering and Technology</p>	<p>Prof. Dr. Boshir Ahmed Professor Department of Computer Science and Engineering Rajshahi University of Engineering and Technology</p>
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Submitted By:

Name: Mondol Mridul Provakar

Roll: 1803062

Section: B

Department of Computer Science and Engineering,  
Rajshahi University of Engineering and Technology.

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## Experiment No.: 5.1

### 5.1.1: Name of the experiment:

Verify the Half Adder Circuit.

### 5.1.2: Objectives:

- To understand how to use the logisim software, test logic design and debug it.
- To study & implement Half Adder Circuit.
- Simplifying logic circuit functions
- Understand how to implement simple circuits based on a schematic diagram using logic gates.

### 5.1.3: Theory:

A half adder is used to add two single-digit binary numbers and results into a to-digit output. It is named as such because putting two half adders together with the use of an OR gate results in a full adder. In other words, it only does half the work of a full adder.

The adder works by combining the operations of basic logic gates, with the simplest form using only a XOR and an AND gate. This can also be converted into a circuit that only has AND, OR and NOT gates.

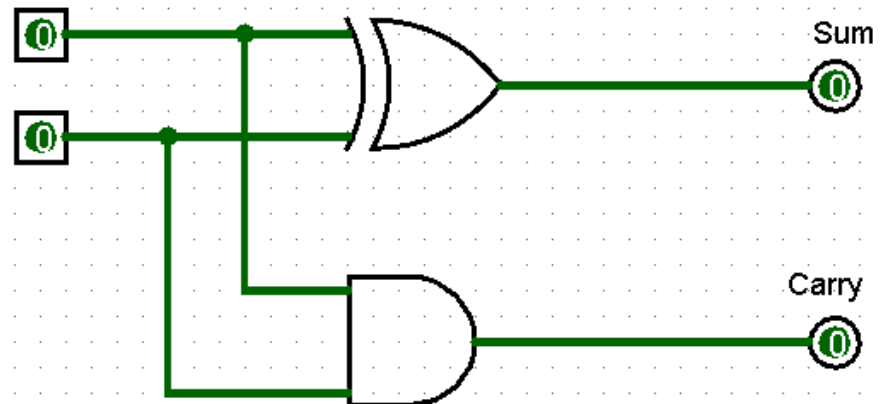
#### 5.1.4: Experimental Analysis:

(i) Truth Table:

x	y	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(ii) Circuit Diagram:

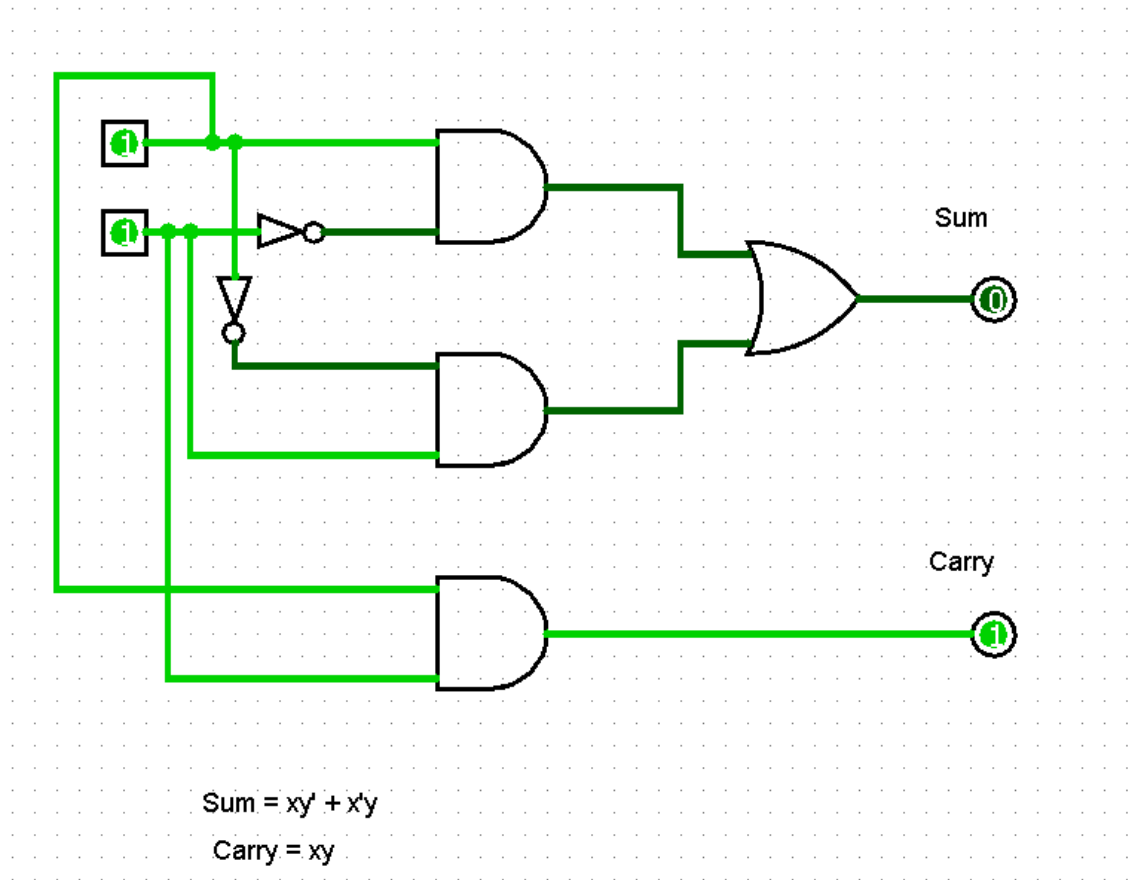
(1)



$$\text{Sum} = x \text{ XOR } y$$

$$\text{Carry} = xy$$

(2)



#### 5.1.5: Conclusion:

The basic logic gates are the building blocks of more complex logic circuits. Half adder is a combinational circuit that performs the addition of two bits. In this experiment, a half adder was implemented in two ways. One was through XOR and AND gate & the other was through only the basic logic gates.

Thus the experiment was done successfully.

## Experiment No.: 5.2

### 5.2.1: Name of the experiment:

Verify the Full Adder Circuit.

### 5.2.2: Objectives:

- To understand how to use the logisim software, test logic design and debug it.
- To study & implement Full Adder Circuit.
- Simplifying logic circuit functions
- Understand how to implement simple circuits based on a schematic diagram using logic gates.

### 5.2.3: Theory:

A full adder takes two binary numbers plus a carry or overflow bit. The output is a sum and another carry bit. Full adders are made from, XOR, AND and OR gates in hardware. Full adders are commonly connected to each other to add bits to an arbitrary length of bits, such as 32 or 64 bits. A full adder is effectively two half adders, an XOR and an AND gate, connected by an OR gate.

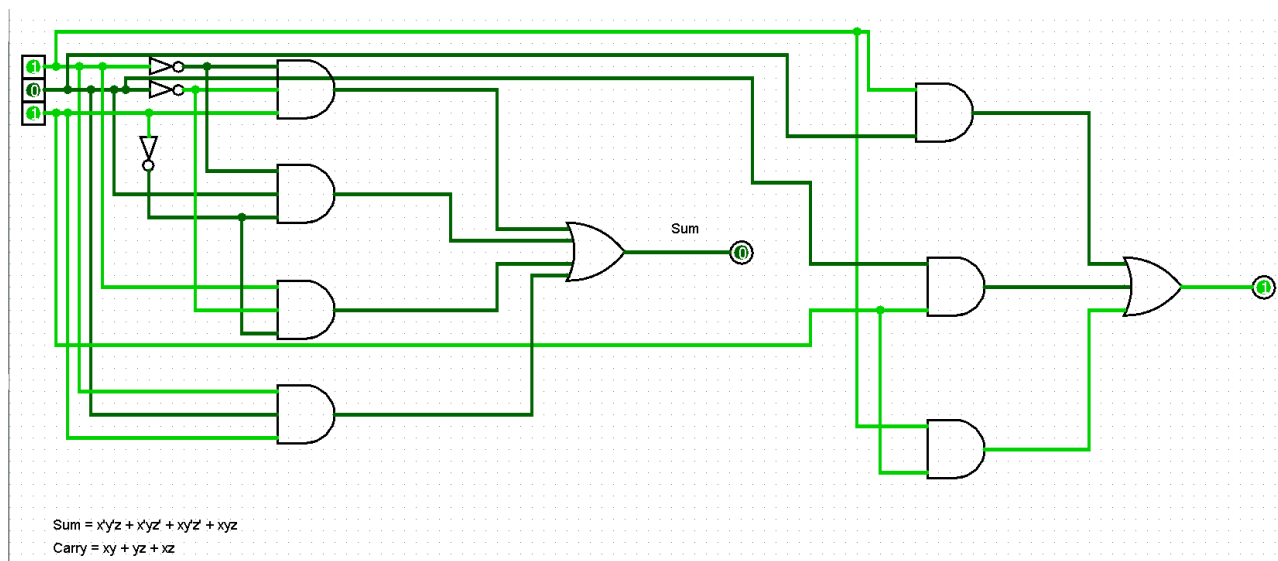
### 5.2.4: Experimental Analysis:

#### (i) Truth Table:

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0

0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(ii) Circuit Diagram:



5.2.5: Conclusion:

The basic logic gates are the building blocks of more complex logic circuits. Full adder is a combinational circuit that performs the addition of three bits. In this experiment, a full adder was implemented in SOP.

Thus the experiment was done successfully.

## Experiment No.: 5.3

### 5.3.1: Name of the experiment:

Implement the Full Adder Circuit by using Half Adder Circuit and verify the result.

### 5.3.2: Objectives:

- To understand how to use the logisim software, test logic design and debug it.
- To study & implement Full Adder Circuit using Half Adder.
- Simplifying logic circuit functions
- Understand how to implement simple circuits based on a schematic diagram using logic gates.

### 5.3.3: Theory:

A full adder takes two binary numbers plus a carry or overflow bit. The output is a sum and another carry bit. Full adders are made from, XOR, AND and OR gates in hardware. Full adders are commonly connected to each other to add bits to an arbitrary length of bits, such as 32 or 64 bits. A full adder is effectively two half adders, an XOR and an AND gate, connected by an OR gate.

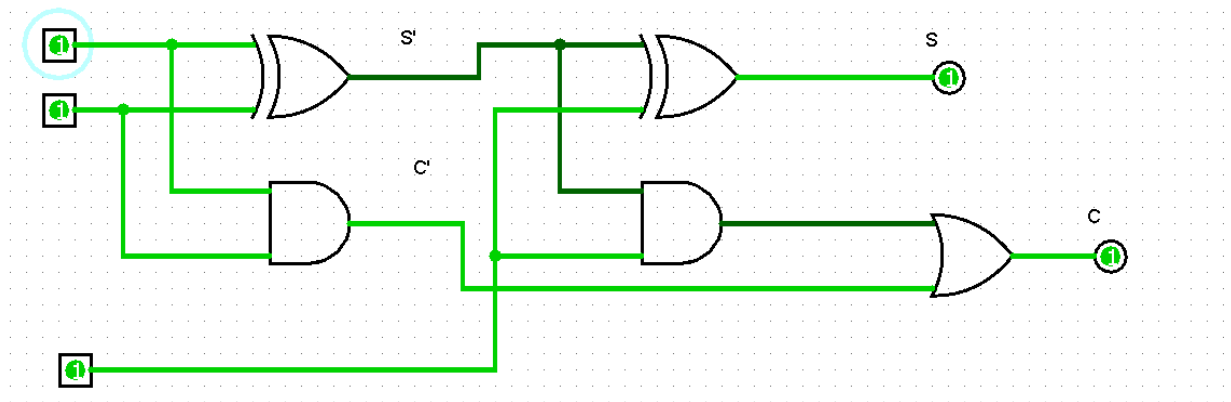
### 5.3.4: Experimental Analysis:

(i) Truth Table:

A	B	C	Sum	Carry
0	0	0	0	0

0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(ii) Circuit Diagram:



### 5.3.5: Conclusion:

The basic logic gates are the building blocks of more complex logic circuits. Full adder is a combinational circuit that performs the addition of three bits. In this experiment, a full adder was implemented through two Half Adder & an OR gate.

Thus the experiment was done successfully.