

Heaven's Light Is Our Guide
RAJSHAHI UNIVERSITY OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

3rd Year Even Examination 2021

COURSE NO: CSE 3203 COURSE TITLE: Computer Architecture and Design
FULL MARKS: 72 TIME: 3 HRS

- N.B. (i) Answer any SIX questions taking any THREE from each section.
(ii) Figures in the right margin indicate full marks.
(iii) Use separate answer script for each section.

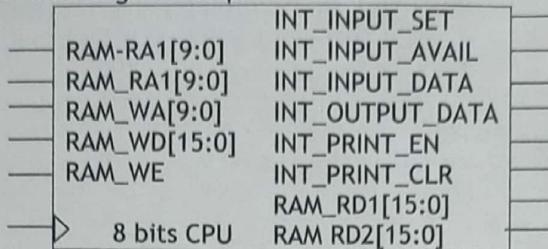
	<u>SECTION : A</u>	Marks	CO
Q.1.	(a) Explain importance of computer architecture for both software and hardware engineers. Explain the way where addition can be used to perform both addition and subtraction. (b) Show difference between SSD and HDD. Also show difference between main memory and secondary memory. (c) Discuss ZF, SF and OF FLAG in FLAG register. Design a parity flag (PF) detector for a 4-bit CPU.	4	CO1
Q.2.	(a) Show how Booth Multiplication Algorithm performs binary multiplication of $X = 11$ and $Y = 11$ step by step along with its equivalent top level circuit. (b) Built a RAM with following configurations: i) size = 3×2 ii) operation = 1 Write operation and 1 Read operation. (c) Design an operation circuit for ALU for a 4-bit CPU supporting TEST RA, POS instruction which checks whether RA register has value 1 in bit position specified by POS. If yes, then set carry FLAG (CF). If no, then do nothing.	4	CO2
Q.3.	(a) Explain the limitations of sign magnitude representation of any number. Show a 4-bit signed adder circuit and its output when $X=1010$ and $Y=1111$. (b) Write the reasons to use DRAM for main memory instead of SRAM. (c) Write the functions of a register in a CPU circuit. Design a 4-bit register circuit.	4	CO3
Q.4.	(a) Show binary subtraction of 2048.75 and 48.5 using IEEE-754 single precision format (b) Discover mapping between 1GB of Virtual Memory and 64MB of physical memory with a page size of 16KB with figure. (c) Discuss Arithmetic Operation performed by ALU. Design an ALU based on following configurations: i) Word size=2 bit ii) supported operations = RIGHT ROTATE (opcode = 111) and XOR(opcode = 010)	4	CO1
		4	CO2
		4	CO3

SECTION : B

Q.5.	(a) Discuss Performance Equation of a CPU. (b) Design a CPU based on following configurations: i) Word size = 16-bit ii) No of Registers = 32 Registers iii) Instruction = JZE LABEL iv) RAM size = 256 x 24 Also design ISA and Control Unit of CPU.	1	CO4
		6	CO4
	(c) Show difference between Pipelining and Scalar Pipelining. Show pipeline diagram for Pipelining and scalar Pipelining for following code snippet: START: MUL R3, R2 ADD R2, 1 CMP R4, R2 JMP START	5	CO5

Bypass strategy will be used in case of hazards.

Q.6. (a) Consider the following CPU chip:



7 CO4

i) Connect CPU chip with RAM chip, connect 8 switches to input port and 4 LEDs to output port of CPU.

ii) Write down assembly program so that AND operation can be performed between 1st half of 8 switches and 2nd half of 8 switches and 4 LEDs can be used to provide output.

(b) Consider the following code snippet:

5 CO5

```
ADD R1, 2  
XOR R2, R2  
CMP R1, R2  
JG LABEL
```

Find data hazard and control hazard and use pipelining diagram to show how hazard will be avoided if stall strategy is used.

Q.7. (a) Discuss based with Displacement Addressing Mode. 1 CO4

(b) Design a Based with Displacement Mode LOAD instruction where Displacement will always be multiplied by 4 for a 8-bit CPU having 32 registers along with its 20-bit ISA and Control Unit. 6 CO4

(c) Show a HDL program of 4bit register with asynchronous enable and synchronous reset along with a test bench. 5 CO5

Q.8. (a) Compare RISC and CISC processor. Give an example of each. 3 CO4

(b) Explain Interrupt. Write three devices or situations that would generate interrupt and explain in each case what would cause the interrupt to be generated. 4 CO4

(c) Show a 2 to 1 priority encoder circuit using case statement in verilog HDL and also write the test bench that can verify the circuit. 5 CO5

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COURSE NO: CSE 3207 COURSE TITLE: Peripherals and Interfacing
FULL MARKS: 72 TIME: 3 HRS

- N.B. (i) Answer any SIX questions taking any THREE from each section.
(ii) Figures in the right margin indicate full marks.
(iii) Use separate answer script for each section.

SECTION : A

Marks CO

- Q.1.** (a) Memory is nothing but a storage device for data, instructions and programs. Memory mainly two types: RAM and ROM. To interface with RAM & ROM we need RD and WR signals. There can be multiple RAM & ROM chips connected to the microprocessor. So, there should be a logic for selecting memory chips that the microprocessor wants to communicate for read or write operation to do the above job perfectly-
- i) Which type of device is needed?
 - ii) Explain the detail functionality of the device which you have mentioned in (i).
- (b) Let, assume that, you are an engineer of a renowned hardware chip manufacturing company. One day, your boss asks to design some memory chips to interface with 8086 microprocessor. The main concern is that you have to ensure that, the 8086 microprocessor can access 16 bits of data at one cycle. Now, as an engineer you have to design a logic circuit diagram to interface 32KB EPROM using 16KB chips and 128 KB RAM using 32 KB chips with 8086 microprocessor.
- i) The starting address of EPROM-1 is F8000H, what will be the ending address of EPROM-1?
 - ii) Using the following LS138 decoder, draw the complete circuit connection (use A₁₅, A₁₆ & A₁₇) pins as selection inputs.

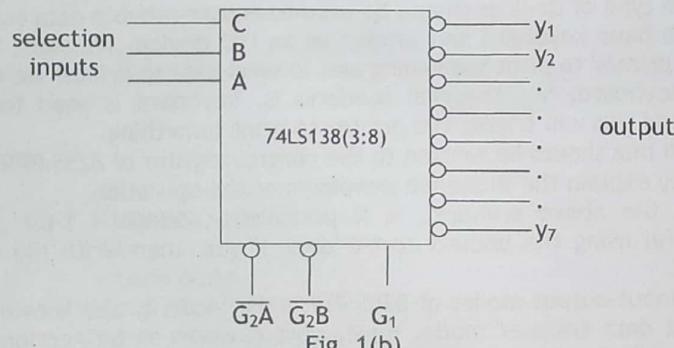


Fig. 1(b)

- iii) The starting address of RAM-1 is 00000H, what will be the ending address of RAM-1?
 - iv) Also mention the starting and ending address of all EPROM and RAM chips.
- (c) In program controlled I/O interfacing, IN and OUT instructions are used to transfer data between processor and I/O device. Now, using the concept of program controlled I/O interfacing, write appropriate instructions to perform the following operations:
- i) send data 1234H to port number 80H.
 - ii) send data 1234H to port number 8000H.

- Q.2.** (a) Interrupt means break the sequence of instruction execution. 8086 has only two interrupt inputs, NMI and INTR. If we save NMI for power failure interrupts, this leaves only one interrupt for all other applications. To handle interrupt from multiple devices, we use an IC called 8259 PIC. Now, consider the following scenario:

IRR

IR ₇	IR ₆	IR ₅	IR ₄	IR ₃	IR ₂	IR ₁	IR ₀
0	0	0	0	0	1	1	0

ISR

0	0	0	0	0	0	0	1
---	---	---	---	---	---	---	---

IMR

1	1	1	1	1	1	0	0
---	---	---	---	---	---	---	---

- i) IN normal end of interrupt mode, describe the interrupt request execution procedure in step by step.
- ii) IN automatic end of interrupt mode, what will be the current ISR? How the IR₁ and IR₂ requests are going to be executed?
- iii) Which operational command word should be sent to mask the higher priority lines (IR₀, IR₁, IR₂)?
- iv) From the following ISR, we can see that IR₀ is in service. Is it possible to request in IR₀ pin again, while it is in execution?
- (b) Suppose, you are working with a 8259A priority interrupt controller (PIC). You are already known that it has three unique registers: interrupt request register (IRR), in service register (ISR) and interrupt mask register (IMR). Now, you are given the following values of these three registers:

$$\text{IRR} = 11101000$$

$$\text{IMR} = 01010101$$

$$\text{ISR} = 00001000$$

4 CO3

- How will the 8259A PIC resolve these interrupts? Justify your answer.
- (c) For 8259A PIC, there are four initialization command words (ICW) and three operational command words (OCW). Suppose you are given the following values for the corresponding command words:

$$\text{ICW1} = 01010001$$

$$\text{ICW2} = 00001111$$

$$\text{ICW4} = 00010101$$

$$\text{OCW2} = 01110011$$

$$\text{OCW3} = 01001011$$

3 CO3

From the above mentioned values, mention the actions/approaches taken by the 8259 PIC.

- Q.3. (a) We can connect I/O devices with 8086 microprocessor through data bus. But it performs unreliable data transfer

3 CO2

- i) In which conditions, the direct data transfer between I/O and microprocessor are called unreliable?

- ii) Which signals ensure reliability in data transfer?

- iii) Which type of devices should be used to ensure reliable data transfer?

- (b) Suppose, we have keyboard and printer as an I/O device. We want to send data to the printer to print something and to send data to printer we need to press the keyboard. So, the real scenario is, keyboard is used for press something and this will trigger the printer to print something.

6 CO2

- i) Which bits should be written to the control register of 8255 PPI?

- ii) Briefly explain the sequence waveform of the operation.

- iii) Form the above scenario, is it possible to design a 1-bit counter (binary) using the unused port-C pins. If yes, then write the control word.

- (c) One of the input-output modes of 8255 PPI is the mode 2, also known as the bidirectional data transfer mode. Here, port A works as bidirectional port and port B works in either mode 0 or mode 1. Port A uses five signals of port C as the handshake signals. Remaining three lines can be used as simple I/O or handshake signals for port B. Now, consider the fig. 3(c) picture and from this figure, explain the working process of the bidirectional data transfer mode.

3 CO2

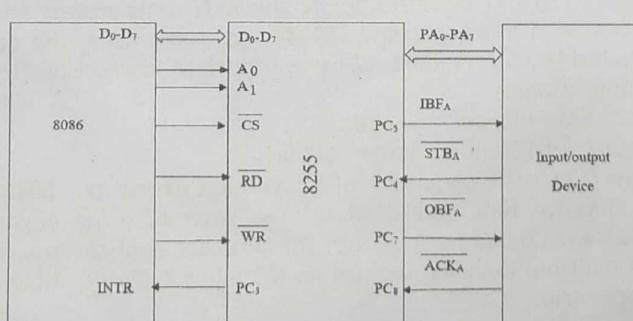


fig. 3(c)

- Q.4. (a) Microprocessor transfers data between memory & I/O using instructions. But, this procedure is time-consuming. To overcome this problem, 8086 microprocessor uses 8257 DMA controller. When the 8257 DMAC becomes the bus master, it can transfer data between memory and I/O without the

5 CO2

intervention of 8086 microprocessor. But, the main problem is that, 8257 DMAC has only eight address lines. This eight address lines can produce maximum 8-bits address. But, to perform data transfer between memory and I/O, 8257 DMAC needs to generate 16 bit logical address.

- i) Briefly explain the steps, how the 8257 DMAC becomes the bus master?
 - ii) How the 8257 DMAC generates 16-bits logical address using eight bits address lines?
- (b) The control word of 8251 defines the complete functional definition of 8251 block diagram in microprocessor and they must be loaded before any transmission or reception. The control words of block diagram of 8251 microcontroller are split in two formats: mode instruction and command instruction. Suppose, you are given the following values:

Mode Instruction = 10111010

Command Instruction = 11010101

Determine the significance of each bit in the mode instruction and command instruction.

- (c) Consider the following scenario:

- i) You are an administrator of a web server. Now, if you want to perform DMA operation, which data transfer mode of DMA operation, which data transfer mode of DMA you will choose and why?
- ii) Assume that, you are a hardware fabrication engineer at INTEL. While building processor for personal uses, which data transfer mode of DMA you will choose and why?

4 CO2

3 CO2

3 CO3

SECTION : B

Q.5.

- (a) Suppose, 8086 microprocessor executes 100 instructions. After completing 10 instructions it wants a delay of 10 seconds. After 10 seconds it resumes the execution for next 10 instructions and again stops the execution for 10 seconds. In that way, processor executes 100 instructions and takes a break for 10 seconds after executing consecutive 10 instructions. Consider the following scenario:

1	
2	
3	
.	Instruction
10	
MOV ECX, 10	
L1:	
<Loop Body>	
Loop L1	
11	
12	
.	
20	
MOV ECX, 10	
L1:	
<Loop Body>	
Loop L1	
21	
22	
.	
100	

- i) By using the above procedure, processor can implement a delay of 10 seconds after every 10 instructions. Now, briefly explain what are the advantages and disadvantages of it.

- ii) If there is any disadvantages, find out the solution and explain the merits and demerits of the solution.

- (b) A certain memory has a capacity of 4K x 8

- i) How many data input and data output lines does it have?

4 CO4

- ii) How many address lines does it have?
 iii) What is its capacity in bytes?
 iv) Draw the diagram of the memory.
 (c) We know that semiconductor memories are used as the main memory of a computer. Another form of memory is the auxiliary memory which has the capacity to store massive amount of data without the need for electrical power. Now, in a class of "peripheral and interfacing", Karim said- "A computer system normally uses high-speed main memory and slower external auxiliary memory". Justify this statement of Karim. 3 CO4
 (d) Which memory stores the most bits: stores 3M memory or a memory that stores 3M words at a word size of 16 bits? 5Mx8 2 CO4
 Q.6. (a) 3Mx16 8251 USART stands for Universal synchronous asynchronous receiver transmitter. We can connect 8251 with 8086 microprocessor either in I/O mapped I/O or in memory mapped I/O mode. Now, consider the figure 6(a) what should be addresses of 8251 USART? 3 CO3

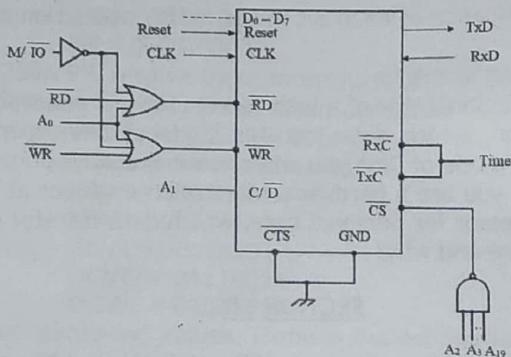


fig. 6(a)

- (b) For the given DAC of fig 6(b), find the full scale output voltage, if $R_f = 2\text{K}\Omega$ and $R = 1\text{K}\Omega$. Find the output voltage when the output is 101100 and reference voltage = 5V. 4 CO3

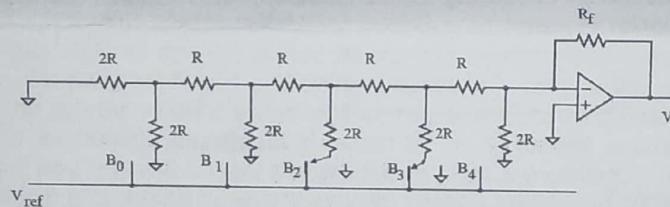


fig. 6(b)

- (c) Consider the following binary weighted resistor DAC of fig 6(c), find the V_{max} and V_{min} for $R_f = R$ and $V_{ref} = 5\text{V}$. Also mention the drawbacks of the circuit. 5 CO3

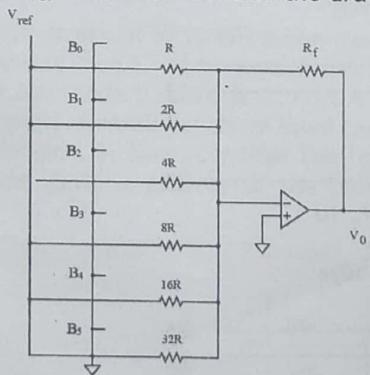


fig. 6(c)

- Q.7. (a) Nowadays, many types of DACs (Digital to Analog Converters) are available, Binary weighted Resistor is one of the types. It utilizes a summing op-amp circuit. Here, transistors are used to switch between V_{ref} and ground (bit high or low). Consider the following configuration of a binary-weighted DAC (fig. 7(a)) and determine the output voltage. Redraw the picture when the input is 10101110. 5 CO2

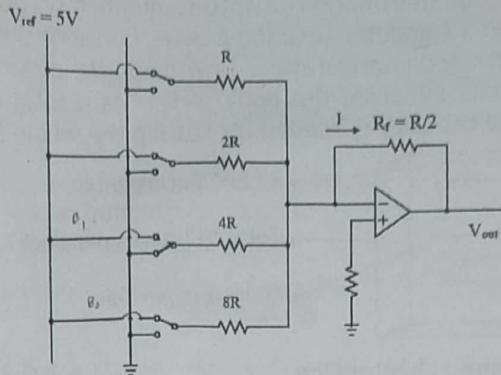


fig. 7(a)

- (b) Successive approximation ADC is used to convert the analog input voltage to its equivalent digital output. Let's consider $V_{in} = 11.2V$, and $V_{ref} = 16V$. Now, using the following output generation graph, draw the SAR-tree for all possible output combinations.

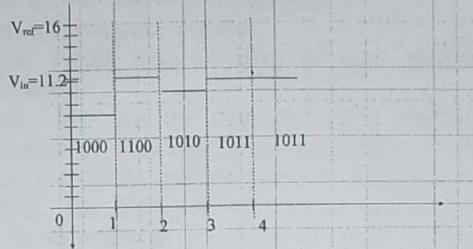


Fig. 7(b)

4 CO4

- (c) Let us assume that, you are an engineer of a renowned hardware manufacturer company. You have to build different DMA chips for different operations, which types of data transfer modes of DMA should be used for the following operations:

- To perform high-speed data transfer operations between server applications.
- To perform printing type operations.
- To perform such operations, where the processor is completely busy with instructions from retrieving stack and does not need the system bus.
- CPU and DMA share the bus cycles equally with each other.

- Q.8. (a) 8086 can not deal with floating point-numbers. Therefore, it deals with complex arithmetic operations such as roots, logarithmic trigonometric functions with the help of 8087 math co-processor. While interfacing with the 8086 microprocessor, 8288 bus controller generates control signals, for the 8087 math co-processor. Now, from the following table, which signal is generated by 8288 bus controller?

S'_2	S'_1	S'_0	Output
0	0	0	?
0	0	1	?
0	1	0	?
0	1	1	?
1	0	0	?
1	0	1	?
1	1	0	?
1	1	1	?

3 CO4

- (b) A peripheral device is an auxiliary device that connects to and works with the computer to either put information into it or get information out of it. Peripherals can be of two types: internal peripherals and external peripherals. Determine which of the followings are internal peripherals and which are external peripherals.

- Keyboard
- Mouse
- Graphics Card
- Hard-drive
- Loud speaker
- Printer.

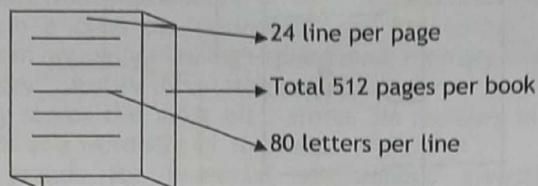
- (c) Consider the following sequence for a RAM and draw the timing diagram for the RAM. Note that these are sequential signals that mean there is no cycle-loss between two commands.

→ sequence: read, write, write, read

4 CO1

2 CO1

- (d) The smallest piece of information (a letter, number or punctuation mark) that can be stored in a computer is called a byte. Consider the book in the fig. 8(d) with the mentioned configuration. How many MB of storage capacity is needed for this book? Suppose, this book series has a total of 6 books. How many MB of storage capacity is needed for storing the whole book series?



I don't know my name: chapter One

Fig. 8(d)

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3rd Year Even Semester Examination 2021
COURSE NO: CSE 3201 COURSE TITLE: Operating Systems
FULL MARKS: 72 TIME: 3 HRS

- N.B. (i) Answer any SIX questions taking any THREE from each section.
(ii) Figures in the right margin indicate full marks.
(iii) Use separate answer script for each section.

<u>SECTION : A</u>				CO	Marks
Q.1.	(a)	Explain the following remark: "Linux is a monolithic kernel."	CO1	4	
	(b)	In a C program, the address of a variable can be obtained by using the "&" operator on a variable and assigning it to a pointer type. Discuss whether the pointer represents a logical address or physical address of the variable. Also, provide reasoning behind this design choice.	CO3	4	
	(c)	Explain cache coherence problem with a suitable example.	CO1	4	
Q.2.	(a)	Define zombie and orphan processes.	CO2	2	
	(b)	As a process executes, it changes states. Describe different states of a process with necessary diagram.	CO2	5	
	(c)	A fast-food restaurant has four kind of employees: (1) Order-takers, (2) Cooks, (3) Packaging specialists, and (4) Cashiers. Each employee can be regarded as a communicating sequential process. Explain the form of inter-process communication they use.	CO4	5	
Q.3.	(a)	Write the comparison among compile time, load time, and run time address binding schemes.	CO2	4	
	(b)	Consider a logical address space of 128 pages with a 2-kB page size, mapped onto a physical memory of 64 frames.	CO2	4	
	i)	Determine the number of bits in the logical address.			
Q.4.	ii)	Determine the number of bits in the physical address.			
	(c)	Explain the function of MMU with a suitable diagram.	CO2	4	
	(a)	Java programming language is designed to be platform-agnostic, with a focus on "write once, run anywhere" using byte code. Explain how Java byte code achieves portability.	CO1	4	
Q.4.	(b)	Consider the set of processes with arrival time (in milliseconds), CPU burst time (in milliseconds), and priority (0 is the highest priority) shown below. None of the processes has I/O burst time.	CO2	8	

Process Name	Arrival Time	Burst Time	Priority
P1	0	11	2
P2	5	28	0
P3	12	2	3
P4	2	10	1
P5	9	16	4

- i) Draw the Gantt chart using FCFS, non-preemptive priority scheduling and preemptive priority scheduling algorithm.
ii) Determine the average waiting time and average turnaround time for each of the above mentioned algorithms.
iii) Determine the better algorithm for the given scenario. Justify your answer.

SECTION : B

Q.5.	(a)	Describe any two system calls in UNIX-based OS.	CO1	3	
	(b)	Given six memory partitions of 50 KB, 400 KB, 130 KB, 300 KB, 150 KB, and 70 KB (in order) and five processes with space requirements of 230 KB, 180 KB, 130 KB, 120 KB, and 200 KB (in order). i) Determine the memory allocation of processes using the first-fit, best-fit, and worst-fit algorithms. ii) Determine external fragmentation for each of the above mentioned algorithms and deduce the most memory efficient algorithm.	CO3	5	
	(c)	Define file system. Discuss the importance of file system in OS.	CO4	4	
Q.6.	Consider the following reference string:		CO2		
			CO2		

1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6. Assuming demand paging with three frames, calculate the number of page faults for each of the following page replacement algorithms.

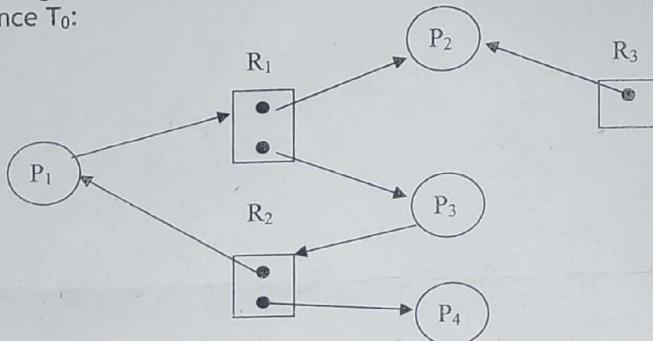
- | | |
|---|-------------------------------------|
| Q.7.
(a) FIFO
(b) LRU
(c) Optimal Page Replacement Algorithm
(d) Second-Chance Algorithm
(a) Define deadlock.
(b) Consider the following snapshot of a system | 3
3
3
3
CO2 2
CO4 10 |
|---|-------------------------------------|

Process	Allocation				Max				Available			
	A	B	C	D	A	B	C	D	A	B	C	D
P ₀	2	0	0	1	4	2	1	2	X	2	2	2
P ₁	3	1	2	1	5	2	5	2				
P ₂	2	1	0	3	2	3	1	6				
P ₃	1	3	1	2	2	4	2	4				
P ₄	1	4	3	2	3	6	6	5				

i) Determine the smallest value of X for which there is a safe sequence.

ii) Determine whether the system still be safe if a request from P₁ for (0,1,1,0) is granted immediately.

- Q.8. (a) Following resource allocation graph is a snapshot of a system at time instance T₀: CO4 6



i) Determine if the system is deadlocked or not. If the system is not deadlocked, find a safe sequence.

ii) At time instance T₁, P₄ makes a request for an instance of resource type R₃. Assume that no process has finished execution between T₀ and T₁. Determine if the system is deadlocked or not. If the system is not deadlocked, find a safe sequence.

- (b) Consider the following two code snippets: CO2 6

<pre> int var = 10; int main() { int pid = fork (); if (pid == 0) var = 100; else { wait (NULL); printf ("%d", var); } return 0; } </pre>	<pre> int var = 10; int main() { int pid = vfork (); if (pid == 0) var = 100; else { wait (NULL); printf ("%d", var); } return 0; } </pre>
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Determine and discuss the output of each snippet.

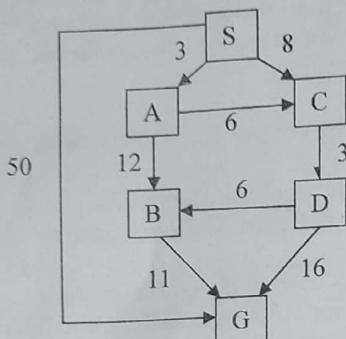
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COURSE NO: CSE 3209 COURSE TITLE: Artificial Intelligence
FULL MARKS: 72 TIME: 3 HRS

- N.B. (i) Answer any SIX questions taking any THREE from each section.
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SECTION : A

COs Marks

- Q.1. Suppose we have a graph with nodes S, A, B, C, D and G, where S is the start and G the goal node. The distances between connected nodes are:



The heuristic estimates of the distance to G are

from:	S	A	B	C	D	G
distance:	22	20	8	12	10	0

- (a) Perform a search with algorithm A. CO2 4
(b) Is the heuristic optimistic? Briefly explain your answer. CO2 4
(c) What does it mean for the search process if the heuristic function optimistic? CO2 4
- Q.2. (a) What is artificial intelligence? Briefly explain the following concepts. CO1 4
i) Iterative deepening.
ii) Turing test.
- (b) Consider a state space where the initial state is the number 1 and each state k has two successors: numbers $2k$ and $2k+1$. Suppose the goal state is 2010.
i) What is the branching factor in each direction of the bidirectional search?
ii) Write down a solution to this search problem.
- Q.3. (a) Running from You-Know-Who, Adil enters the CS building on the 1st floor. He flips a fair coin: if it is heads he hides in room 103, otherwise he climbs to the 2nd floor. In that case he flips the coin again, if it is heads he hides in SR, Otherwise he climbs to the 3rd floor. In that case he flips the coin yet again, if it is heads he hides in 301, otherwise he hides in the Men's room. What is the entropy of Adil's location? CO3 4
- (b) There are 100 parrots. They have either a red beak or a black beak. They can either talk or not. Complete the two cells in the following table so that the mutual information(i.e. information gain) between "Beak" and "Talk" is zero. Table is as follows: CO3 4
- | Number of Parrots | Beak | Talk |
|-------------------|-------|------|
| 10 | Red | Yes |
| ? | Red | No |
| ? | Black | Yes |
| 45 | Black | No |
- (c) Consider a Bayes network $A \rightarrow B \leftarrow C$ with binary variables and CPTs: CO3 4
 $P(A=T) = 1/4$.
 $P(B=T | A=T, C=T) = 1/3$.
 $P(B=T | A=T, C=F) = 1/\pi$.
 $P(B=T | A=F, C=T) = 1/42$.
 $P(B=T | A=F, C=F) = 2/(1+\sqrt{5})$.

- $P(C=T) = 0.540$.
 Compute $P(A=F|C=F)$.
- Q.4. (a) Explain First-Order logic with a suitable example. CO4 4
 (b) Let C1 be the clause $\neg\text{Republican}(\text{Mother}(x)) \vee \text{Republican}(x)$ and let C2 be the clause $\neg\text{Republican}(y) \vee \text{likes}(y, \text{Sarah}) \vee \neg\text{Resident}(y, \text{Alaska})$. What is the result of applying the resolution rule of inference to C1 and C2? CO4 4
 (c) Are the following two expressions unifiable? If so, what is the most general unifier? Is not, why? CO4 4

SECTION : B

- Q.5. (a) Why is conflict resolution important? What to do if there is more than one (1) matching rule in each inference cycle? CO1 2
 (b) Suppose, you are instructed to develop an MRI machine that can scan the upper abdomen of human body. What type of knowledge will you use for knowledge designing and reasoning? CO1 2
 (c) Consider the following set of rules:
 R1: IF engine does not turn AND battery is not flat THEN ask user to test starter motor.
 R2: IF there is no spark THEN ask user to check the points.
 R3: IF engine turns AND engine does not start THEN ask user to check the spark.
 R4: IF engine does not turn THEN ask user to check the battery.
 R5: IF battery is not flat THEN ask user to charge battery and EXIT.
 Now, if the initial facts are "Engine does not turn" and "battery is not flat":
 i) Find out the conflict set and write in appropriate format.
 ii) Which conflict resolution strategy will be appropriate here and why? Explain briefly.
 (d) Consider the diagram in the following figure: CO1 4

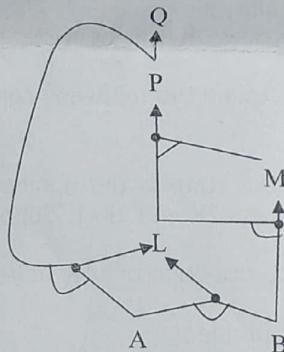


Figure: Chaining

- i) What type of chaining does the diagram represent?
 ii) Whether the diagram fact-driven or goal-driven?
 iii) Generate the rules which are represented by the diagram.
- Q.6. (a) Explain Bayes theorem with example. CO3 3
 (b) A certain disease affects about 1 out of 10,000 people. There is a test-to check whether the person has the disease. The test is quite accurate. In particular, we know that:
 - the probability that the test result is positive (suggesting the person has the disease), given that the person does not have the disease, is only 2 percent.
 - the probability that the test result is negative (suggesting the person does not have the disease), given that the person has the disease, is only 1 percent.
 A random person gets tested for the disease and the result comes back positive. What is the probability that the person has the disease?
- (c) We would like to predict the sex of a person based on two binary attributes: leg-cover (pants or skirts) and facial-hair (some or none). We have a dataset of 2000 individuals, half male and half female. 75% of the males have no facial hair. Skirts are worn by 50% of the females.
 All females are barefaced and no male wears a skirt. CO3 5

- i) What is the initial entropy in the system?
 ii) Compute the information gain of initially choosing the attribute leg-cover and for initially choosing facial-hair.
 iii) Based on your calculations, which attribute should be used as the root of a decision tree?
- Q.7. (a) What do you mean by admissibility of an algorithm and depth of a problem? CO2 2
 (b) Define adversarial search. Explain the drawbacks of hill-climbing search with figures and mention the corresponding solutions. CO2 4
 (c) Consider the following game-tree where the upward triangles represent MAX player and down-ward triangles represent MIN player. CO2 6

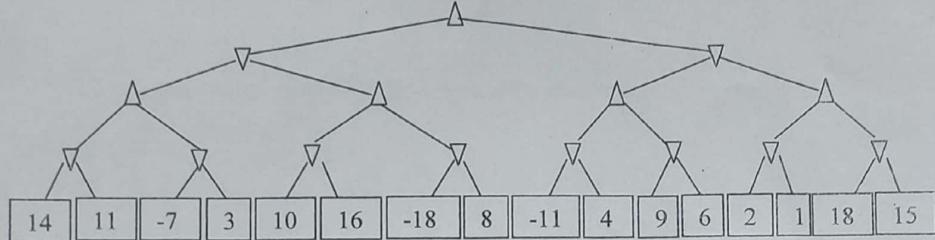


Figure: Game tree for α - β pruning

Now,

- i) Fill-up the triangles with final values which represent the corresponding node values (where applicable) considering α - β pruning.
 ii) Write the final α and β values for each of the corresponding triangles at the right side of it (where applicable).
 iii) Use double slash (//) to prune a branch.
- Q.8. (a) What is problem formulation? Formulate an 8-puzzle problem for random initialization and goal state. CO2 4
 (b) There is a 1% probability for a hard drive to crash. Therefore, it has two backups, each having a 2% probability to crash, and all three components are independent of each other. The stored information is lost only in an unfortunate situation when all three devices crash. What is the probability that the information is saved? CO3 4
 (c) What is Bayesian reasoning? Consider the Bayes net as shown in the following figure. Now, compute the following probabilities from the given Bayes net. CO3 4
- i) $P(A|B)$
 ii) $P(B|D)$
 iii) $P(C|B)$

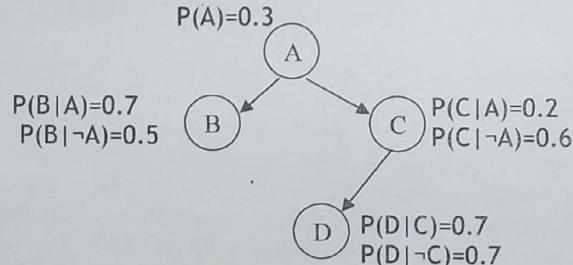


Figure: Bayes net

Heaven's Light Is Our Guide
RAJSHAHI UNIVERSITY OF ENGINEERING & TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
3rd Year Even Examination 2021
COURSE NO: CSE 3205 COURSE TITLE: Computer Networks
FULL MARKS: 72 TIME: 3 HRS

N.B. (i) Answer any SIX questions taking any THREE from each section.
(ii) Figures in the right margin indicate full marks.
(iii) Use separate answer script for each section.

<u>SECTION : A</u>		Marks	CO
Q.1.	(a) Differentiate TCP/IP and OSI reference model. (b) What are the reasons for using layered protocols? State the purpose of each layer of OSI model. (c) Find the class and network address of the following addresses: i) 227.12.14.87 ii) 193.14.56.22 iii) 252.5.15.111	3 5 4	C01 C01 C02
Q.2.	(a) Explain the purpose of using 'sequence number' and 'age' in link state packets. (b) Compare connection oriented service and connectionless service of network layer. Mention at least two applications of both. (c) Describe the desired properties of routing algorithm. Explain optimality versus fairness.	4 4 4	C04 C04 C04
Q.3.	(a) Define IP address. Can any Smartphone have two different IP addresses at the same time? Justify your answer. (b) Describe the reasons for subnetting a network. Can subnetting ensure zero IP wastage? Provide necessary arguments for your answer. (c) Suppose, A new university has opened up recently in Rajshahi. It has four departments till now BBA, LAW, CSE and EEE. Now the university hired a network administrator to manage the networks within university. The requirement of PC (hosts) are listed as below	3 3 6	C02 C02 C02
	BBA - 200 LAW - 150 CSE - 500 EEE - 350		
	The original IP address brought by the university is 172.16.0.0/18. Find the followings: i) Subnet mask of CSE department ii) 12 th PC address of EEE department iii) Last PC address of LAW department iv) Broadcast address of BBA department.		
Q.4.	[P.S: IP address are assigned sequentially] (a) Explain the count to infinity problem with proper example. Put forward solution to solve the problem. (b) Define congestion control. Differentiate between two ways of traffic shaping. (c) Between pure ALOHA and slotted ALOHA which one provides the lowest collision rate explain with proper example.	4 4 4	C03 C03 C03

SECTION : B

Q.5.	(a) Define Framing. Explain the advantage of bit stuffing over byte stuffing with proper example. (b) Justify which kind of error is most likely in real life scenarios between single bit error and burst error. If data is sent at a rate of 1 Gbps, then how many bits will be affected by a noise of 10ms duration? (c) Sender and receiver are using checksum for error detection. At some point in the communication, receiver has received the following message.	4 4 4	C03 C03 C03
	0101 1100 0011 0011 0110 1100 0110 1001		
	Find out if any error occurred or not while the message was transmitting via the medium?		
Q.6.	(a) Station A needs to send a message consisting of 9 packets to station B using sliding window (window size=3) and Go Back-n error control	4	C03

strategy. All packets are immediately available for transmission. If every 5th packet that A transmits gets lost (but no ACKs from B ever get lost), then find out the number of packets that A will transmit for sending the message to B.

- (b) Explain the coding and encoding process of CDMA with proper example. 4 CO4
(c) Sender and Receiver have agreed upon Hamming code for error correction. Now at a certain time receiver has received the following message. 4 CO3

101101010110
Find out the position in which the error occurred if any error is detected.

- Q.7. (a) Suppose data stream "A B ESC C ESC FLAG FLAG D" needs to be transmitted at the data link layer. What is the output after byte stuffing? 3 CO3
(b) Explain piggybacking. Discuss the advantages and disadvantages of it. 4 CO3
(c) Distance vector routing is used and the following vectors have just come in to router C: 5 CO3

from B: (5, 0, 8, 12, 6, 2)

from D: (16, 12, 6, 0, 9, 10)

from E: (7, 6, 3, 9, 0, 4)

The costs of the links from C to B, D and E are 6, 3 and 5, respectively. What is C's new routing table? Give both the outgoing line to use and the cost.

- Q.8. (a) Given that keyword "MONARCHY" and plaintext = "RUET" calculate the cipher text using play-fair method. 5 CO5
(b) Discuss the difference between monoalphabetic cipher, polyalphabetic cipher and one-time pad with proper example. 4 CO5
(c) List the applications of crypto Hash functions. Explain any of them. 3 CO5
