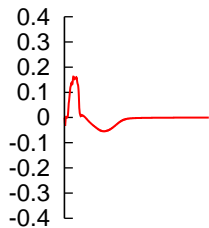
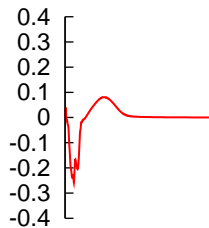
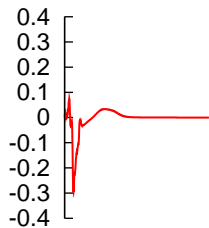
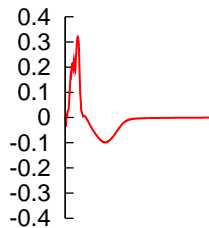


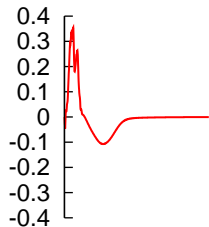
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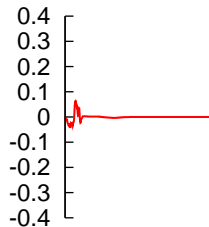
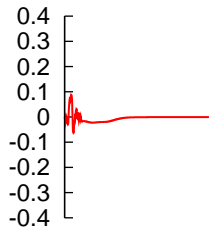
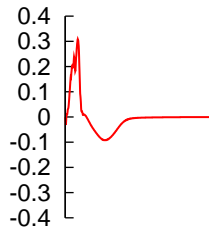
aVR

 $V_1$  $V_4$ 

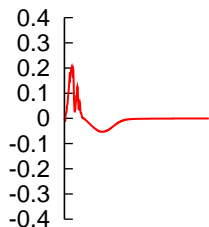
II



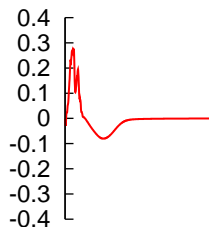
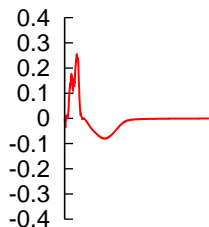
aVL

 $V_2$  $V_5$ 

III



aVF

 $V_3$  $V_6$ 