HOMEWORK I (Part I) Report

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Summary what has been done:

[universal counter]

* RTL level design - 16 bit counter (Fig.1)
* Pre-synthesis simulation (Fig.2 ~ Fig.9)
* Synthesis
* Post-synthesis simulation with Error (Fig.10)
* nLint analysis (Fig.11)
* README file for ucounter

[universal counter]

* Pre-synthesis simulation (Fig.12)
* Synthesis
* Post-synthesis simulation (Success!)
* nLint analysis (Fig.13)
* README file for alu

Required tools:

* Lab: NC-Verilog, Debussy (nTrace & nWave), Design Compiler(dv)
* Ubuntu: Icarus Verilog (iverilog), gtkwave, Dia

Learned lessons:

* Stuck:
  + Unfamiliar with Verilog language.
  + Design 16 bit counter with 8 bit counter modules.
  + Draw block diagram.

16 bit counter design:

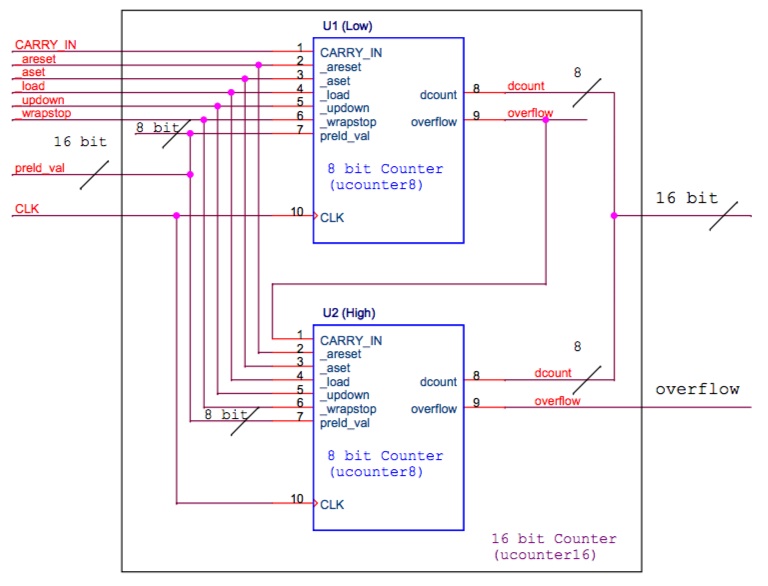


Fig 1: RTL level design - 16 bit counter

Pre-simulated waveforms:

* \_areset



Fig 2: Pre-simulated waveforms for \_areset

* \_aset

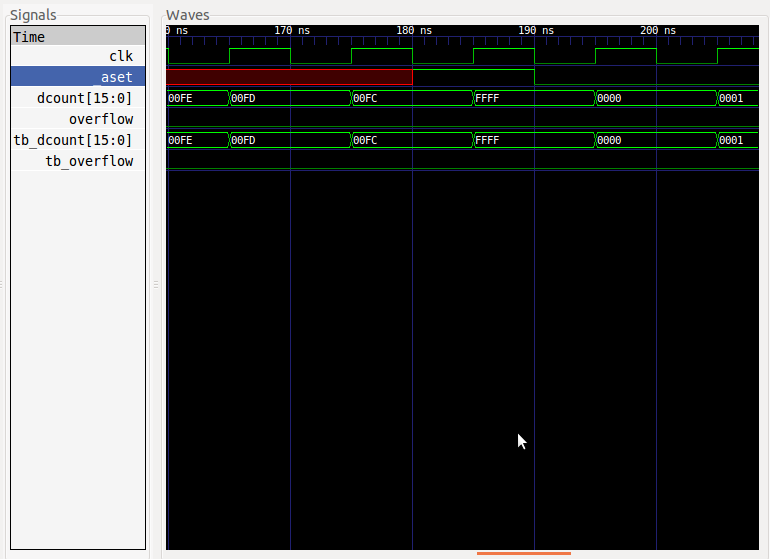


Fig 3: Pre-simulated waveforms for \_aset

* \_load and preld\_val

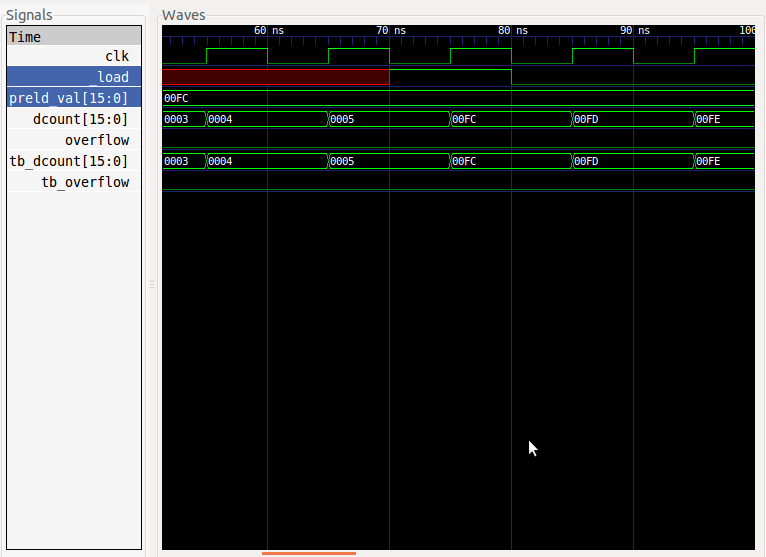


Fig 4: Pre-simulated waveforms for \_load and preld\_val

* \_updown (up)

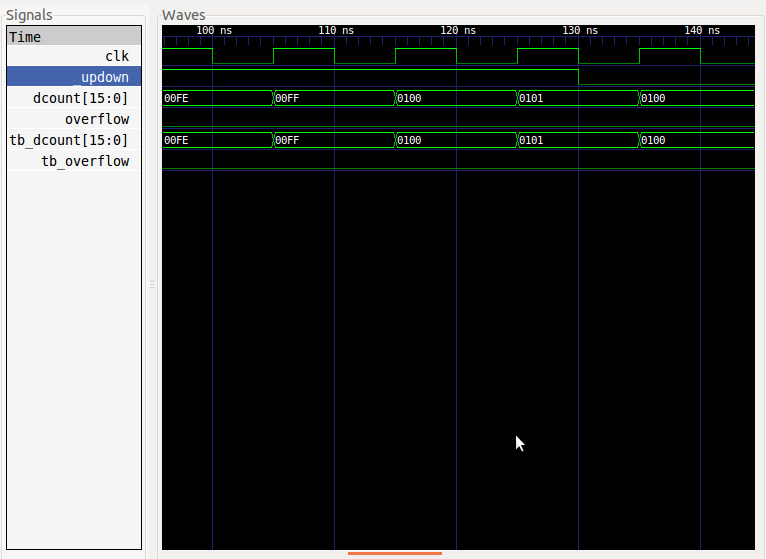


Fig 5: Pre-simulated waveforms for \_updown (up)

* \_updown (down)

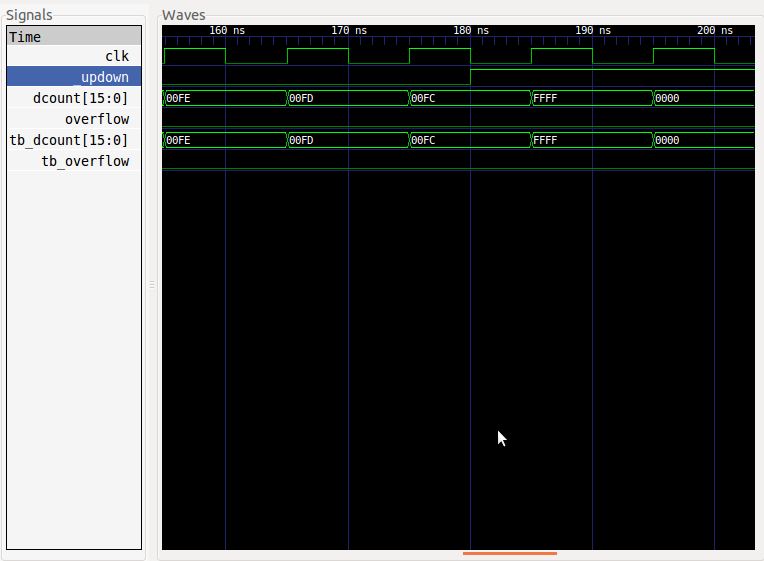


Fig 6: Pre-simulated waveforms for \_updown (down)

* \_wrapstop (cycle)

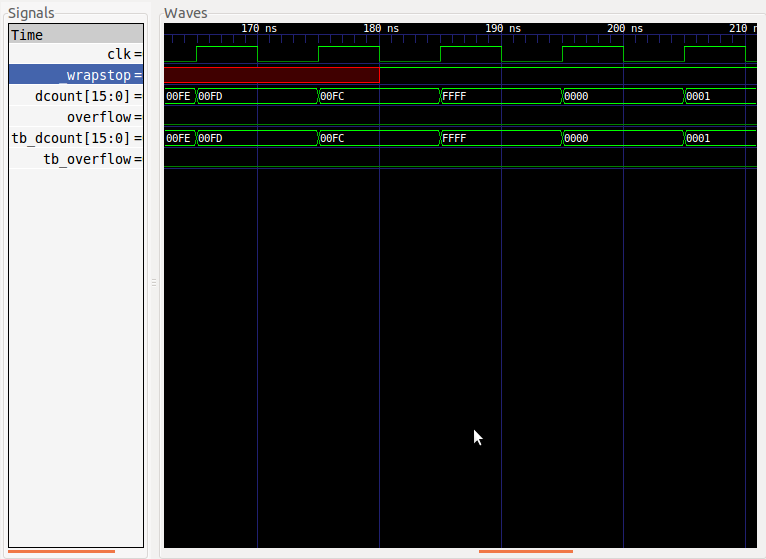


Fig 7: Pre-simulated waveforms for \_wrapstop (cycle)

* \_wrapstop (stop) and overflow

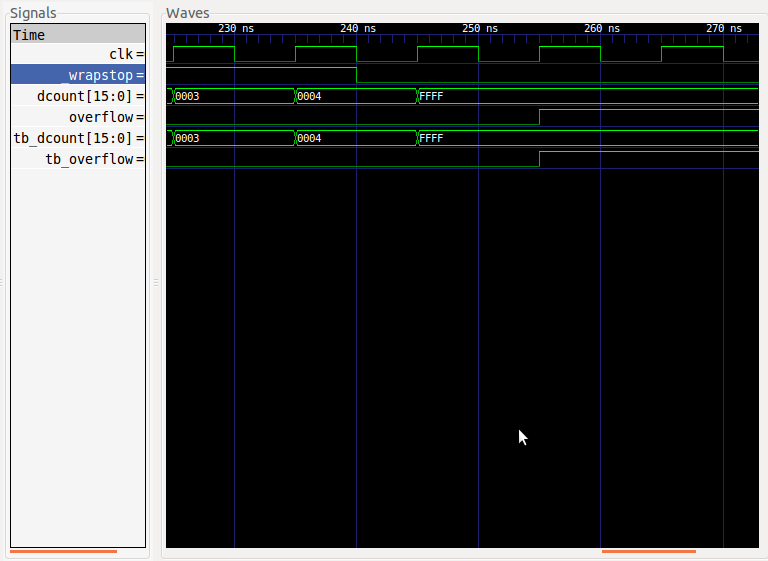


Fig 8: Pre-simulated waveforms for \_wrapstop (stop) and overflow

* Know issue:

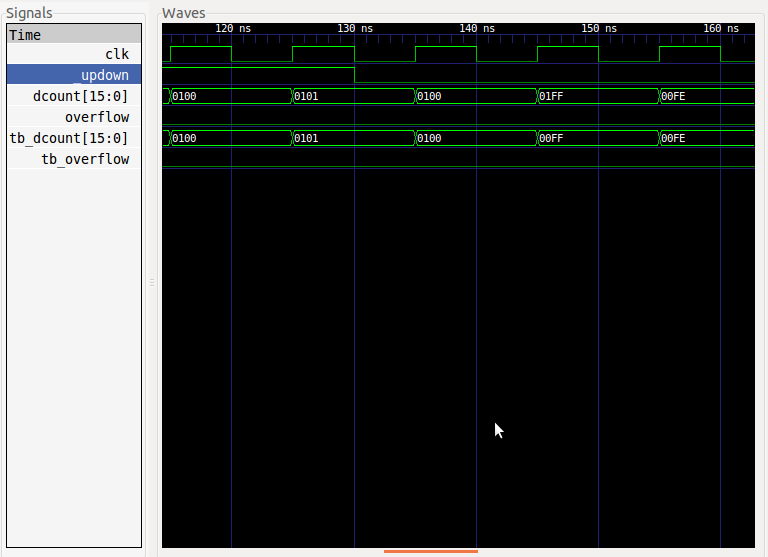


Fig 9: Result error.

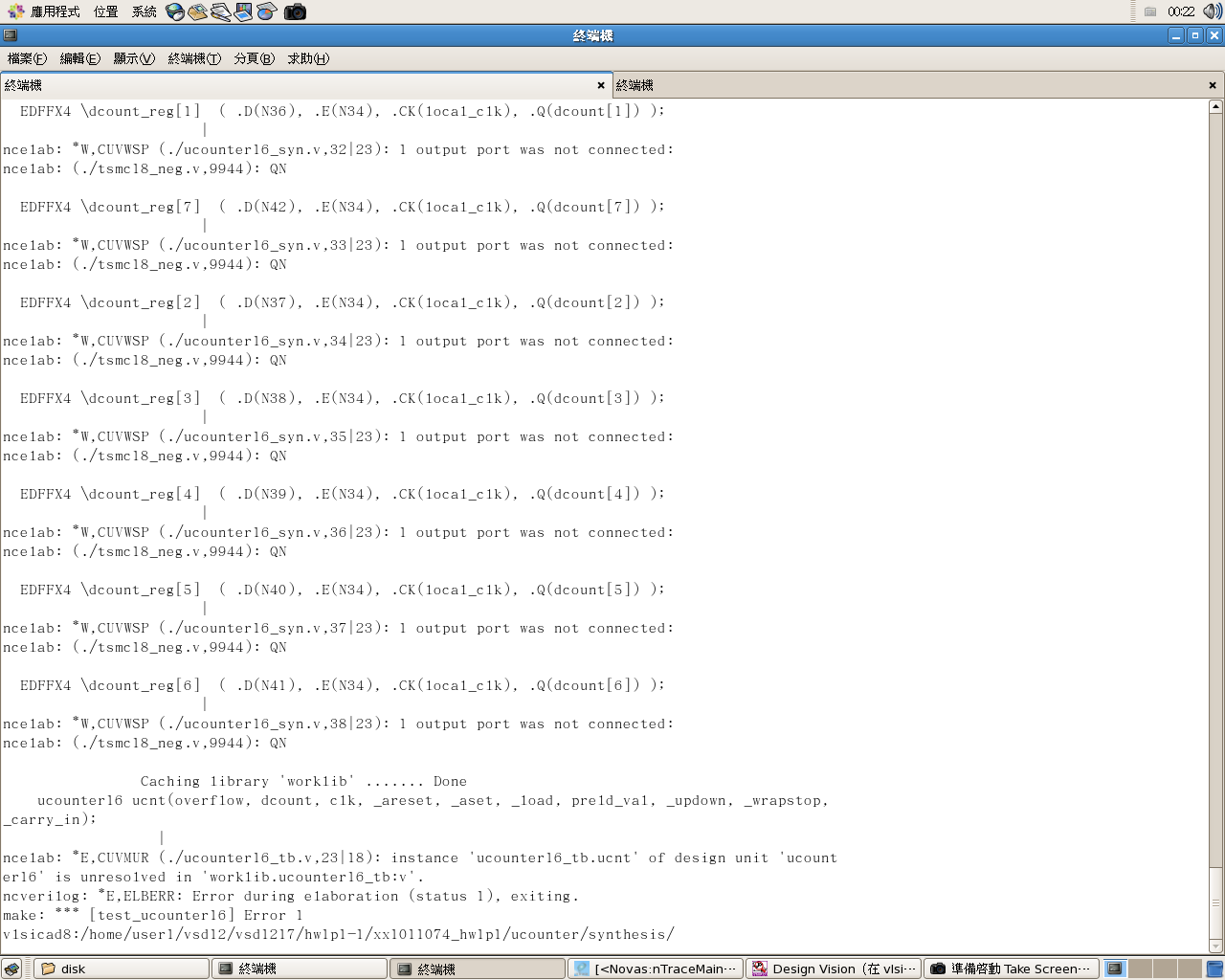


Fig 10: dv errors

EDFFX4 \dcount\_reg[0] ( .D(N35), .E(N34), .CK(local\_clk), .Q(dcount[0]) );

|

ncelab: \*W,CUVWSP (./ucounter16\_syn.v,31|23): 1 output port was not connected:

ncelab: (./tsmc18\_neg.v,9944): QN

EDFFX4 \dcount\_reg[1] ( .D(N36), .E(N34), .CK(local\_clk), .Q(dcount[1]) );

|

ncelab: \*W,CUVWSP (./ucounter16\_syn.v,32|23): 1 output port was not connected:

ncelab: (./tsmc18\_neg.v,9944): QN

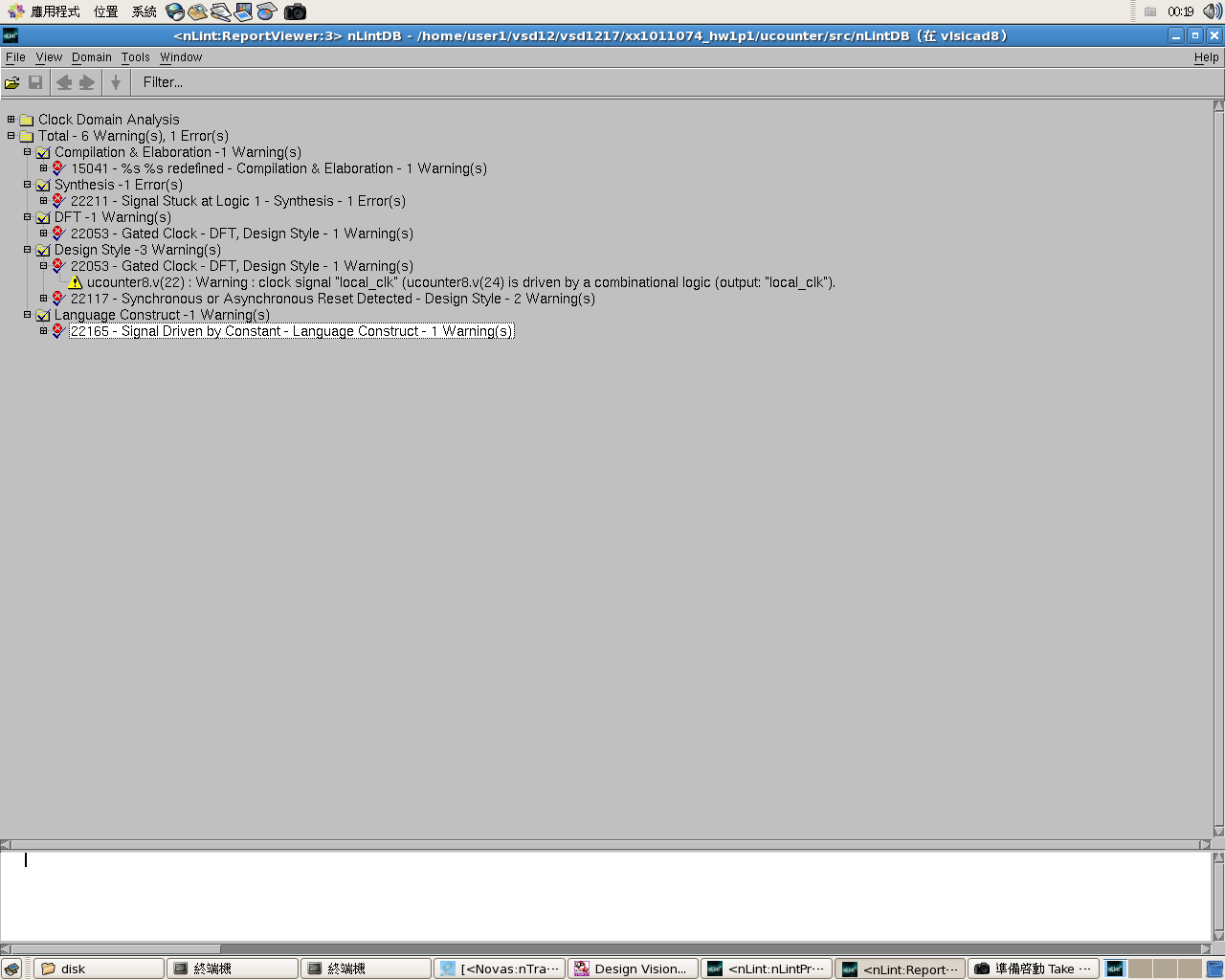
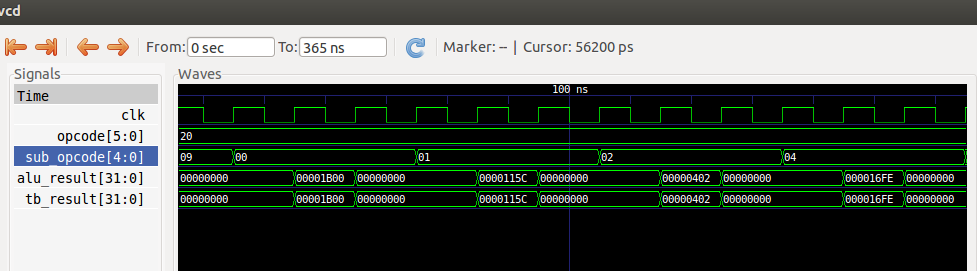
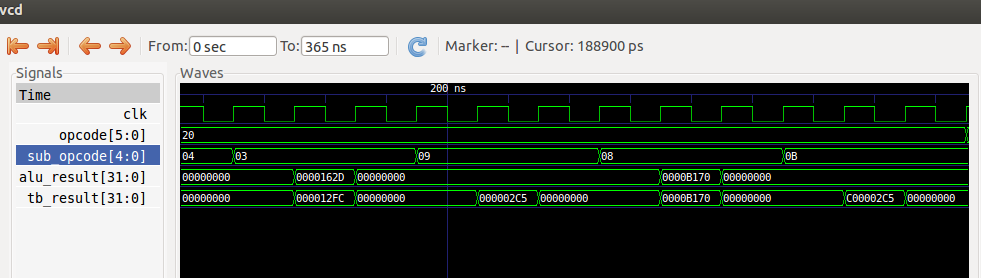


Fig 11: nLint errors (ucounter8.v & ucounter16.v)





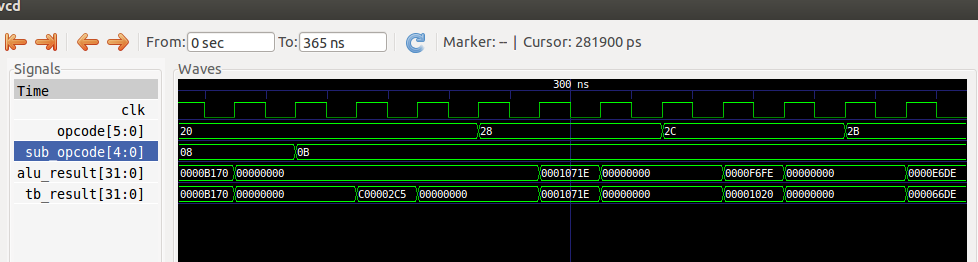


Fig 12: Waveform for ALU

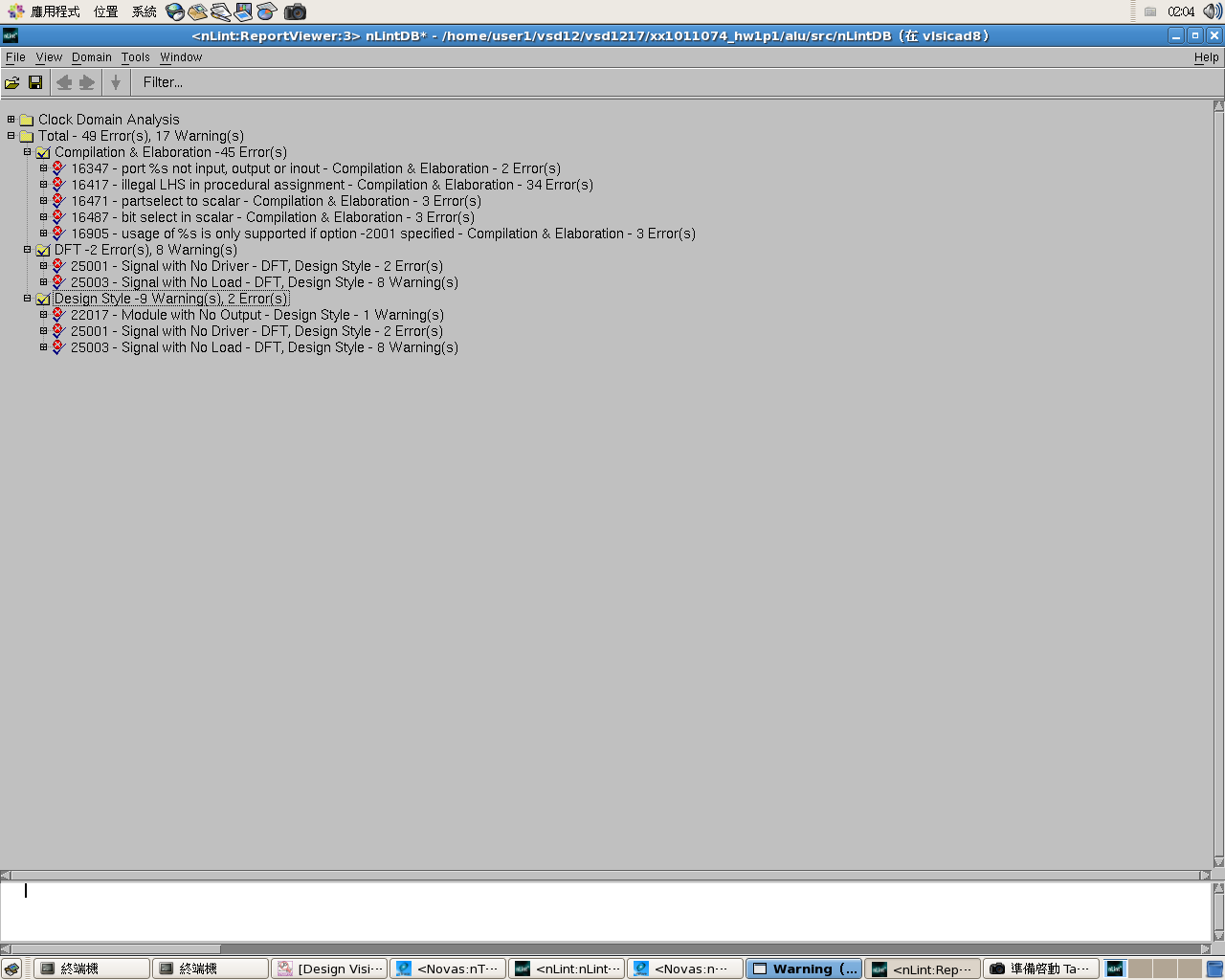


Fig 13: nLint errors (alu32.v)

ucounter

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Usage:

$ cd ucounter

$ make test\_ucounter16

Description:

RTL/ucounter16.v - Top module for 16 bit counter.

RTL/ucounter16\_tb.v - Testbench for 16 bit counter.

RTL/ucounter8.v - Module for 8 bit counter.

RTL/ucounter8\_tb.v - Testbench for 8 bit counter.

RTL/nLintErros - Screenshot of nLint errors.

pre-syn/ucounter16\_tb.vcd - Dumped file.

pre-syn/ucounter16\_tb.fsdb - Dumped file.

post-syn/ucounter16\_syn.v - Timing report.

post-syn /ucounter16\_syn.sdf - Timing information.

post-syn /ucounter16\_tb.v - Modified file for gate level simulation.

post-syn /dv\_erros - Error message at gate level simulation.

post-syn /dv\_erros.png - Screenshot of dv errors.

alu

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Usage:

$ cd alu

$ make test\_alu32

Description:

RTL/alu32.v - Top module for 32 bit ALU.

RTL/alu32\_tb.v - Testbench for 32 bit ALU.

RTL/nLintErros - Screenshot of nLint errors.

pre-syn/alu32\_tb.vcd - Pre-synthesis dumped .vcd file.

pre-syn/ alu32\_tb.fsdb - Pre-synthesis dumped .fsdb file.

post-syn/ alu32\_syn.v - Timing report.

post-syn / alu32\_syn.sdf - Timing information.

post-syn / alu32\_tb.v - Modified file for gate level simulation.

pre-syn/alu32\_tb.vcd - Post-synthesis dumped .vcd file

pre-syn/ alu32\_tb.fsdb - Post-synthesis dumped .fsdb file