HOMEWORK I (Part I) Report

Summary what has been done:

* RTL level design (16 bit counter)
* Pre-synthesis simulation
* Synthesis
* Post-synthesis simulation

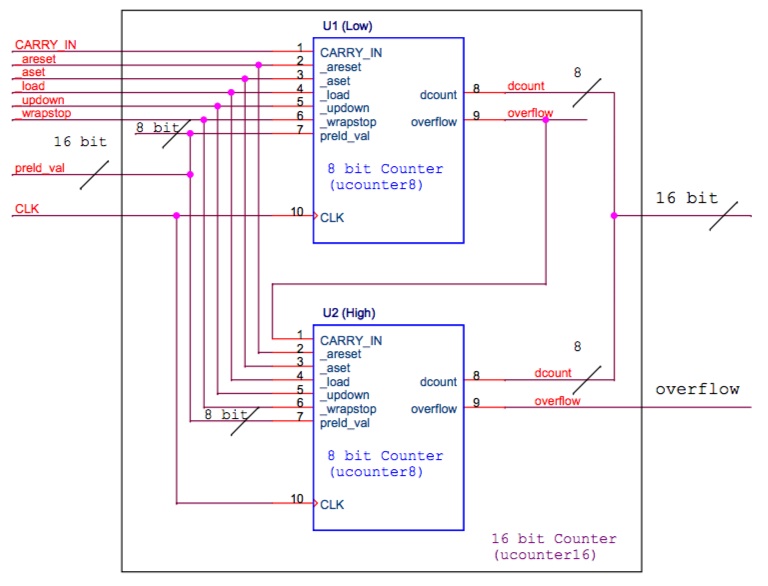
Required tools:

* Lab: NC-Verilog, Debussy (nTrace & nWave), Design Compiler(dv)
* Ubuntu: Icarus Verilog (iverilog), gtkwave, Dia

Learned lessons:

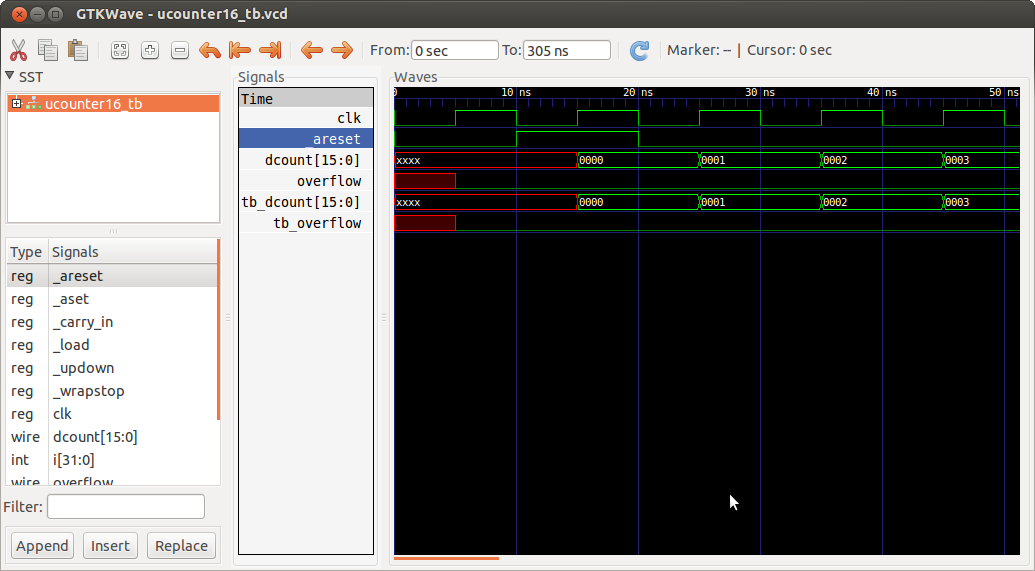
* Stuck:
  + Unfamiliar with Verilog language.
  + Design 16 bit counter with 8 bit counter modules.
  + Draw block diagram.
* Find:
* Exciting things:

16 bit counter Design:

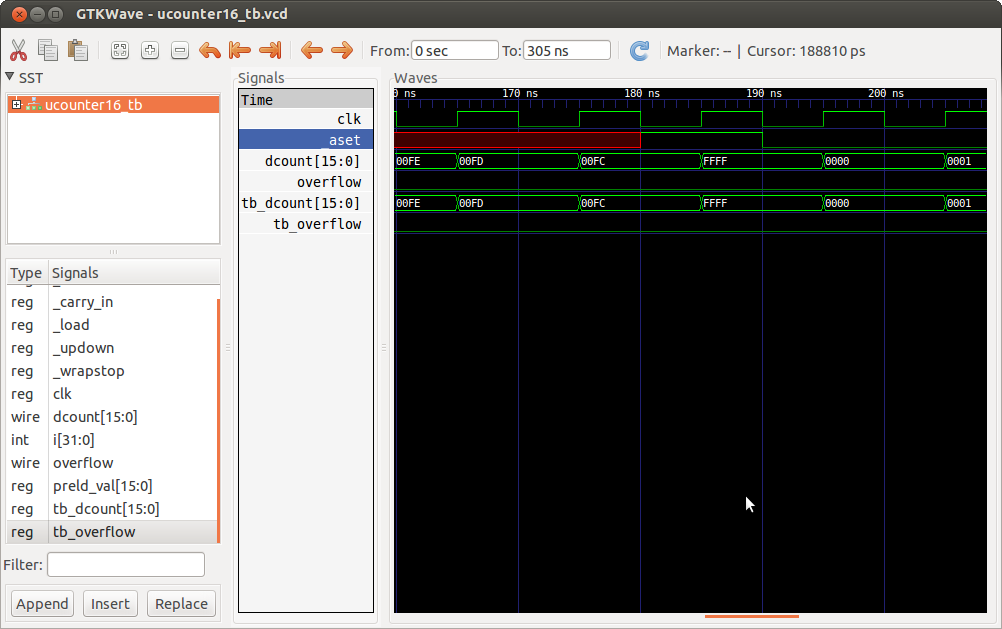


Pre-simulated waveforms:

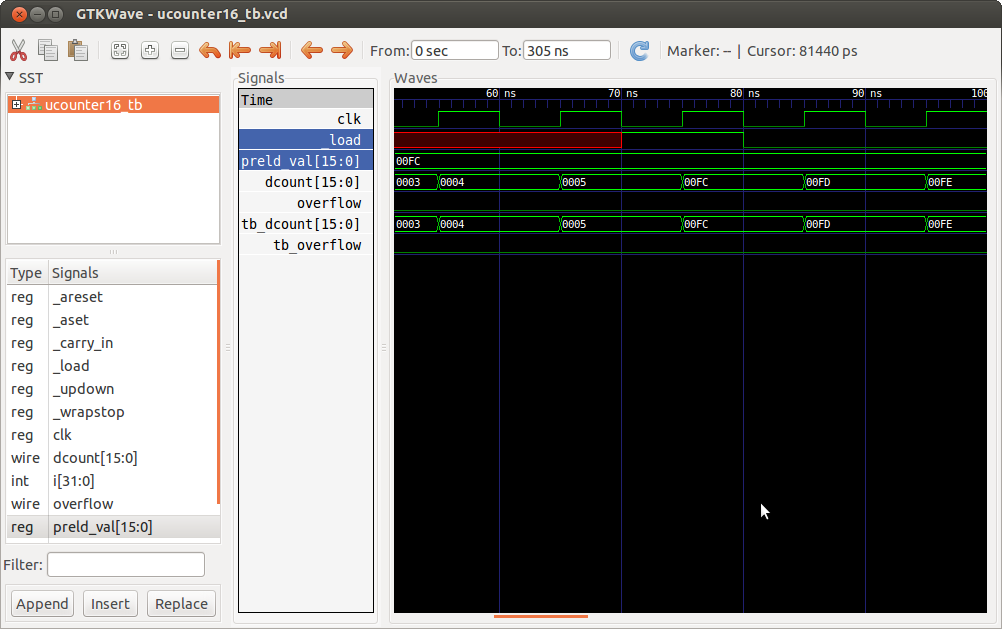
* Test 1. \_areset



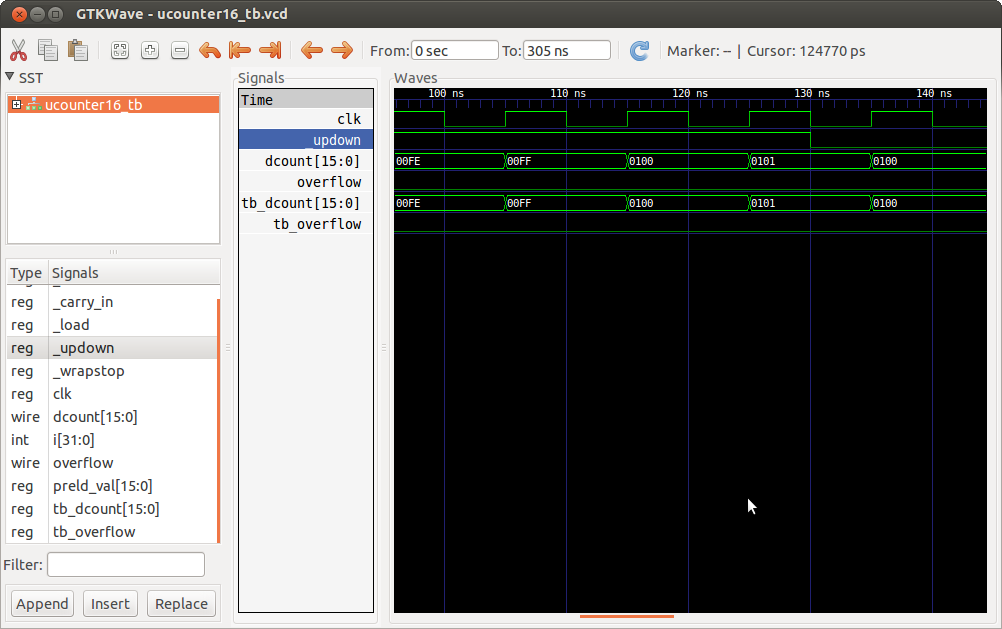
* Test 2. \_aset



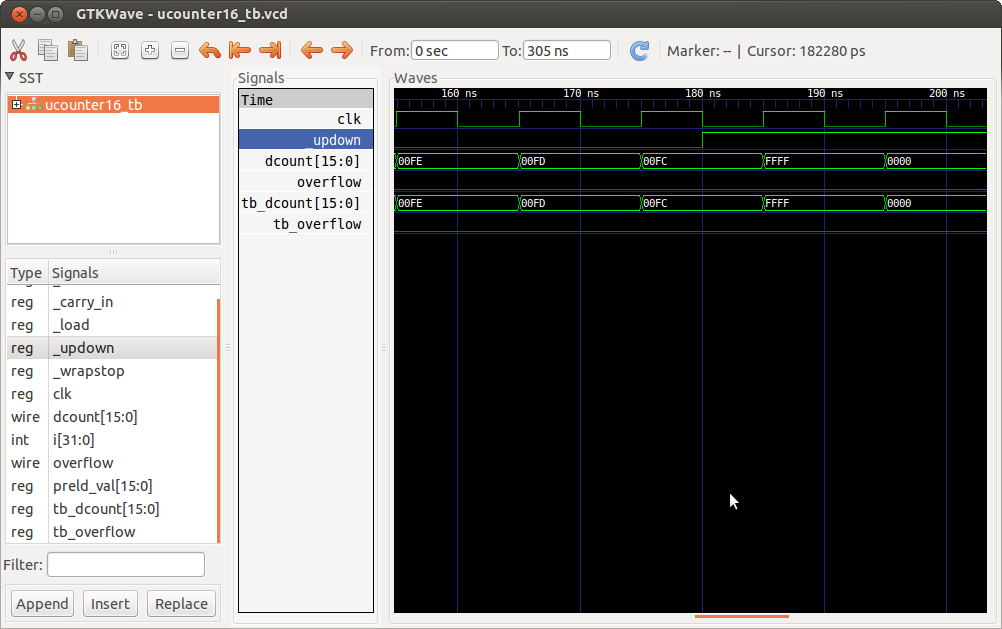
* Test 3. \_load and preld\_val



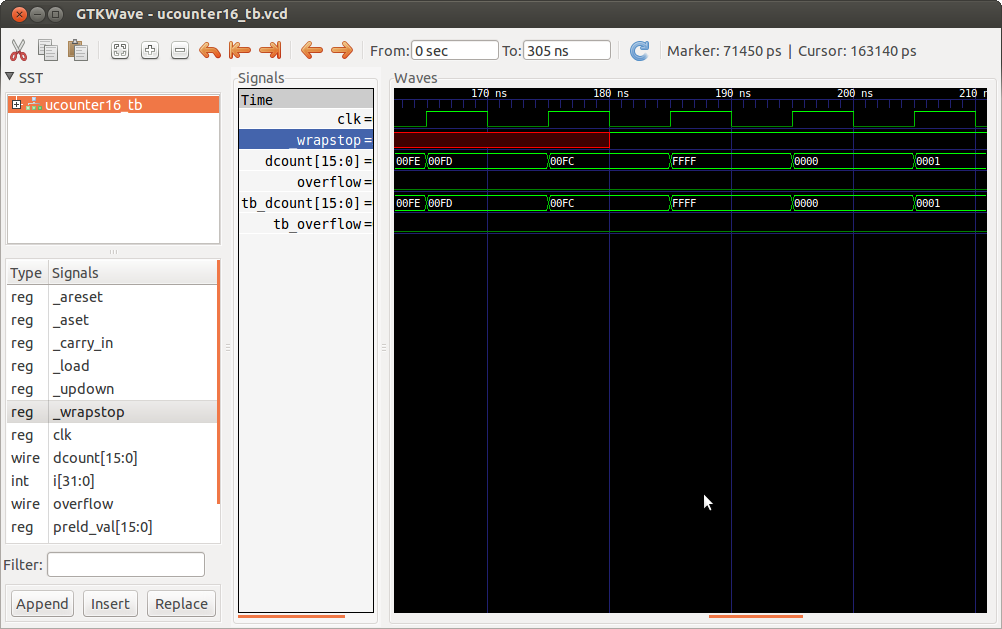
* Test 4. \_updown (up)



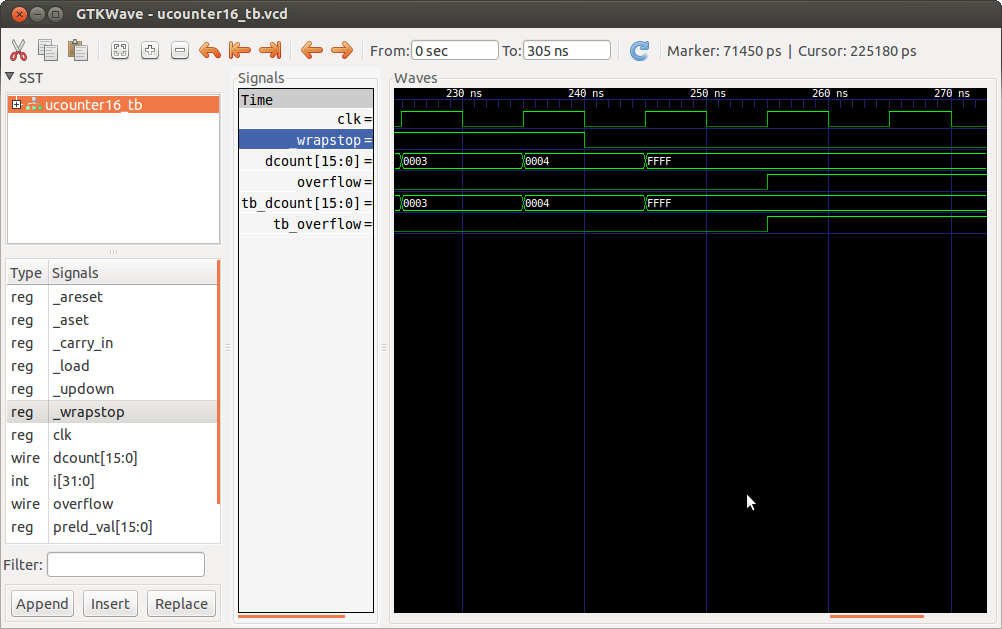
* Test 5. \_updown (down)



* Test 6. \_wrapstop (cycle)

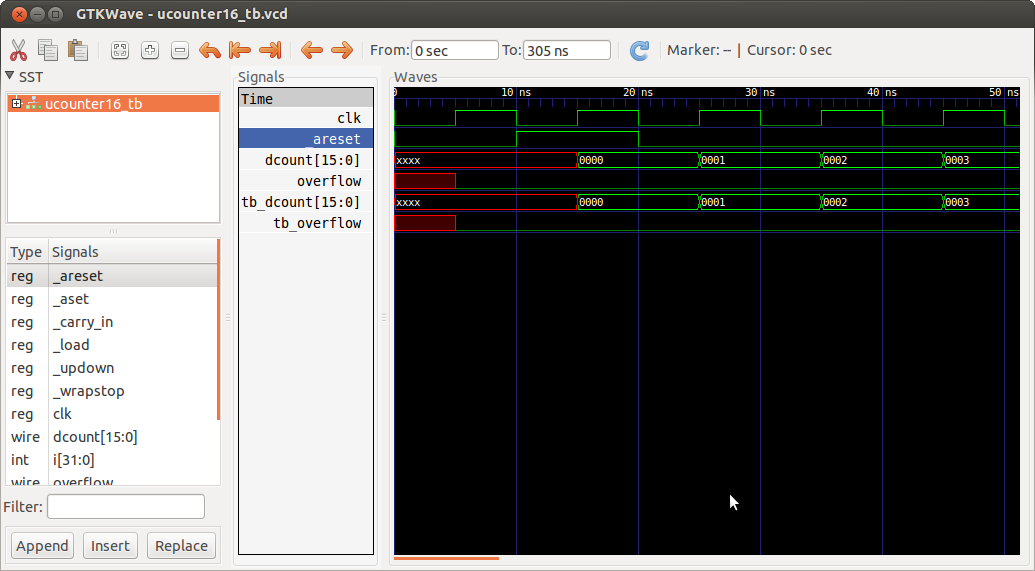


* Test 7. \_wrapstop (stop) and overflow

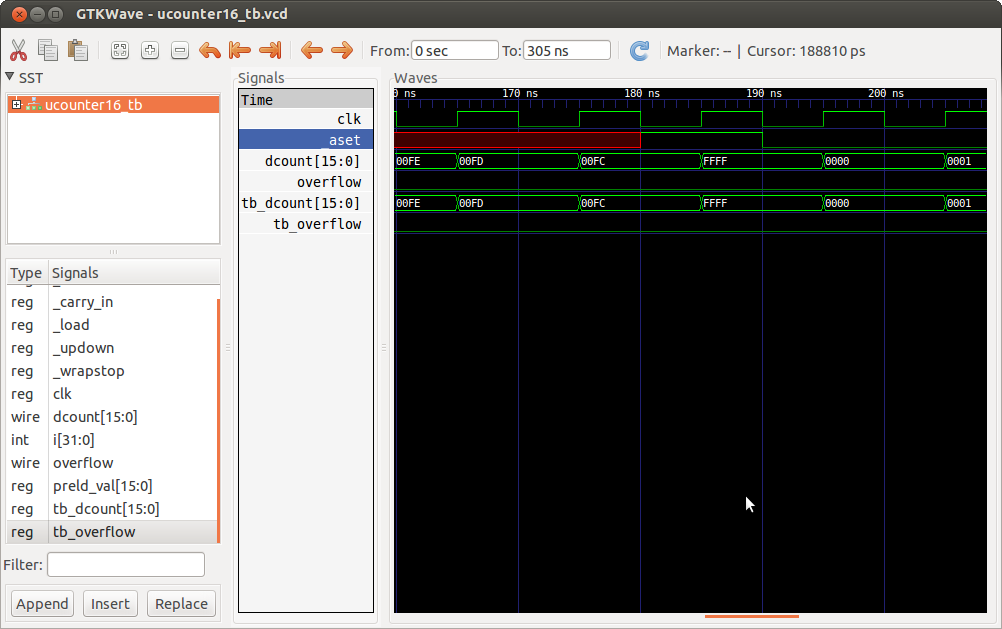


Post-simulated waveforms:

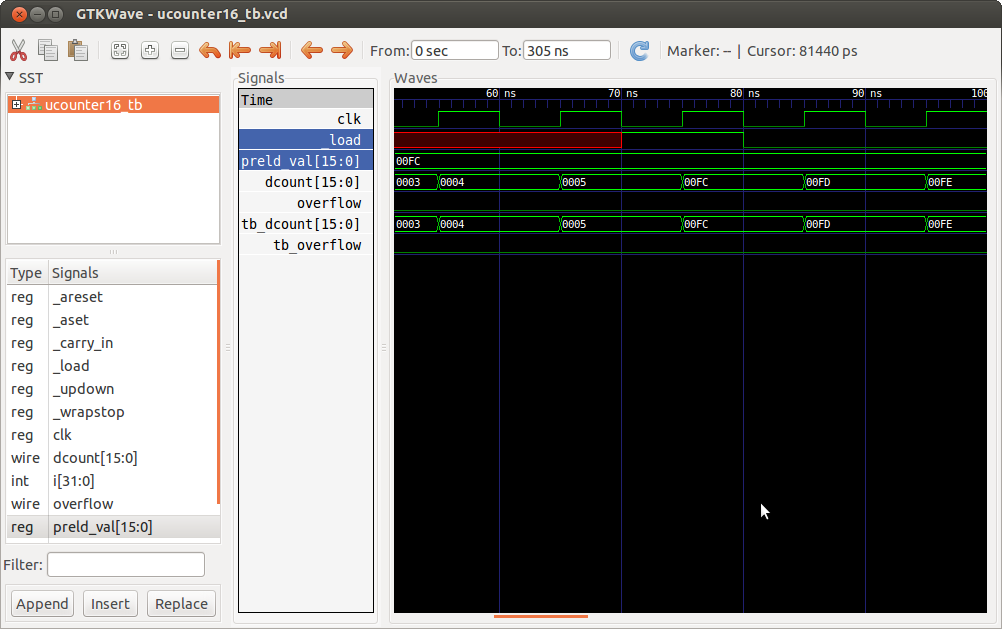
* Test 1. \_areset



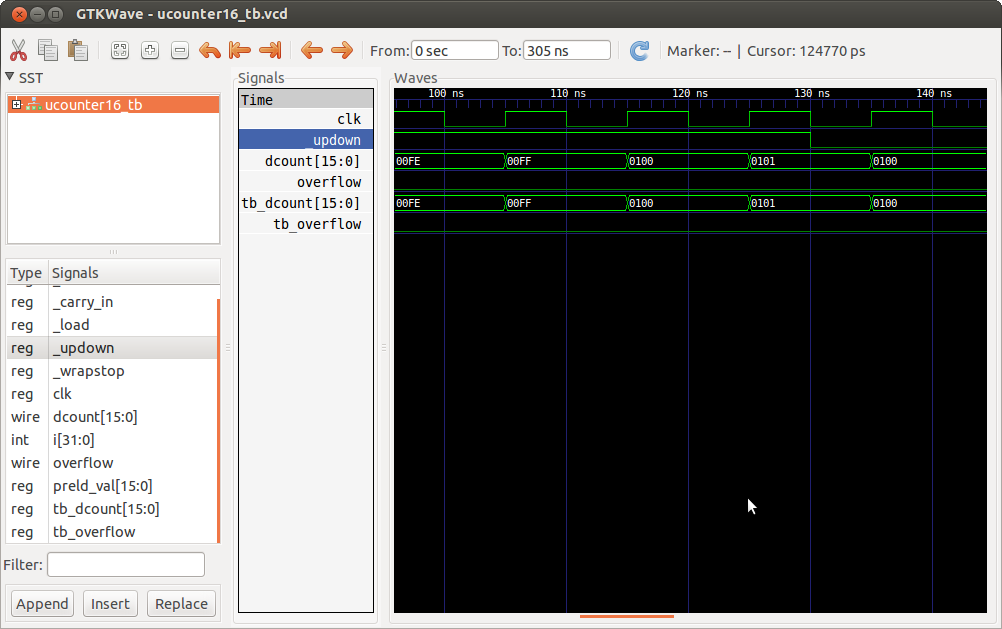
* Test 2. \_aset



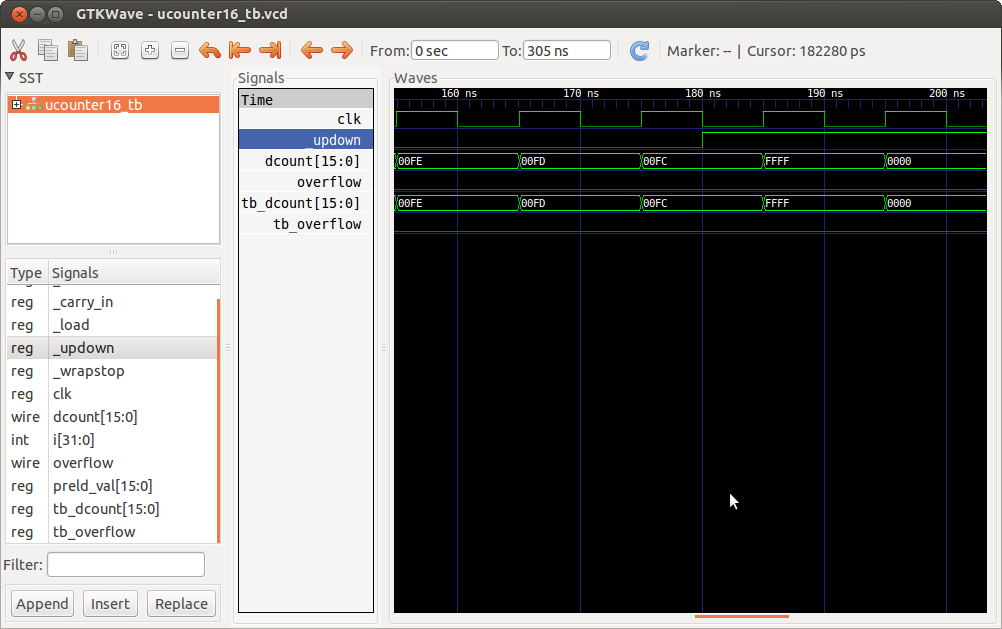
* Test 3. \_load and preld\_val



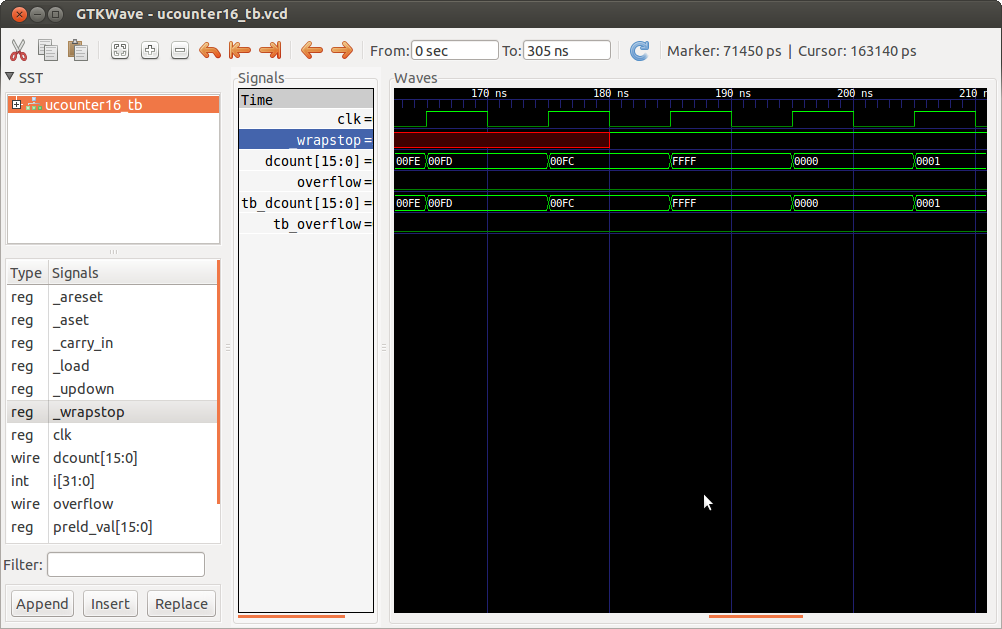
* Test 4. \_updown (up)



* Test 5. \_updown (down)



* Test 6. \_wrapstop (cycle)



* Test 7. \_wrapstop (stop) and overflow

