**Checklist**

Please put “” in the checkbox after you have checked your homework **DO Follow** each item in the checklists.

**Simulation environment**

|  |  |
| --- | --- |
|  | Run simulation **at SOC LAB** before you submit your homework. |

**Top module checklist**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Checkbox** | **Specifications** | | | | |
| **Name** | **I/O** | **Bit width** | | **Function explanation** |
|  | **For system signal** | | | | |
| clk | input | 1 | system clock | |
| rst | input | 1 | system reset | |
| system\_enable | input | 1 | system enable | |
|  | **connect with IM** | | | | |
| instruction | input | 32 | IM data output | |
| IM\_read | output | 1 | Enable IM read | |
| IM\_write | output | 1 | Enable IM write | |
| IM\_enable | output | 1 | Enable IM | |
| IM\_in | output | 32 | IM data input | |
| IM\_address | output | 10 | IM address input | |
|  | **connect with DM** | | | | |
| DM\_out | input | 32 | DM data output | |
| DM\_read | output | 1 | Enable DM read | |
| DM\_write | output | 1 | Enable DM write | |
| DM\_enable | output | 1 | Enable DM | |
| DM\_in | output | 32 | DM data input | |
| DM\_address | output | 15 | DM address input | |
|  | **for performance counter** | | | | |
| cycle\_cnt | output | 128 | Counter cycle count output | |
| ins\_cnt | output | 64 | Counter instruction count output | |
| load\_stall\_cnt | output | 64 | Counter load stall output | |
| branch\_stall\_cnt | output | 64 | Counter branch stall output | |
|  | **connect with External Memory** | | | | |
| MEM\_data | input | 32 | External memory data output | |
| MEM\_en | output | 1 | Enable external memory | |
| MEM\_read | output | 1 | Enable external memory read | |
| MEM\_write | output | 1 | Enable external memory write | |
| MEM\_in | output | 32 | External memory data input | |
| MEM\_address | output | 16 | External memory address input | |
|  | **connect with ROM** | | | | |
| rom\_out | input | 36 | ROM data output | |
| rom\_enable | output | 1 | Enable ROM | |
| rom\_address | output | 8 | ROM address input | |
|  | **I/O interrupt** | | | | |
| IO\_interrupt | input | 1 | For external interrupt  signal input | |

**Memory module checklist**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Module Type** | | **Specifications** | | | |
|  | **Instruction Memory** | **Module Name** | | | |
| **IM** (and declare as “**IM IM1(…)**” in your testbench) | | | |
| **Port Name** | **I/O** | **Bit width** | **Function explanation** |
| instruction | output | 32 | IM data output |
| clk | input | 1 | clock |
| rst | input | 1 | reset  (active high) |
| IM\_read | input | 1 | Enable IM read  (1:enable , 0:disable) |
| IM\_write | input | 1 | Enable IM write  (1:enable , 0:disable) |
| IM\_enable | input | 1 | Enable IM  (1:enable , 0:disable) |
| IM\_in | input | 32 | IM data input |
| IM\_address | input | 10 | IM address input |
|  | **Data Memory** | **Module Name** | | | |
| **DM** (and declare as “**DM DM1(…)**” in your testbench)  and in DM module, the register is named as **DM\_REG** | | | |
| **Port Name** | **I/O** | **Bit width** | **Function explanation** |
| DM\_out | output | 32 | DM data output |
| clk | input | 1 | clock |
| rst | input | 1 | reset  (active high) |
| DM\_read | input | 1 | Enable DM read  (1:enable , 0:disable) |
| DM\_write | input | 1 | Enable DM write  (1:enable , 0:disable) |
| DM\_enable | input | 1 | Enable DM  (1:enable , 0:disable) |
| DM\_in | input | 32 | DM data input |
| DM\_address | output | 15 | DM address input |
|  | **External Memory** | **Module Name** | | | |
| **EM** (and declare as “**EM EM1(…)**” in your testbench)  and in DM module, the register is named as **EM\_REG** | | | |
| **Port Name** | **I/O** | **Bit width** | **Function explanation** |
| MEM\_data | output | 32 | External memory data output |
| clk | input | 1 | clock |
| rst | input | 1 | reset  (active high) |
| MEM\_en | input | 1 | Enable external memory  (1:enable , 0:disable) |
| MEM\_read | input | 1 | Enable external memory read  (1:enable , 0:disable) |
| MEM\_write | input | 1 | Enable external memory write  (1:enable , 0:disable) |
| MEM\_in | output | 32 | External memory data input |
| MEM\_address | input | 16 | External memory address input |
|  | **ROM** | **Module Name** | | | |
| **ROM** (and declare as “**ROM ROM1(…)**” in your testbench)  and in DM module, the register is named as **ROM\_REG** | | | |
| **Port Name** | **I/O** | **Bit width** | **Function explanation** |
| rom\_out | output | 36 | ROM data output |
| clk | input | 1 | clock |
| rom\_enable | input | 1 | Enable ROM  (1:enable , 0:disable) |
| rom\_address | input | 8 | ROM address input |

**File hierarchy for homework checklist**

|  |  |
| --- | --- |
| **Checkbox** | **Folders & Files** |
|  | Root folder name : “n2601XXXX” |
|  | P1 folder name : “P1” ,  and all needed files described in Appendix A have been included in “P1” |
|  | AHB folder name : “AHB” ,  and all needed files described in Appendix A have been included in “AHB”  (This folder is for bonus) |
|  | Report document name : “n2601XXXX.doc” |
|  | SubmissionCheckList.doc |