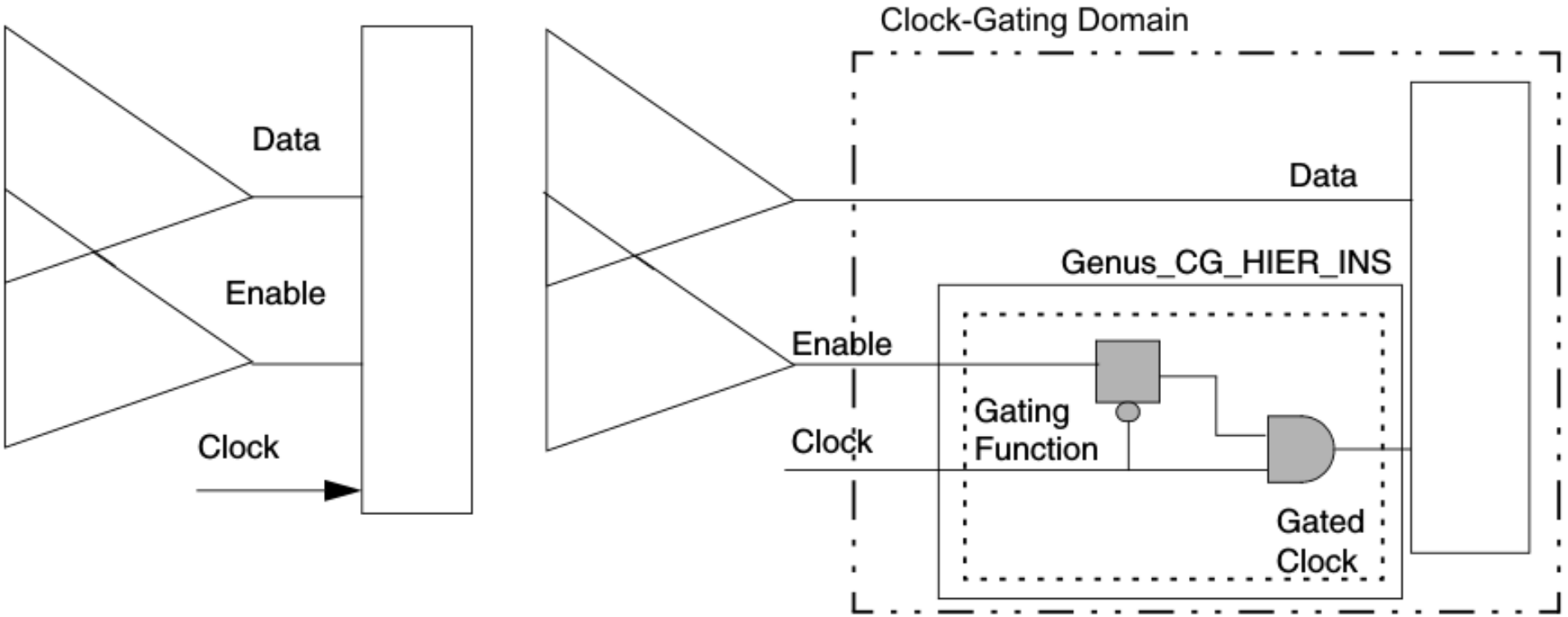
syn_generic

- Optimization of datapath components (adders, multipliers, shifters, etc.) to meet the required performance goal
- Using enable conditions in the fanin of registers to implement clock-gating logic and thus reducing power
- Stops the clocks for individual blocks when those blocks are inactive --> disabling functionality of those blocks.


Data
Enable
Clock
Clock-Gating Domain
Data
Genus_CG_HIER_INS
Enable
Clock
Gating
Function
Gated
Clock

Commands

- Start from Pg 106 of Synthesis Low power guide
- set_attribute lp_insert_clock_gating true
- set_attribute leakage_power_effort medium #before the elaborate command
- set_attribute lp_clock_gating_exceptions_aware true --> if multiple flip-flops have different types of clock gating requirements
- Syn_opt -incr --> optimises and generates reports in increments
- report_clock_gating -gated_ff > reports/clk-gatingtiming.txt
- Check power after optimisation using report_power
- gui_show to see the clock gated instance

Example

- Try this optimisation on an FSM design or any other sequential design with flip-flops in the middle of the data path