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A Low Pseudo-NMOS Based 4:2 Compressor Design

A MINOR PROJECT - IV REPORT

Submitted by

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BONAFIDE CERTIFICATE

Certified that this **18ECP105L - Minor Project IV** report **"A LOW POWER PSEUDO-NMOS BASED 4:2 COMPRESSOR DESIGN"** is the bonafide work of "MONISHA (927621BEC129), POOJASHREE M(927621BEC146), SASIREKHA T(927621BEC189), SATHIYADHARSHINI S(927621BEC190)" who carried out the project work under my supervision in the academic year **2023- 2024 – EVEN** Semester.

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Abstract	**Matching with POs, PSOs**
4:2 compressor, CMOS,Power,XOR-XNOR,Approximate computing.	PO1,PO2,PO3,PO4,PO5,PO7,PO8,PO12, PSO1,PSO2

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ABSTRACT

In VLSI circuits and systems, the compressor is a crucial component that is mainly used as a central processing unit. XOR-XNOR and multiplexer modules are used in this study's attempt to create a 4-2 compressor. The compressor's performance is analyzed in detail and is implemented and simulated using Synopsys tools with 90 nm CMOS technology. Important parameters are carefully calculated to verify its effectiveness, including average power dissipation and current ratings. A thorough performance comparison with current compressors is also carried out. Based on simulations conducted using 90nm CMOS technology, the results highlight the suggested compressor's impressive achievement of demonstrating drastically reduced power usage. Specifically, we include n-MOS pseudo logic in this work to achieve even lower power consumption, which improves overall efficiency across a range of VLSI applications.

Keywords: 4:2 compressor, CMOS, power, XOR-XNOR, Approximatecomputing.

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LIST OF ABBREVIATIONS

ACRONYM		ABBREVIATION
VLSI	-	Very large-scale Integration
NMOS	-	N-channel metal -oxide semiconductor
CMOS	-	Complementary metal-oxide semiconductor
LT SPICE	-	Linear Technologies Simulation Program with Integrated Circuit Emphasis
MSI	-	Medium-Scale Integration
LSI	-	Large-Scale Integration
EDA	-	Electronic Design Automation
SSI	-	Small-Scale Integration
ACG	-	Approximate Computing
WM	-	Wallace Multiplier
ACs	-	Approximate Compressors
PDAP	-	Power-Delay-Area-Product

CHAPTER 1

INTRODUCTION

1.1. Emerging of VLSI Technology

Very-Large-Scale Integration (VLSI) technology creates integrated circuits by integrating dozens to millions of transistors onto a single chip, transforming the electronics industry. It progressed from Small-Scale Integration (SSI) in the 1960s to Medium-Scale Integration (MSI) and Large-Scale Integration (LSI) in the 1970s. VLSI, which emerged in the late 1970s and early 1980s, made substantial advances in photolithography, fabrication techniques, and reliable semiconductor materials such as silicon. VLSI development was fueled by advancements in semiconductor production, materials, and Electronic Design Automation (EDA) tools, as well as an increasing demand for small, efficient electronics. VLSI technology facilitated the development of powerful microprocessors, advanced memory chips, and sophisticated consumer devices such as smartphones and tablets. It also upgraded telecommunications infrastructure, which is critical in modern

1.2. Importance of Digital circuits

A digital circuit is a type of circuit that uses several logic gates. Logic gates are usedto distinguish between different power signals. It can be used to send power signalsto various areas of an electronic device via gates. This will help to generate an outputsignal that is proportionate to the energy level of the input signals. The majority of these circuits consist of analog components. Their design is more sophisticated thanthat of analog circuits.

Digital circuits can be created with the numerous components that are commonly utilized in the circuit. We've illustrated a simple circuit with a few crucial components. The circuit below includes a diode, a resistor, an inductor, a

capacitor, and a power supply. Digital Circuit Design of Compressor is shown in Fig1.1.

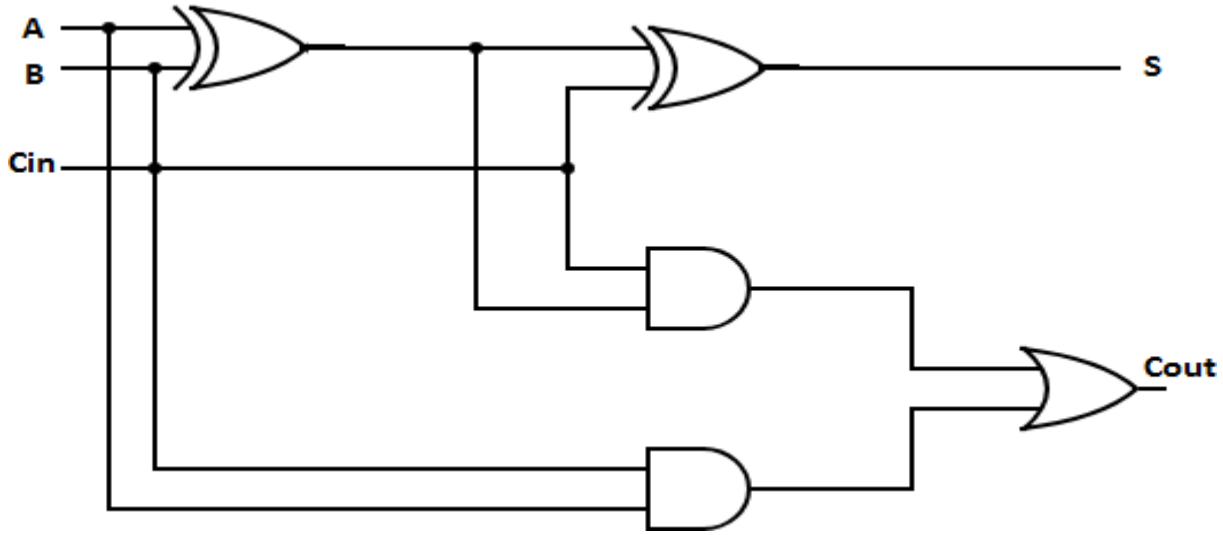

Fig .1.1 Digital Circuit Design of Compressor

The full-adder circuit shown below can be used to add the circuit's bits. To obtain the result, the circuit applies a boolean operation to the input bits. The circuit contains two XOR gates, two AND gates, and one OR gate.

1.3. Basics of Compressor

One of the major speed enhancement techniques used in modern digital circuits is the ability to add numbers with minimal carry propagation. The basic idea is that three numbers can be reduced to 2, in a 3:2 compressor, by doing the addition while keeping the carries and the sum separate.

This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs. The sum and carry can be recombined

normal addition to form the correct result. This process may seem more complicated and pointless, but the power of this technique is that any amount, number of additions can be added together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressors is also known as full adder. It adds three one bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is fromthe carry output from the cascade circuit. Carry output from full adder is fed to another full adder.

1.3.1. 4:2 compressor

A compressor is a device which is mostly used in multipliers to reduce the operandswhile adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder. It has Three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two Cascaded 3-2 compressor circuits. The conventional implementation of a 4-2 compressor is composed of two serially connected full adders. Different structures of 4-2 compressors are reported in literature and these are governing by the basic equation as shown in fig. 1.2.

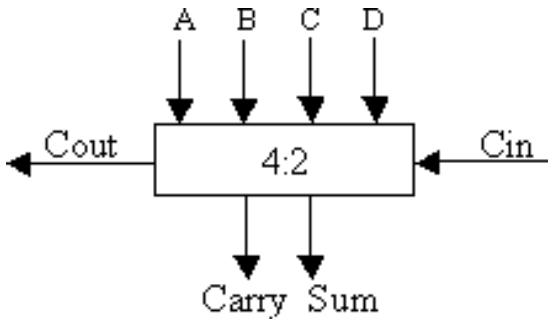

Fig.1.2. Block Diagram Of 4-2 compressor

One of the major speed enhancement techniques used in modern digital circuits is the ability to add numbers with minimal carry propagation. The basic idea is that three numbers can be reduced to 2, in a 3:2 compressor, by doing the addition while keeping the carries and the sum separate. This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs. The sum and carry can be recombined in a normal addition to form the correct result. This process may seem more complicated and pointless, but the power of this technique is that any amount, number of additions can beaded together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressor is also known as full adder. It adds three one bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is from the carry output from the cascade circuit. Carry output from full adder is fed to another full adder. The characteristics of the 4:2 compressors are:

- The outputs represent the sum of the five inputs, so it is really a 5 bit adder
- Both carries are of equal weighting (i.e. add "1" to the next column)
- To avoid carry propagation, the value of Cout depends only on A, B, C and D.It is independent of Cin.
- The Cout signal forms the input to the Cin of a 4:2 of the next column.

1.4 Objective

- The main objective is to design and implement a low-power 4:2 compressorusing pseudo-NMOS logic. This compressor will efficiently compress four inputbits into two output bits while prioritizing power efficiency.

- The ultimate aim is to provide an energy-efficient solution suitable for integration into modern VLSI technologies, thereby contributing to the development of more power-efficient digital circuits.

1.5. Organization of Report

The report is organized as follows,

Chapter 2: Literature Survey

This chapter provides a comprehensive review of existing literature related to the topic. It explores previous research findings, theoretical frameworks, and key concepts that form the foundation for the study.

Chapter 3: Existing Methodology

This chapter discusses the methodologies currently used in the field. It examines the techniques, tools, and processes that have been employed in previous studies, highlighting their strengths and weaknesses.

Chapter 4: Problem Identification

This chapter identifies the specific problem addressed by the study. It outlines the gaps in existing research and the challenges that need to be overcome, providing a clear justification for the proposed research.

Chapter 5: Proposed Method

This chapter presents the method proposed to address the identified problem. It details the research design, including the techniques and procedures that will be used to collect and analyze data, and explains why this method is expected to be effective.

Chapter 6: Implementation and Results

This chapter describes the implementation of the proposed method and presents the results obtained. It includes a detailed account of the data collection process, analysis, and interpretation of the findings, and discusses the implications of the results.

Chapter 7: Conclusion

This chapter summarizes the main findings of the study and their significance. It reflects on the research objectives, discusses the limitations of the study, and suggests directions for future research.

CHAPTER -2

LITERATURE REVIEW

2.1. Design and Implementation of Low power FinFET based Compressor [1]

Author Name: V. Siva Nagaraju; P. Ashok babu; B. Sadgurbabu; RajeevRatna Vallabhuni (2021)

Compressors are the essential supplements of Full adders and half adder in any multiplier design. Compressors play a vital role in reducing delay and increasing the overall performance of a multiplier. In this paper, various compressors such as 5:3, 10:4, 15:4 and 20:5 are designed and implemented in Cadence virtuoso tool at 180nm technology. Later on, the compressor was designed using FinFET technology. The designs in both technologies were simulated, and their performance was compared. Simulation analysis depicts that the compressor designed in FinFET technology will show less power consumption than CMOS technology.

2.2. Asic design of low power VLSI architecture for different multiplier algorithms using compressors [2]

Author Name: R. Abhilash; Sanjay Dubey; M. C. Chinnaaiah (2016)

In most of the digital systems, adders and multipliers are the fundamental components in the design of many applications domains such as a digital signal processing especially for multimedia application such as graphics 3D depends on extensive number of multiplication, scientific and numerical applications. This paper proposes a novel Compressors for low power VLSI architecture of different multiplier Algorithms and their ASIC design. Purely combinational logic is used in the design of these multipliers. The partial product bits are obtained by ANDing of both multiplier and multiplicand bit. Then the partial Products are summed using

compressor technique. In this paper the proposed novel 4-2 and 5-2 compressors architecture achieve low energy consumption, when used for different multipliers. All the proposed architectures are designed using Verilog HDL and are simulated using Xilinx tool for functionality verification. The physical verification is also done using the 180nm tsmc technology library, operating in slow (balanced-tree) conditions generated by Encounter (R) compiler. In particular, the results were compared with conventional multiplier algorithms and found that the proposed compressors when used in multiplier algorithms are more efficient in terms of power.

2.3. 4-2 Compressor Design with New XOR-XNOR Module [3]

Author Name: Sanjeev Kumar; Manoj Kumar (2014)

In this method, a low-power high speed 4-2 compressor circuit is proposed for fast digital arithmetic integrated circuits. The 4-2 compressor has been widely employed for multiplier realizations. Based on a new exclusive OR (XOR) and exclusive NOR (XNOR) module, a 4-2 compressor circuit has been designed. Proposed circuit shows power consumption variation in the range of 718.72 pW to 3357.40 pW. Maximum output delay of the circuit presents variation in the range of 43.83 ps to 27.74 ps. Further, power-delay product (PDP) of circuit is varying from 315.01×10-22(J) to 931.34×10-22(J) with change in supply voltage from 1.8V to 3.3V. Power consumption, delay and PDP of proposed 4-2 compressor circuit have been compared with earlier reported circuits and proposed circuit is proven to have the minimum power consumption and the lowest delay. Simulations have been performed by using SPICE based on TSMC 0.18μm CMOS technology.

2.4. Low power VLSI compressors(2013)[4]

Author Name: V Anandi; R Rangarajan (2013)

Present a new design for a 1-bit full adder featuring hybrid-CMOS design style. Our approach achieves low-energy operations in 180nm technology. The proposed new SERF- full adder (FA) circuit optimized for ultra low power operation is based on modified XNOR gates with clock gating to minimize the power consumption. And also generates full-swing outputs simultaneously. During our simulations, we arrived at the conclusion that many of the previously reported adders suffered from the problems of low swing and high noise when operated at low supply voltages. Compressor using blockwise power shut down technique is implemented. Simulated results using 180nm CMOS technology are provided. The 32×32 bit MAC unit using proposed full adder without block wise shut down technique produced a power saving of 24.27% over 32 bit MAC designedusing SERF full adder and 35.07% power savings over 32 bit MAC designed usingconventional 28T full adder.

2.5. Redesigned CMOS (4: 2) compressor for fast binary multipliers [5]

Author Name:Abdoreza Pishvaie; Ghassem Jaberipur; Ali Jahanian (2013)

(4: 2) compressors seem to be the most popular bit-compressing cells with principal application in multi-operand addition and multiplication hardware. Therefore, performance of (4: 2) compressors is particularly influential in the efficiency of multiplication intensive computations. Realization of these cells is mainly based on XOR/XNOR gates, which are functionally equivalent to three simpler ones among AND/NAND and OR/NOR gates. Decomposition of XOR/XNOR gates in some (4: 2) compressors to their constituent simpler ones may lead to removal of some hardware redundancy. In this paper we take advantage of such decomposition to propose a new (4: 2) compressor design, evaluate its

performance, and compare it with previous designs. The proposed (4: 2) compressor, as such, and those of reference works are simulated with HSPICE using 45nm post-layout CCMOS standard cell library with presence of process variation. The results show performance improvements, compared to the best of reference designs, in terms of delay (17%), power (13%), and power-delay-product (30%). For more realistic comparison, performance of each design is evaluated via incorporation of more than 1300 (4; 2) compressors in 54×54-bit binary multipliers as a uniform test bench via MAGMA tools. This experience confirmed the above results on isolated single (4; 2) compressors.

2.6. Design of a multiplier with low power data-compressors [6]

Author Name: Minkyu Song (1995)

A parallel structured 54/spl times/54 bit multiplier with low power data compressors is proposed. Using a tally-function circuit, an optimized low power data compressor is designed. The average power consumption of the proposed data compressor is reduced by about 35%, compared with that of the conventional multiplier; while the propagation delay is nearly same as that of the conventional one.

2.7. Successive Approximation Compressor for Efficient FIR Filters in C-MOS VLSI Design [7]

Author Name: M. S. S. Brundana; P.S.R. Rajeswari; N. Sravani; Sanjeev Kumar (2021)

In this method, a successive approximately compressor based techniques have beenanalysed. The audio signals have been captured without compressing the signal to noise ratios to help increase the area and the energy savings in low-powered circuitsby approximately computing with an energy reduction area of 15.5%. The dual-quality

compressor delivers high speed and low power consumption at the cost of low accuracy. We contract with ripple carry adders, which are part of cutting edge, generated totally in CMOS, and later refer to the true application of the identical, as opposed to estimates.

2.8. A Systematic Comparison of Approximate 4-2 Compressors forEfficient Approximate Multipliers [8]

Author Name: E. Jagadeeswara Rao; P. Samundiswary (2022)

In a Digital Signal Processing (DSP) system, the multiplier is an essential element. It had given the large design parameters values in DSP systems, and hence efficient multipliers are now in high demand. Approximate Computing (ACG) has been used in exact multiplier design by lowering design parameter values. This paper, first, reviews the eighteen recent proposed 4-2 Approximate Compressors (ACs). Next, develop the Verilog code of eighteen 4-2 ACs and 8-bit Wallace Multiplier (WM) with these 4-2 ACs. Next, these 4-2 ACs and WM were then simulated and synthesized by Cadence RTL Compiler in a 90 nm CMOS standard library file. The results reveal that Liu2 provided the best design parameter values compared to WM with the remaining 4-2 ACs.

2.9. Area Efficient Approximate 4–2 Compressor and Probability-Based Error Adjustment for Approximate Multiplier [9]

Author Name: Mingtao Zhang; Shinichi Nishizawa; Shinji Kimura (2023)

Many multipliers based on approximate compressors have been developed for error-tolerant applications such as image processing to reduce power, but the combination of them has not been fully studied. This brief proposes a novel 4 gate 4–2 approximate compressor which is complementary with other compressors from earlier work and constructs a hybrid multiplier based on the compressors, a constant approximation, and error correction AND gate. According to the simulation results, the proposed hybrid approximate multiplier has excellent accuracy and electrical

performance tradeoff and reduces the power-delay-area product (PDAP) by 66% with an MRED of 2.5% when compared to the exact multiplier.

2.10. Low-power low-voltage 4-2 compressors for VLSI applications [10]

Author Name: M. Margala; N.G. Durdle (1999)

This method presents new 4-2 compressor architectures, a full-swing bipolar double pass-transistor 4-2 compressor, a new full-swing BiNMOS 4-2 compressor, a reduced-swing bipolar double pass-transistor 4-2 compressor and a reduced-swing double pass-transistor BiNMOS 4-2 compressor, that outperform a standard CMOS 4-2 compressor up to 3 times in power-efficiency at supply voltages 1.5 V-3 V. The bipolar double pass-transistor 4-2 compressor is more power-efficient than a standard CMOS 4-2 compressor even at a fanout of 1. All remaining proposed 4-2 compressors have a lower crossover capacitance with a standard CMOS 4-2 compressor than previously reported low-power 4-2 compressors. Circuits were designed and fabricated in 0.8 /spl mu/m BiCMOS technology.

2.11. SUMMARY

The literature survey encompasses various advanced techniques and designs aimed at optimizing compressor circuits for multipliers, which are critical components in digital arithmetic operations. The reviewed works highlight several approaches to enhancing the performance of compressors, including the use of FinFET technology, novel low power VLSI architectures, and innovative XOR-XNOR modules. Otherstudies focus on hybrid-CMOS designs, redesigned CMOS compressors for binarymultipliers, and optimized low power data compressors for parallel multipliers. Moreover, recent advancements include successive approximation compressors forFIR filters, systematic comparisons of approximate compressors for multipliers,

and novel combinations of approximate compressors to improve accuracy and efficiency. Additionally, low-power low-voltage compressor architectures have been explored to enhance power efficiency.

Despite significant advancements, existing designs often face challenges such as high power consumption, increased delay, and complex circuit implementations. The drawbacks of these existing methods underline the need for a more efficient solution. The proposed method, a low power Pseudo-NMOS based 4:2 compressor design, aims to address these issues by offering a simplified design with reduced power consumption and delay, thereby enhancing the overall performance of multipliers.

CHAPTER 3

EXISTING METHODOLOGY

3.1. Introduction

Multipliers are essential components of digital arithmetic circuits, particularly for applications that need high computing capacity like multimedia, digital signal processing (DSP), and image processing. Compressor utilization has grown in popularity as a means of improving these multipliers' efficiency. In order to improve speed and lower power consumption in multipliers, compressors are essential for lowering the number of partial products in the multiplier. Approximate computing has become popular recently as a way to further improve efficiency by accepting small errors in return for large power, latency, and area savings.

The construction of a unique 4-2 approximation compressor is investigated in the work "Area Efficient Approximate 4-2 Compressor and Probability-Based Error Adjustment for Approximate Multiplier" by Mingtao Zhang, Shinichi Nishizawa, and Shinji Kimura shown in fig3.1. This architecture is specifically intended for error-tolerant applications, where little errors may be tolerated, such image processing. The suggested compressor is a component of a hybrid multiplier design, which strikesa fair balance between efficiency and accuracy by combining approximation compressors with error correcting techniques. According to simulation studies, this hybrid multiplier, when compared to an exact multiplier, dramatically reducesthe power-delay-area product (PDAP) by 66% while keeping the mean relative error distance (MRED) at 2.5%.

3.2 Existing 4-2 Compressor

The compressor design consists of two NOR gates, one OR gate, and one XOR gate. It uses less transistors and has a probability of six faults out of sixteen input patterns, making it more competitive is shown in Fig.3.1.

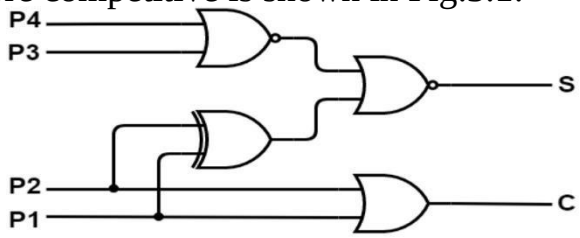

Fig.3.1. Circuit diagram of the Existing 4-2 Compressor

If we compel the erroneous output to occur at specific input characteristics, we can remedy compressor errors with a simple logic gate. The method can be extended to scenarios with more than four faults of the total sixteen input patterns. A new area efficient 4-2 compressor is designed in an effort to make the sum of S (sum) and C (carry) as close to the exact result as possible and to improve the regularity of the Karnaugh map. Table 3.1 shows the truth table of the existing compressor's outputs Sand C.

Table 3.1 Truth table of 4-2 Compressor

Input p1-p4	***Prob.***	***C S***	***E***
0000	81/256	00	
0001	27/256	01	
0010	27/256	01	
0011	9/256	01	-1
0100	27/256	10	+1
0101	9/256	10	
0110	9/256	10	
0111	3/256	10	-1
1000	27/356	10	+1
1001	9/256	10	
1010	9/256	10	
1011	3/256	10	-1
1100	9/256	10	
1101	3/256	11	
1110	3/256	11	
1111	1/256	11	-1

According to De Morgan's laws, the expression of C (Eqn.(3.1)) and S (Eqn.(3.2)) under the assumption of using the fewest number of logic gates possible. It is worth noting that, NAND and NOR gates have better performance than AND and OR gates.

$$C = a1 + a2 \tag{3.1}$$

$$S = (a1 \cdot a2 + a1 \cdot a2)(a3 + a4)$$
$$= (a1 \oplus a2) + (a3 + a4) \tag{3.2}$$

3.3. Challenges in Existing Method

Existing approaches confront a number of obstacles, including high power consumption and the difficulty of attaining low delay while preserving power and space efficiency. Traditional compressor designs are complex, which increases development time and costs. Furthermore, addressing errors caused by approximate computing is difficult, sometimes resulting in performance deterioration in precision-critical applications such as image processing. Finding a balance between accuracy and efficiency remains difficult, with current solutions sometimes trading one for the other. Finally, incorporating new compressor designs into old systems necessitates considerable changes and testing, making the process both resource-intensive and time-consuming.

CHAPTER 4

PROBLEM IDENTIFICATION

In digital signal processing and computational applications, multipliers are critical to overall system performance, relying on compressor circuits to increase speed andefficiency. However, present compressor designs have several major flaws that limittheir effectiveness. High power consumption is a big concern, especially for battery-powered and portable devices, because traditional compressors frequently require alot of power. Additionally, obtaining low delay while retaining power and area efficiency is difficult, resulting in trade-offs that limit performance. The intricacy of typical compressor circuits exacerbates these challenges, increasing developmenttimes and costs while complicating optimization efforts. Furthermore, error management in approximate computing is poor, resulting in performance deterioration in precision-critical applications. Another key problem is balancing accuracy and efficiency, as existing methods sometimes compromise one for the other.

Finally, incorporating new compressor designs into current digital systems necessitates significant adjustments and thorough testing, making the process both resource-intensive and time-consuming. Addressing these issues is critical for improving the performance and efficiency of digital multipliers, and the proposed low-power Pseudo-NMOS-based 4:2 compressor architecture intends to deliver a streamlined, power-efficient, and accurate solution that is easier to integrate and optimize.

CHAPTER 5

PROPOSED SYSTEM

5.1 Introduction-Pseudo NMOS

Pseudo-nMOS logic is used in the design of a low-power 4:2 compressor in a methodical manner to maximize the benefits of the technology while meeting the compressor's operational requirements. This procedure starts with a thorough understanding of compressor logic and moves on to the use of basic pseudo-nMOS gates such as NAND, NOR, and inverters. The compressor's intended logic functionality is then achieved by integrating these gates. One of the main goals of the design process is to minimize power consumption by careful transistor sizing, a reduction in the number of transistors, and a reduction in needless switching activity. Prior to planning and manufacture, simulation tools are essential for confirming functioning and power consumption. Post-layout simulations make sure that performance is not harmed by layout parasitics. The design is then rigorously tested and characterized to ensure that it meets predetermined standards. Iterative optimization is then carried out as needed to further improve performance or power efficiency. For future understanding and maintenance, thorough documenting of design decisions and optimizations is essential, with careful consideration of application-specific needs driving design choices. These gates are designed to minimize transistor count and optimize topologies for low power consumption, all while embodying the needed compressor functionality through logic synthesis. Subsequently, different power optimization strategies are used to further improve energy efficiency, including transistor size and gate restructure. The manufactured design is put through a

thorough testing and characterization process to confirm that it complies with the specifications. The design may then undergo iterative optimization, with adjustments made in response to simulation feedback and test results. Throughout the process, meticulous documentation is maintained, capturing design decisions, optimizations, and testing results. Consideration of application-specific requirements guides design choices, ensuring the final product aligns with the intended use case.

5.2 Proposed Pseudo-NMOS Based 4-2 Compressor

In pseudo NMOS logic, the pulldown network is constructed by NMOS, while an amalgamation of NMOS-PMOS transistors are employed in pull-up network. The general structure of the Pseuso-NMOS logic is shown in Fig. 5.1. By the comparison of Static and Pseudo NMOS circuits, it has more advantages in the elimination of input capacitance and area, because a N number of transistors in the Pull up network were eliminated and it have been replaced by a single PMOS transistor with ground input.

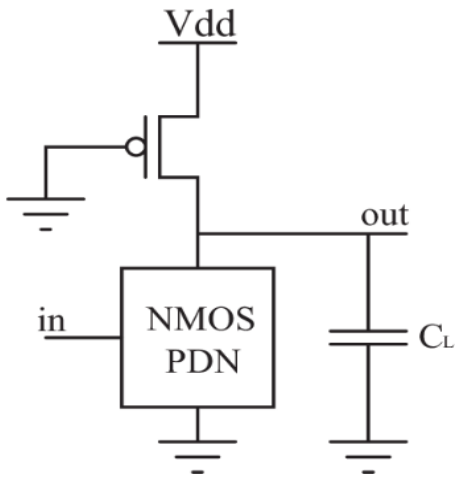

Fig. 5.1. General Structure of the Pseudo-NMOS logic

Here, Pseudo-NMOS logic is extended to design the NOR-XOR logic based 4-2 compressor. The pseudo-NMOS based NOR, OR and XOR circuits. The entire pullup network of the each gate will be replaced by single PMOS transistor.

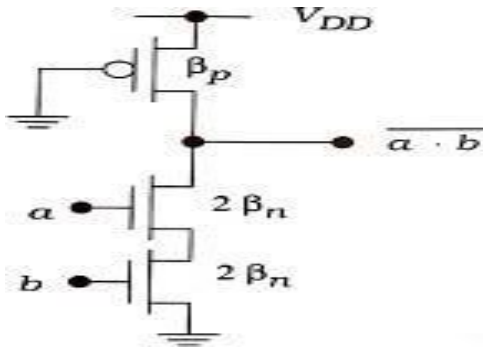

Fig. 5.2 Pseudo-NMOS based NOR-Gate

Here, Pseudo-NMOS logic is extended to design the NOR logic based 4-2 compressor shown in fig.5.2. The entire pull up network of the each gate will be replaced bysingle PMOS transistor.

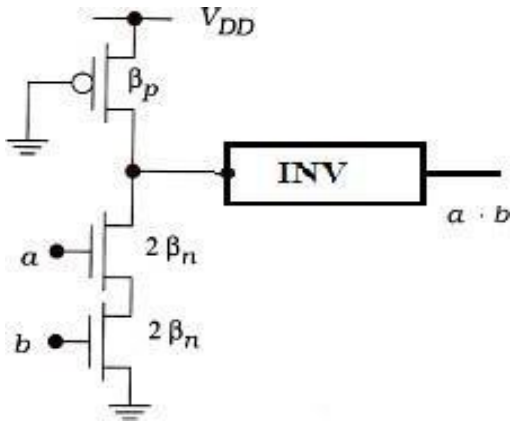

Fig. 5.3 Pseudo-NMOS based OR-Gate

Here, Pseudo-NMOS logic is extended to design the OR logic based 4-2 compressor shown in fig.5.3. The entire pull up network of the each gate will be replaced by single PMOS transistor.

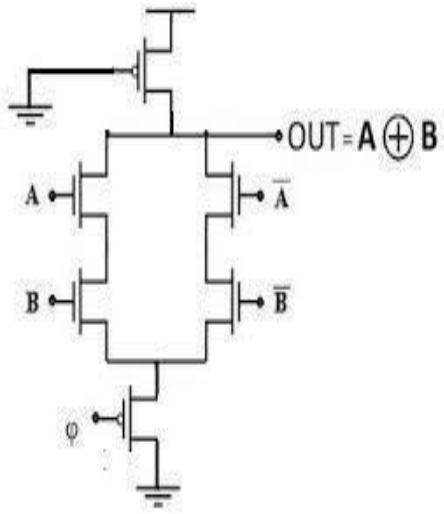

Fig. 5.4 Pseudo-NMOS based XOR-Gate

Here, Pseudo-NMOS logic is extended to design the XOR logic based 4-2 compressor shown in fig.5.4. The entire pull up network of the each gate will be replaced by singlePMOS transistor.

5.3 Advantages

The proposed low power Pseudo-NMOS based 4:2 compressor design offers several advantages over existing methods:

1. **Reduced Power Consumption**: By leveraging Pseudo-NMOS technology, the proposed compressor significantly lowers power consumption, making it ideal for battery-operated and portable devices.
2. **Lower Delay**: The design optimizes circuit paths to minimize delay, enhancing the speed of arithmetic operations, which is crucial for high-speed computing applications.
3. **Simplicity and Efficiency**: The Pseudo-NMOS design simplifies the circuit structure, reducing complexity and making it easier to implement and optimize compared to traditional designs.

4. **Enhanced Accuracy**: While maintaining low power and delay, the design includes mechanisms to manage and correct errors, ensuring high accuracy and reliability in applications that require precision, such as image processing.
5. **Balanced Tradeoff**: The proposed method effectively balances the tradeoff between accuracy and efficiency, providing substantial power and area savings without compromising on performance.
6. **Improved Integration**: The simpler design facilitates easier integration into existing digital systems, requiring fewer modifications and less extensive testing, thus saving development time and resources.

By addressing the primary challenges of existing methods, the proposed low power Pseudo-NMOS based 4:2 compressor design presents a robust solution for enhancing the efficiency and performance of digital multiplier

CHAPTER 6

IMPLEMENTATION RESULTS

6.1. Tool Description

LTspice® is a high-performance SPICE simulation software, schematic capture,and waveform viewer with features and models that make it easier to simulate analog circuits. The materials listed below are designed to help you get started with LTspice or execute more complex simulations.

LTspice is a free, powerful tool designed specifically for simulating analog electronic circuits. It combines three key functionalities in one software:

- **Schematic capture:** This lets you visually design your circuit using symbols for electronic components and wires to represent connections.
- **Simulation:** LTspice uses a powerful SPICE simulator to analyze the behavior of your circuit based on various electrical parameters. expand_more You can run different simulations like AC analysis (to see how the circuit behaves with varying frequencies), DC analysis (to find voltages and currents at specific points), transient analysis (to simulate the circuit's response over time), and more.
- **Waveform viewer:** After running simulations, LTspice presents the results in an easy-to-understand graphical format using waveforms. expand_more This helps you visualize how voltages and currents change within the circuit.

LTspice is particularly valuable because:

- **Free and unlimited:** Unlike many simulation tools, LTspice is completely free to use with no restrictions on circuit size or complexity.
- **Extensive library:** It comes with a large library of pre-built models for electronic components from various manufacturers, saving you time and effort in setting up simulations.
- **Fast and accurate:** LTspice is known for its speed and accuracy in circuit simulations.
- **Ease of use:** The user interface is relatively simple to learn, making it accessible to both beginners and experienced circuit designers.

Overall, LTspice is an excellent tool for anyone who works with analog electronics, from students to professional engineers.

6.2. Implementation of Existing Method

LTspice offers a powerful platform to simulate a standard 4-2 compressor circuit. Begin by capturing the schematic using LTspice's interface. Reference a published design featuring NMOS and PMOS transistors, resistors, and voltage sources. meticulously replicate the component connections in your LTspice schematic. Next, set up the simulation. Include a SPICE model file for the specific NMOS transistor used. Define voltage sources for the data inputs (A, B, Cin) and configure output analysis using probes on the Sum and Cout nodes. Choose the appropriate simulation type (e.g., transient analysis) and run the simulation after setting the time range.

Analyze the resulting waveformsto verify the compressor's functionality.

The Sum output should reflect the compressed data based on inputs and carry-in, while the Cout should represent the generated carry-out. Remember, this is a general guideline, and specific details might vary based on the chosen design variant.

6.3. Implementation of Proposed Method

To simulate this design, first locate a reference showcasing the transistor schematics for individual Pseudo-NMOS NOR, OR, and XOR gates (refer to Fig 5.2, Fig 5.3, and Fig 5.4 in the provided text for a general idea). Within LTspice, meticulously replicate these schematics using NMOS transistors, resistors, and a single PMOS transistor for the pull-up network in each gate. Next, interconnect these gates based on the reference design to form the complete 4-2 compressor circuit. Configure the simulation by including a SPICE model for the NMOS transistor and defining voltage sources for data inputs (A, B, Cin). Utilize probes on Sum and Cout nodes for output analysis. Choose a suitable simulation type (e.g., transient analysis) and set the time range. Run the simulation and analyze the resulting waveforms to verify the compressor's functionality. Remember, this is a general approach, and specific details might vary based on the chosen reference design. Comparison of Existing and Proposed Method is shown in Table 6.1.

6.4. Comparison

Table 6.1 Comparison of Existing and Proposed Method

Feature	**Existing 4-2 Compressor (Likely CMOS)**	**Proposed Pseudo-NMOS 4-2 Compressor (Conceptual)**
Transistor Type	Uses both NMOS and	Uses only NMOS

	PMOS transistors.	transistors for pull-down networks and a single PMOS transistor for the pull-up network in each gate.
Circuit Complexity	Generally more complex due to the requirement of both NMOS and PMOS transistors.	Potentially simpler design with fewer transistors overall.
Area Efficiency	Less area efficient due to additional PMOS transistors.	Potentially more area efficient due to the reduction in transistors.
Input Capacitance	Higher input capacitance due to the presence of PMOS transistors at the gate inputs.	Lower input capacitance because only NMOS transistors are used at the gate inputs.
Power Consumption	Potentially higher power consumption due to more transistors involved in the pull-up networks and PMOS leakage current.	Potentially lower power consumption due to fewer transistors and elimination of PMOS leakage current.
Speed	May offer faster switching speeds due to the characteristics of both NMOS and PMOS transistors.	Potentially slower switching speed compared to a fully CMOS design due to relying solely on NMOS transistors.
Implementation	Established design	Might require more

	principles and readily available components.	careful design and simulation to ensure functionality due to the unique characteristics of Pseudo-NMOS logic.

6.5. Experimental Results

The overall implementation of the existing and proposed compressor design is done in the LTSPICE simulation platform while keeping the channel length as 90nm. The schematic blocks involved in the proposed compressor are depicted in Fig. 6.1. The corresponding waveform of the S and C are depicted in simulation waveforms along with Power and Currrent rating Calculations.

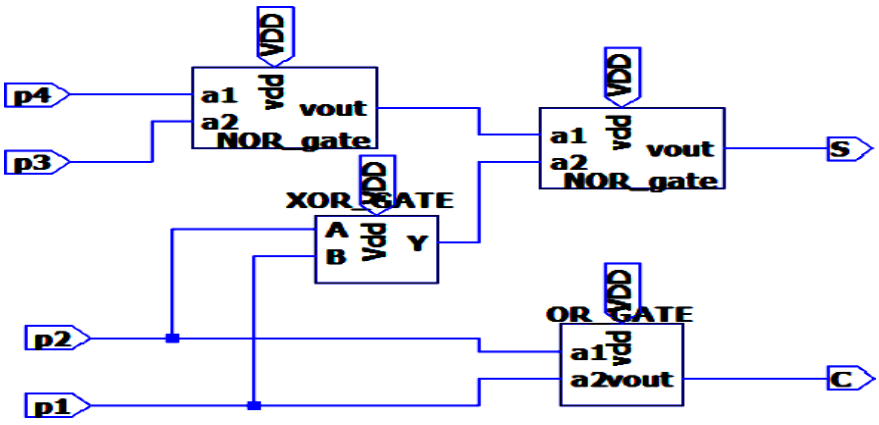

Fig.6.1 Schematic Block of the Proposed 4-2 compressor

A pseudo-NMOS 4:2 compressor architecture with low power consumption is depicted in the schematic block diagram. S imulation Waveform of the proposed 4-2 Compressor shown in Fig 6.2. Its main goal is to efficiently compress binary inputs while using less energy. The design uses pseudo-NMOS logic gatesto create partial products for each input bit, starting with four binary inputs (A[3:0]). Known for its low-power features, this logic uses less energy than conventional techniques. These partial products help to provide carry signals, which are essential for determining the sum output with accuracy. Partial products are combined to create the compressed binary output, which carries signals. Finally, two output lines (S[1:0]) display the compressed result. Energy efficiency is given first priority in this design, which makes it perfect for applications where power consumption is important. power Measurement of 4-2 compressor showns in Fig 6.3.

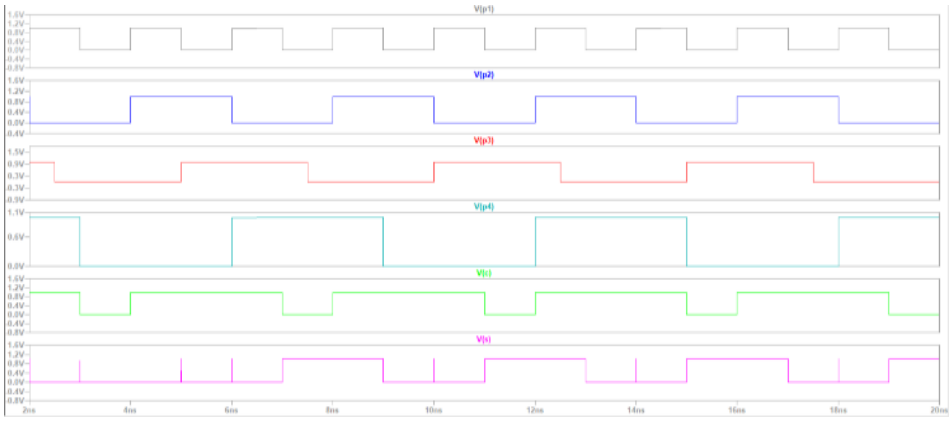

Fig. 6.2 Simulation Waveform of the Proposed 4-2 Compressor

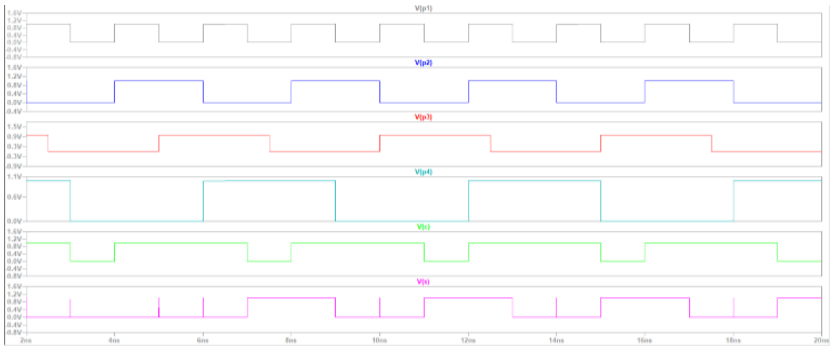

Fig 6.3 Power Measurement of 4-2 compressor

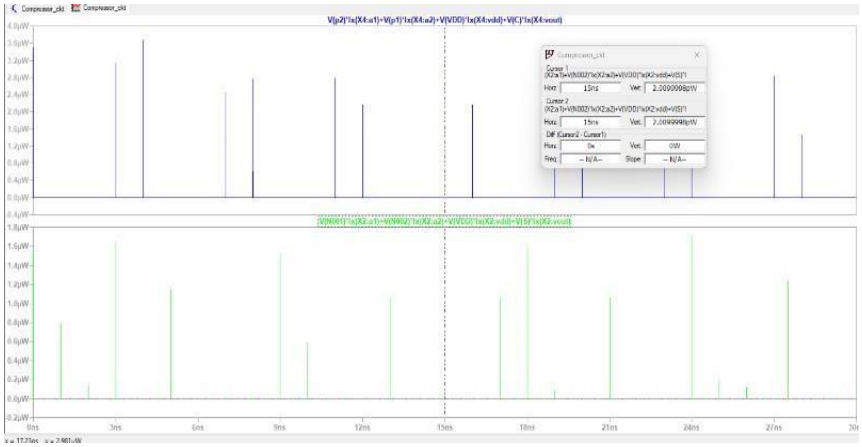

Fig. 6.4. Current Measurement of 4-2 Compressor

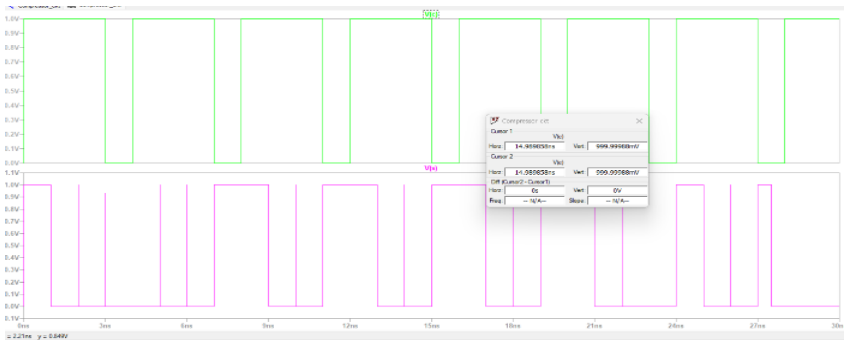

Fig.6.5 Power Measurement of the proposed 4-2 compressor

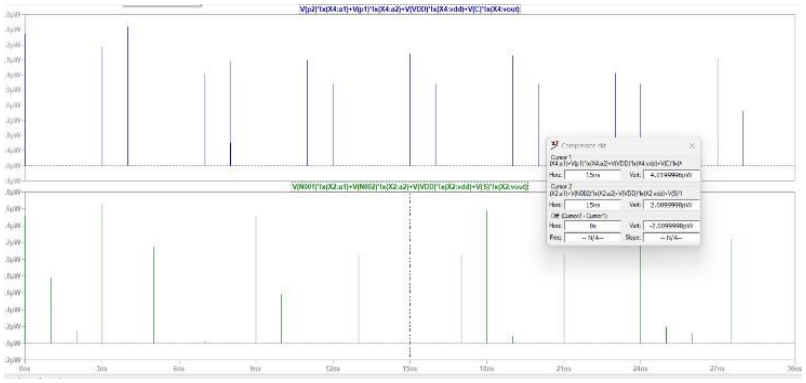

Fig.6.6 Current Measurement of the proposed 4-2 compressor

The performance of the low-power pseudo-NMOS 4:2 compressor architecture is examined in detail by the experimental results.current Measurement of 4-2 Compressor shows Fig 6.4. Initially, the power consumption is measured and compared to conventional designs. These outcomes demonstrate a notable decrease in power consumption, demonstrating the energy-saving efficacy of pseudo-NMOS logic.Power Measurement of the proposed 4-2 compressor shows Fig 6.5. Subsequently, the compressor's functionality is verified by contrasting its outputs with anticipated outcomes using various inputs. This guarantees the accuracy and dependability of the design. Current Measurement of the proposed 4-2 compressor shows Fig 6.6. They also examine performance indicators, such as efficiency and speed, demonstrating the benefits of the pseudo-NMOS technique.

CHAPTER 7

CONCLUSION

In conclusion, this study presents a novel approach to designing a low-power 4:2compressor utilizing XOR-XNOR and multiplexer modules. Through rigorous simulation using Synopsys tools and 90 nm CMOS technology, we have demonstrated the efficacy of our proposed compressor design. By meticulously computing key metrics such as average power dissipation and current ratings, we have validated its efficiency, showcasing notably reduced power consumption compared to existing compressors. Moreover, the integration of n-MOS pseudo logic further enhances power efficiency. This underscores the potential of our compressor design to significantly contribute to the advancement of low-power VLSI circuits and systems. Moving forward, our findings pave the way for future research aimed at exploring additional optimizations and applications of pseudo-NMOS based designs in the realm of VLSI technology.

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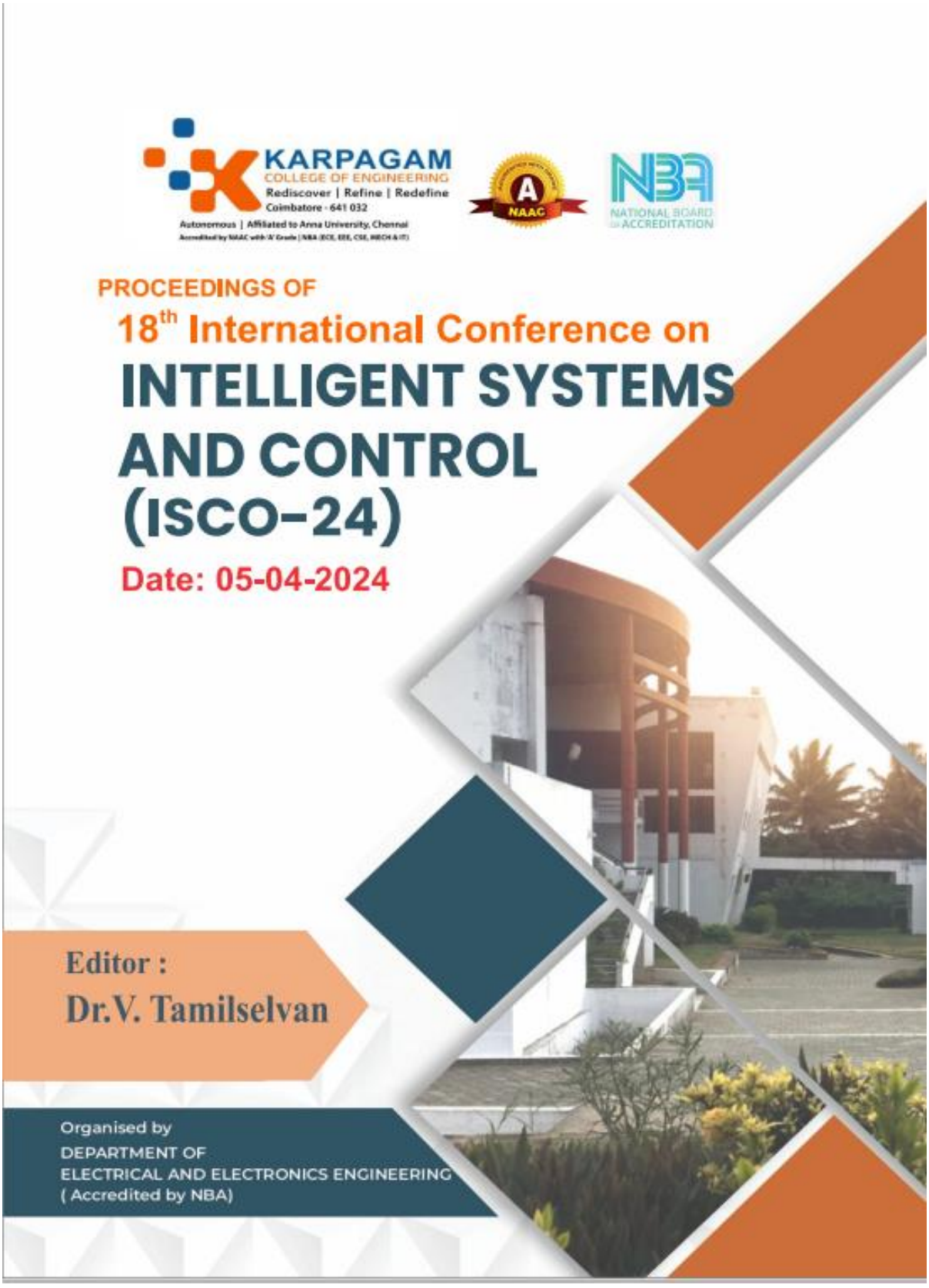

18th INTERNATIONAL CONFERENCE ON INTELLIGENT SYSTEMS AND CONTROL (ISCO 24)

Editor

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Dr. R. Vasanthakumar
Chairman and Managing Trustee, Karpagam Institutions

MESSAGE

It is with great pleasure and honor that I extend my warmest greetings to all of you gathered here for the International Conference on Intelligent System Control (ISCO24), hosted by Karpagam Institutions.

As the Chairman of Karpagam Institutions, I am delighted to welcome distinguished scholars, researchers, professionals, and students from around the world to this prestigious event. ISCO24 promises to be a forum for insightful discussions, knowledge exchange, and collaborative exploration of advancements in intelligent system control.

In today's rapidly evolving technological landscape, intelligent systems and control play a pivotal role in shaping our future. This conference provides a platform for us to engage in interdisciplinary dialogue, share innovative ideas, and foster partnerships that can drive progress and innovation in this critical field.

I would like to extend my sincere appreciation to the organizing committee, keynote speakers, session chairs, reviewers, and all those who have contributed to the success of ISCO24. Your dedication and hard work have been instrumental in making this conference possible.

As you participate in the various sessions, presentations, and networking opportunities throughout ISCO24, I encourage you to embrace the spirit of collaboration and exploration. Let us leverage this platform to inspire one another, push the boundaries of knowledge, and pave the way for a future enriched by intelligent system control technologies.

I wish you all a stimulating and fruitful experience at ISCO24. May your contributions and interactions during this conference lead to valuable insights, new discoveries, and lasting connections that will shape the future of intelligent system control.

Thank you for your participation and commitment to advancing the frontiers of science and technology.

Shri. K. Murugaiah

Chief Executive Officer, Karpagam Institutions

MESSAGE

At Karpagam Institutions, we recognize the critical role that intelligent system control plays in shaping the future of various industries and sectors. This conference provides a unique platform for us to explore the latest trends, discuss emerging technologies, and identify opportunities for collaboration and partnership.

I would like to express my sincere gratitude to the organizing committee, keynote speakers, session chairs, reviewers, and all those involved in organizing ISCO24. Your dedication and hard work have been instrumental in ensuring the success of this event.

As you participate in the conference sessions, presentations, and networking events, I encourage you to engage actively, share your expertise, and forge meaningful connections with your peers. Let us seize this opportunity to inspire innovation, drive progress, and create a lasting impact in the field of intelligent system control.

I wish you all a productive, enriching, and memorable experience at ISCO24. May the knowledge gained and relationships formed during this conference contribute to the advancement of intelligent system control and lead to breakthroughs that benefit society as a whole.

Dr. V. Kumar Chinnaiyan

Principal, Karpagam College of Engineering

MESSAGE

I am honored to welcome distinguished scholars, researchers, industry professionals, and students from around the world to this esteemed gathering. ISCO24 represents a significant opportunity for us to collectively explore and delve into the latest developments, challenges, and advancements in the dynamic field of intelligent system control.

This conference serves as a vital platform for fostering collaboration, sharing innovative ideas, and exchanging valuable insights that will contribute to the advancement of intelligent system control and its applications across various domains. The diverse perspectives and expertise gathered here today promise to enrich our understanding and drive innovation in this critical field.

I extend my heartfelt appreciation to the organizing committee, keynote speakers, session chairs, reviewers, and all those who have worked tirelessly to make ISCO24 a success. Your dedication and hard work are truly commendable and have been instrumental in shaping this conference into a forum of excellence and knowledge exchange.

As you participate in the engaging sessions, presentations, and discussions throughout ISCO24, I encourage you to embrace the spirit of collaboration, creativity, and curiosity. Let us seize this opportunity to ignite new ideas, forge meaningful connections, and inspire breakthroughs that will shape the future of intelligent system control.

I wish you all a productive, enlightening, and memorable experience at ISCO24. May your contributions and interactions during this conference lead to valuable insights, new discoveries, and lasting collaborations that will drive positive change in our world.

Thank you for your participation and commitment to advancing the frontiers of science and technology.

Dr. C. Kumar

Professor and Head, EEE Department, Karpagam College of Engineering

MESSAGE

On behalf of the Department of Electrical and Electronics Engineering (EEE) at Karpagam College of Engineering, it is my utmost pleasure to extend a warm welcome to all attendees of the International Conference on Intelligent System Control (ISCO24).

ISCO24 represents a significant milestone for our department as we come together to explore the latest advancements and innovations in intelligent system control. This conference serves as a platform for sharing cutting-edge research, fostering collaborations, and engaging in discussions that are essential for the progress of our field.

As the organizing department, we have worked diligently to curate a program that showcases the diverse perspectives and expertise within the realm of intelligent system control. We are honored to host esteemed scholars, researchers, industry professionals, and students from around the world, and we look forward to the fruitful exchange of ideas and insights that will take place during ISCO24.

I would like to express my sincere gratitude to the organizing committee, keynote speakers, session chairs, reviewers, and all those who have contributed to the success of ISCO24. Your dedication and hard work have been instrumental in shaping this conference into a platform of excellence and knowledge sharing.

As you participate in the various sessions, presentations, and networking opportunities throughout ISCO24, I encourage you to actively engage, ask questions, and share your expertise. Let us seize this opportunity to inspire one another, forge new collaborations, and pave the way for advancements in intelligent system control.

I wish you all a stimulating and enriching experience at ISCO24. May your contributions and interactions during this conference lead to valuable insights and innovations that will shape the future of our field.

PREFACE

International Conference on Intelligent System and Control (ISCO24) organized by the department of Electrical and Electronics Engineering, Karpagam College of Engineering, Coimbatore, Tamilnadu on 4th and 5th April, 2024.

The conference provides a platform to discuss recent trends in Electrical Energy, Soft Computing and Networks etc. with participants from all over the world, both from academic and industry. Its success is reflected in the papers received, with participants coming from several parts allowing a real multinational multicultural exchange of experiences and ideas.

Every submission has been peer reviewed by - reviewers in the right area and more than 6 submissions have been received with of them were accepted for final presentation, in which article abstracts will be published in conference proceedings and the selective article will be recommended to the UGC / SCOPUS journals.

This conference can only succeed as a team effort so the editors wish to thank the national and international advisory committee members and the reviewers for their excellent work in reviewing the papers as well as their invaluable inputs and advices.

Thanks also goes to the entire team of members from Department of Electrical and Electronics Engineering for their extensive support to ISCO24.

Dr. C. Kumar

On behalf of the Organizing Committees

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A LOW POWER PSEUDO-NMOS BASED 4-2 COMPRESSOR DESIGN

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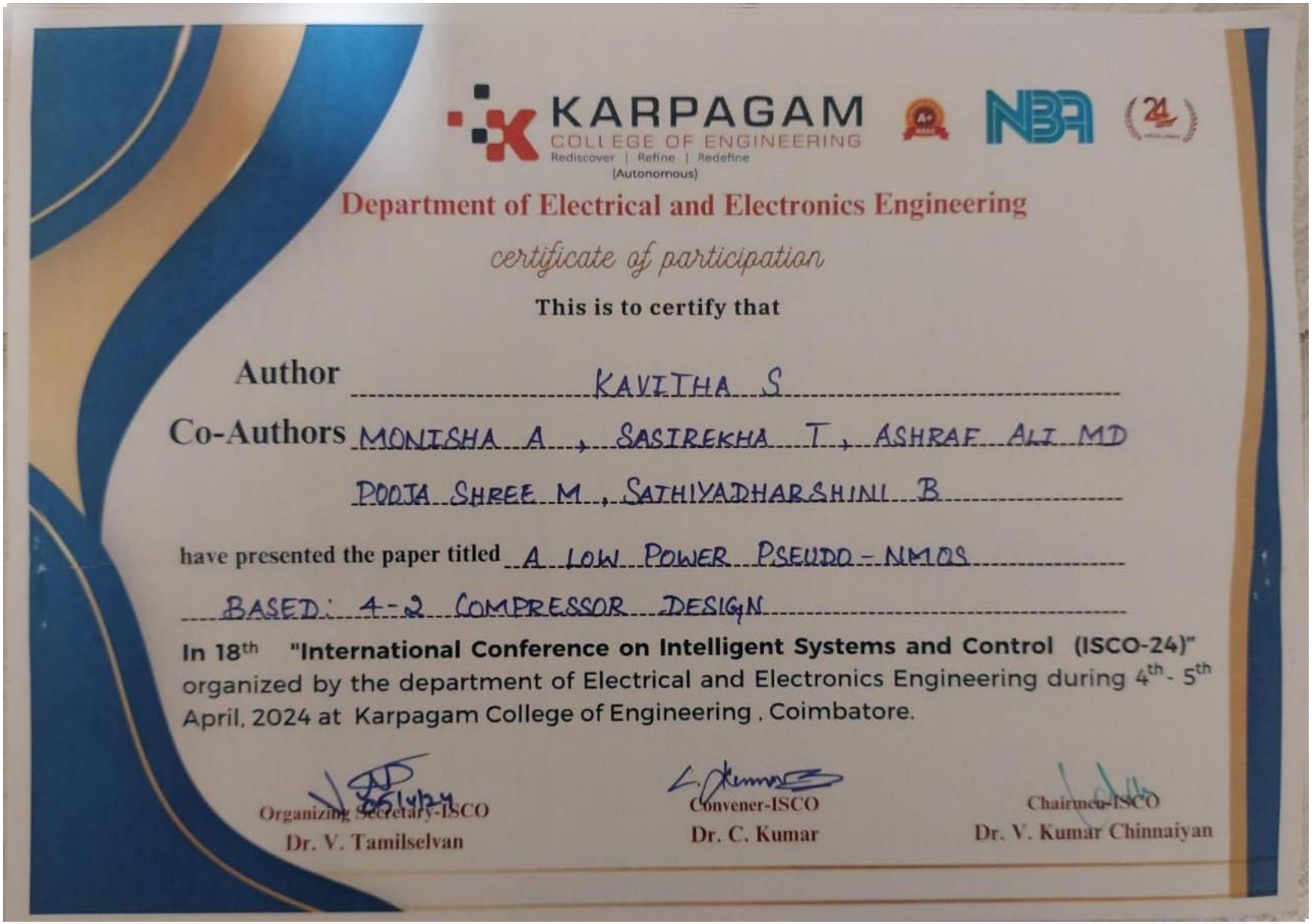
Abstract:

The compressor is a vital element widely utilized in VLSI circuits and systems, primarily serving as a pivotal processing unit. This research endeavours to design a 4-2 compressor employing XOR-XNOR and multiplexer modules. Implemented and simulated via Synopsys tools using 90nm CMOS technology, the compressor's performance is thoroughly evaluated. Key metrics such as average power dissipation and current ratings are meticulously computed to validate its efficacy. Furthermore, a comprehensive performance comparison is conducted against existing compressors. The findings underscore the proposed compressor's remarkable feat of exhibiting significantly lower power consumption when subjected to simulation under 90nm CMOS technology. Notably, in this study, we integrate n-MOS pseudo logic to further reduce power consumption, contributing to the enhancement of overall efficiency in various VLSI applications.

Keywords: 4-2 compressor, CMOS, Power, XOR-XNOR logic, Approximate Computing.



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Co-Authors MONISHA A, SASIREKHA T, ASHRAF ALI MD POOJA SHREE M, SATHIYADHARSHINI B

have presented the paper titled A LOW POWER PSEUDO-NMOS BASED 4-2 COMPRESSOR DESIGN

In 18th "International Conference on Intelligent Systems and Control (ISCO-24)" organized by the department of Electrical and Electronics Engineering during 4th - 5th April, 2024 at Karpagam College of Engineering , Coimbatore.

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