Tanishq Chauhan
21C3184
CS-B

Chauhan Rajshree
PAGE NO.: 01
DATE:

Digital Electronics (CER3C4)

Mid Semester Test - III

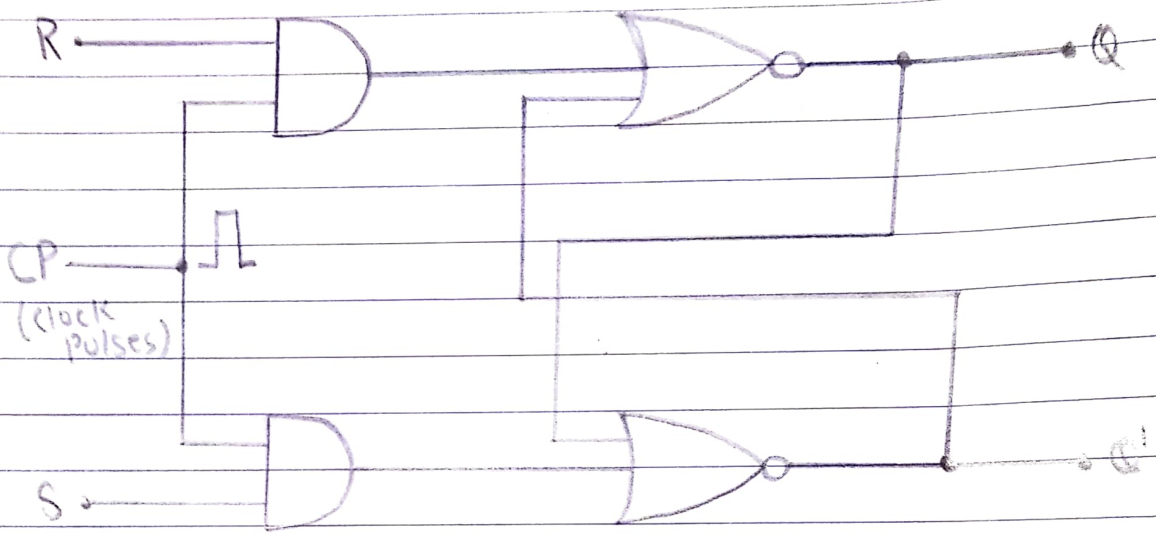
* Answer of Q. No. 1

S. No.	Flip - Flop	Latch
1.	Flip-Flop is a bistable device i.e., it has two stable states that are represented as 0 and 1.	1. Latch is also a bistable device whose states are also represented as 0 and 1.
2.	It checks the inputs but changes the output only at times defined by the clock signal or any other control signal.	2. It checks the inputs continuously and responds to the changes in inputs immediately.
3.	It is a edge triggered device.	3. It is a level triggered device.
4.	Gates like NOR, NOT, AND, NAND are building blocks of flip-flops.	4. These are ~~on~~ also made up of gates.
5.	They are classified into asynchronous or synchronous flip-flops.	5. There is no such classification in latches
6.	Flip-Flop always have a clock signal.	6. Latches doesn't have clock signal.
7.	Ex: D Flip-Flop, JK Flip-Flop	7. Ex: SR Latch, D Latch

Tanishq Chauhan
21C3184
CS-B

Chauhan Rajshree
PAGE NO.: 02
DATE:

Circuit Diagram of RS Flip-Flop

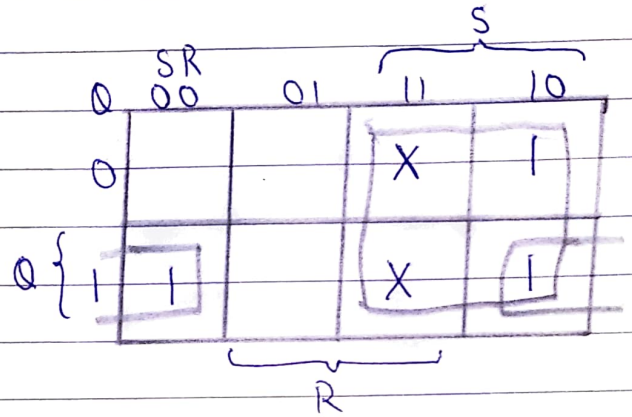


Truth Table of RS Flip-Flop

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

Tanishq Chauhan
2103184
CS-B

Characteristics Equation of RS Flip-Flop



$$Q(t+1) = S + R'Q$$

$$SR = 0$$

Tanishq Chauhan
21C3184
CS-B

Chauhan Rajshree
PAGE NO.: 04
DATE:

* Answer of Q. No. 3

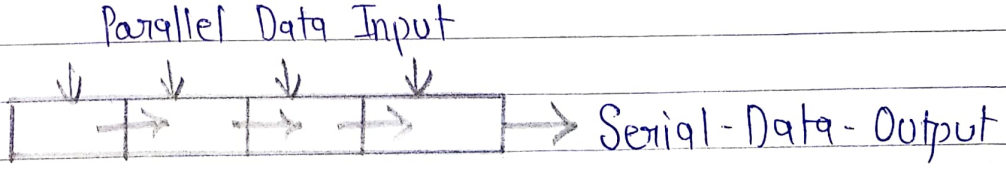
Shift Register

- A number of FFs connected together such that data may be shifted into and shifted out of them is called a shift register.
- Data may be shifted into or out of the register either in serial form or in parallel form.
- So there are four basic types of shif registers:

(i) Serial - In, Serial - Out
(ii) Serial - In, Parallel - Out
(iii) Parallel - In, Serial - Out
(iv) Parallel - In, Parallel - Out

- Data may be rotated left or right. Data may be shifted from left to right, or right to left at will, i.e, in a bidirectional way.

Parallel - ~~In~~put, Serial - Out



Parallel - In, Serial - Out, Shift Register

Tanishq Chauhan
21C3184
CS-B

- There are four data lines A, B, C, D through which the data is entered into the register in parallel form.
- The signal Shift / $\overline{LOAD}$ allows (a) the data to be entered in parallel form into the register and (b) the data to be shifted out serially from terminal Q_4.
- When Shift/$\overline{LOAD}$ line is HIGH, gates G_1, G_2, and G_3 are disabled, but gates G_4, G_5 and G_6 are enabled allowing the data bits to shift right from one stage to the next.

- When shift/$\overline{LOAD}$ line is low, gates G_4, G_5, G_6 are disabled, whereas gates G_1, G_2 and G_3 are enabled allowing the data input to appear at the D inputs of the respective FFs.
- When a clock pulse is applied, these data bits are shifted to the Q output terminals of the FFs and therefore, data is ~~at~~ inputted in one step.

- The OR gate allows wither the normal shifting operation or the parallel data entry depending on which NAD gates are enabled by the level on the Shift/$\overline{LOAD}$ input.

Tanishq Chauhan
2103184
CS-B

Chauhan

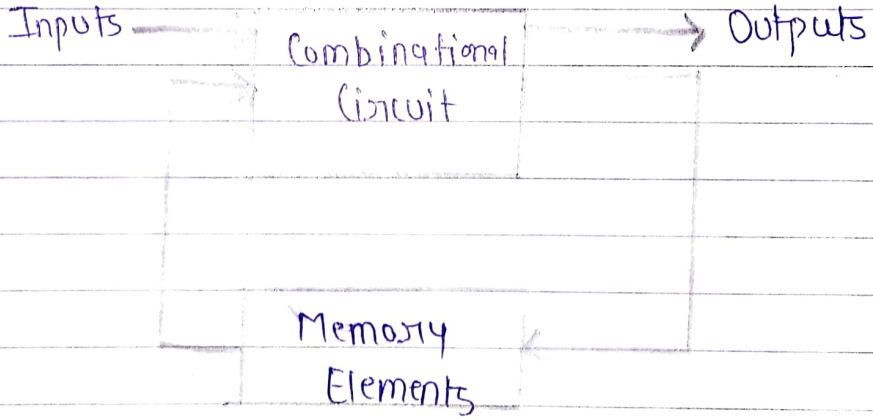
Rajshree
PAGE NO.: 06
DATE:

* Answer of Q. No. 5

- The sequential circuit is a special type of circuit that has a series of inputs and outputs. The outputs of the sequential circuit depend on the both combination of present input and previous outputs. The previous output is treated as the present state. S

- So, The sequential circuit contains the combinational circuit and its memory storage elements.

- A sequential circuit doesn't need to always contain a combinational circuit so, the sequential circuit can contain only the memory element.



Working :

(i) Previous output stored in m/r
(ii) Previous output is treated as present state.
(iii) So, next output is depends on previous output & present input.

Tanishq Chauhan
21C3184
CS-B

Chauhan Rajshree
PAGE NO.: 07
DATE:

* Answer of Q. No. 4

So, there are four basic types of shift registers:

(i) Serial-In, Serial-Out (SISO)
(ii) Serial-In, Parallel-Out (SIPO)
(iii) Parallel-In, Serial-Out (PISO)
(iv) Parallel-In, Parallel-Out (PIPO)

(i) Serial-In, Serial-Out

No of clock cycle required of Serial-In, Serial-Out is n+(n-1).
In SISO a single bit is shifted at a time in either right or left under clock control.
7 clock cycles are required in SISO.

(ii) Serial In, Parallel-Output

No of clock cycle required of Serial-In, Parallel-Output is n.
OR we can say that 1 clock cycle is required for SIPO.

(iii) Parallel-In, Serial-Output

No. of clock cycle required for ~~Ser~~ Parallel-In, Serial-Output is n
OR we can say that 4 clock cyle is required for SIPO.

Tanishq Chauhan
21C3184
CS-B

Chauhan Rajshree
PAGE NO.: 08
DATE:

(iv) Parallel-In, Parallel-Output

In PIPO, the inputs and outputs comes in a parallel way in register.

No. of clock cycle required is → 1.