

## Assignment - 2

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Semester :- 3<sup>rd</sup> Semester

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# Digital Electronics (CER3C4)

## Assignment - 2

1. Write a short note on each :

(i) RTL

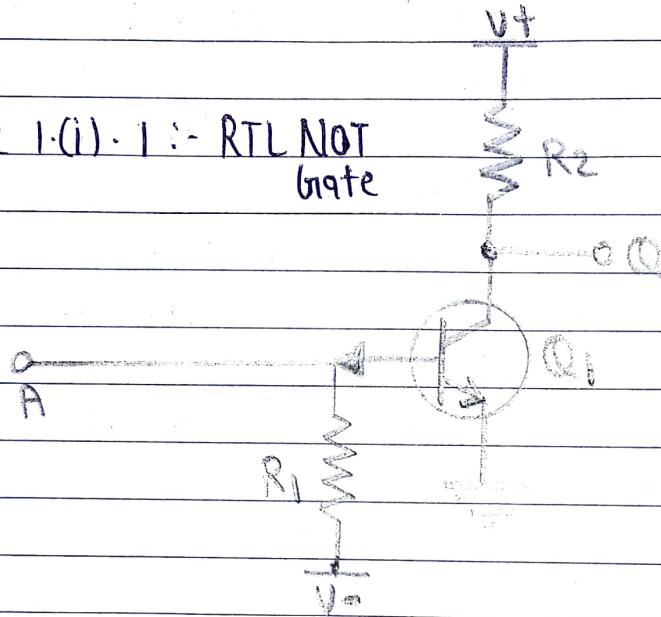
- RTL logic is the first family of logic circuit, it offers high performance but low noise margin.
- The Resistor - Transistor Logic (RTL) are digital circuits that are constructed using resistors and bipolar junction transistors (BJTs).
- The resistors are the input network while the transistors function as switching devices.
- RTL family was the first developed transistor logic circuit that were later improved to form the other classes like diode - transistor - logic (DTL) and transistor - transistor logic (TTL).
- The introduction of the RTL family revolutionized circuit technology by constructing the first RTL monolithic integrated circuit.
- RTL integrated circuit were used in the Apollo Guidance Computer, whose design was begun in 1961 and which first flew in 1966.

### Resistor - Transistor Logic (RTL) NOT Gate

Bipolar transistor switch is the simplest RTL gate. The resistor  $R_1$  in the circuit is used across the base and input terminals. The resistor increases the voltage

drop from 0.7 V to 1 V by converting the input voltage into current. The resistance  $R_1$  is chosen in such a way that it saturates the transistor and obtains high input resistance. The collector resistor  $R_2$  converts collector current into voltage. The resistance of  $R_2$  is high to saturate the transistor and low to obtain output resistance.

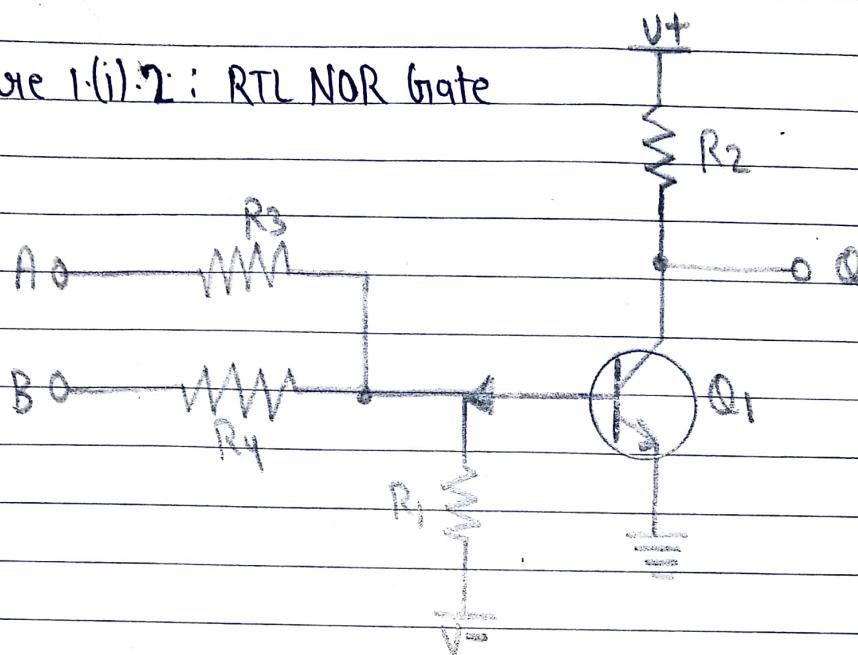
Figure 1(i). 1 :- RTL NOT gate



### RTL NOR gate

- The RTL NOT gate can be converted into an RTL NOR gate by introducing additional base resistors  $R_3$  and  $R_4$ .
- When both A and B are given in logic 0, then the transistor is cut off. The output is inverted since it is complementary. This is because the voltage drop across the collector-emitter junction of the transistor Q1 is taken at Q instead of taking it across collector resistor  $R_2$ .

Figure 1(i).2: RTL NOR Gate



### Parameters

Parameters of the RTL logic circuit are

- FanOut : 5
- Noise Margin : 0.2 volts
- Propagation Delay : 12 nano seconds
- Power Dissipation : 12 mW/gate
- Power Supply Voltage : 3.8 Volts

### Multistage NOR Gate

- A multistage NOR gate circuit consists of parallel connections of BJTs that are controlled by input logic. The inputs are not interconnected and hence if A is high, transistor Q1 conducts and pulls Q to the ground.
- Similarly, if B is high then transistor Q2 conducts and pulls Q to the ground.

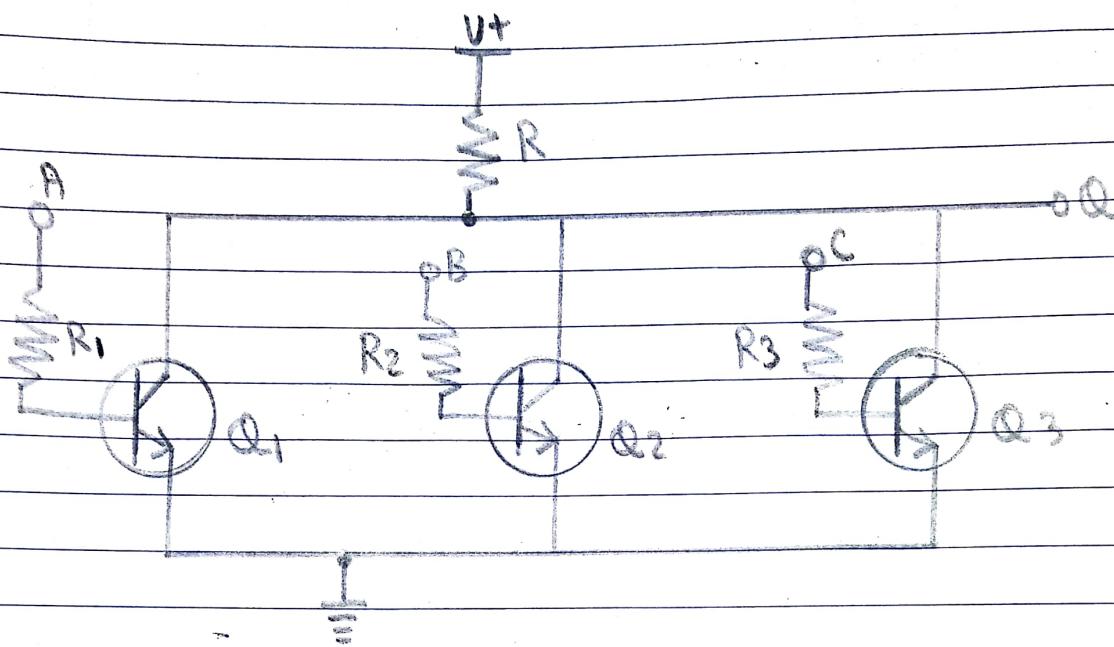


Figure 1-(i)-3 : Multistage NOR gate

### Advantages of RTL

- It used a minimum number of transistors.
- It has low power dissipation.

### Disadvantages of RTL

- It has poor noise immunity.
- It is relatively slow in speed.

(ii) DTL

- The next family, which was introduced after RTL is DTL which have better noise margin though slow in speed.
- Diode - Transistor Logic or DTL, refers to the technology for designing and fabricating digital circuits in which logic gates employ both diodes and transistors.
- DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed, especially in comparison to TTL.

Operation

- If any of one both inputs are at logic 0, That diode will be forward biased through resistor  $R_1$ , which will make the voltage at point X equal to zero and the transistor goes in cut-off state. No collector current results to low outputs (logic 0) at output point Y.

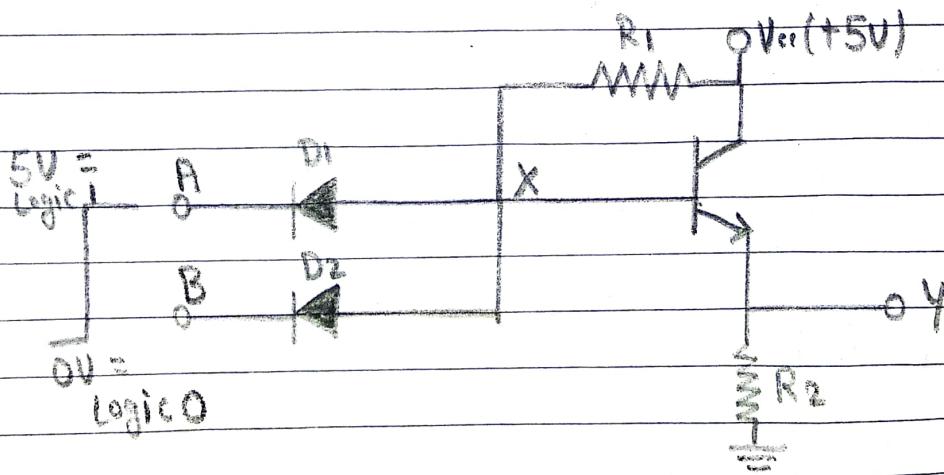


Figure 1.(iii).1 : DTL AND Circuit

- If all inputs are at logic 1 (+5V) the diodes are reverse biased, the transistor conducts heavily to saturation

and output becomes high (logic 1).

DTL OR Gate

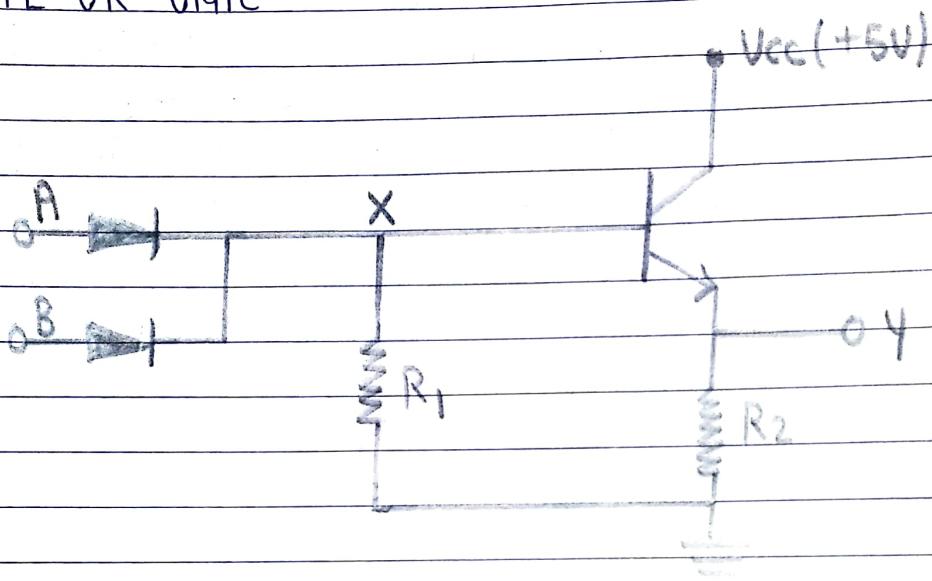


Figure 1.(ii).2 : DTL OR circuit

- If any or all input is at logic 1 (+5V) that diode conducts and point X is clamped to +5V which saturates the transistor and the output is high (at logic 1).
- If all inputs are at ground (logic 0), the diodes remain reverse biased and voltage at point X is zero which drive the transistor in cutoff region and the output is low (at logic 0).

DTL NAND Gate

- DTL, If both the inputs are high (logic 1), the diodes D<sub>1</sub> and D<sub>2</sub> are reverse biased and passes no current and point X is clamped to +5V; the diode D<sub>3</sub> is forward biased and current flows through R<sub>1</sub> and D<sub>3</sub> to the base of Q, thus saturating the transistor, this causes the output-point -Y to go low (logic 0).

- If either input changes to its low logic (logic 0) the corresponding input diode conducts and drives current from base of  $Q_1$ , thus the transistor is off and the output voltage rise to logic 1.

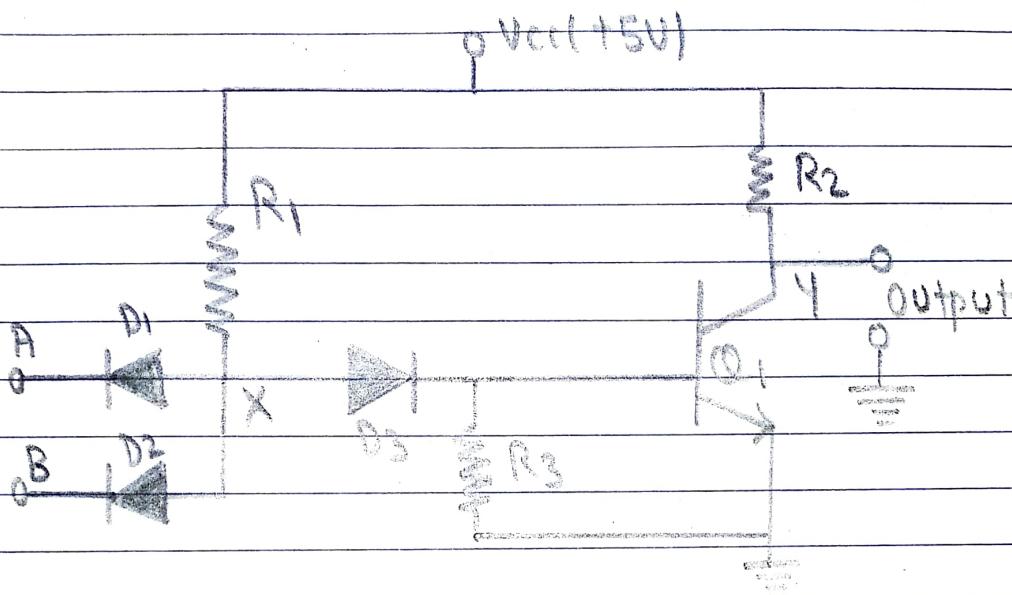


Figure 1.iii.3 : DTL NAND circuit

#### \* Parameters

- FanOut : 8
- Noise Margin : 0.7V
- Propagation Delay : 30 n sec
- Power Dissipation : 8-12 mW/gate
- Power Supply Voltage : +5V

#### \* Advantages of DTL

- It has better noise immunity than RTL circuit.
- It is much more economical because of the use of diode in place of resistors and capacitors.
- It has low power dissipation.

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## Disadvantages of DTL

- It has power noise margin.
- It has high propagation delay.

### (iii) TTL

- TTL logic is modified form of DTL logic, the input diodes in the case of DTL logic are replaced by transistors with one emitter with more than one emitter as input.
- It has come to existence so as to overcome the speed limitations of DTL family. The basic gate of this family is TTL NAND gate.
- Transistor Transistor Logic (TTL) is a logic family built from bipolar junction transistors. TTL integrated circuits (ICs) were widely used in applications such as computers, industrial controls, test equipments and instrumentation, consumer electronics, and synthesizer.
- It was build in 1961 by James L Bui and commercially used in logic design in 1963.

### Classification of TTL

TTLs are classified based on the output

#### 1. Open Collector Output

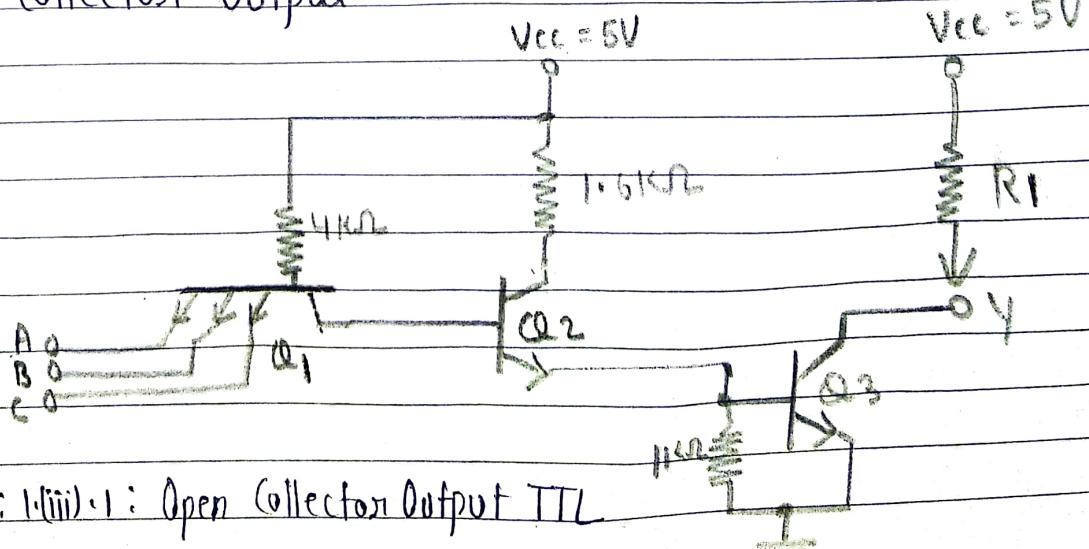


Figure: 1(iii).1: Open Collector Output TTL

- The main feature is that its output is 0 when low and floating when high.
- Usually an external  $V_{cc}$  may be applied.

## 2. Totem Pole Output

- Totem Pole means addition of an active pull up circuit in the output of the Gate which results in reduction of propagation delay.

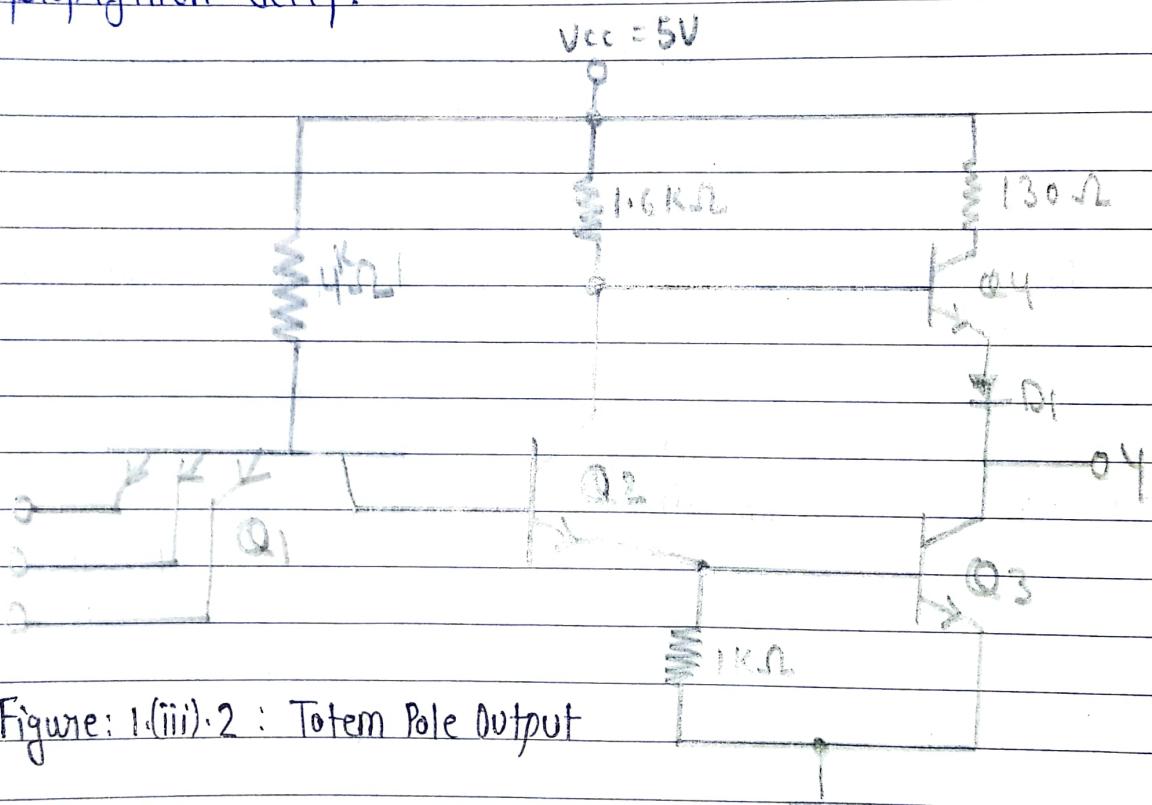
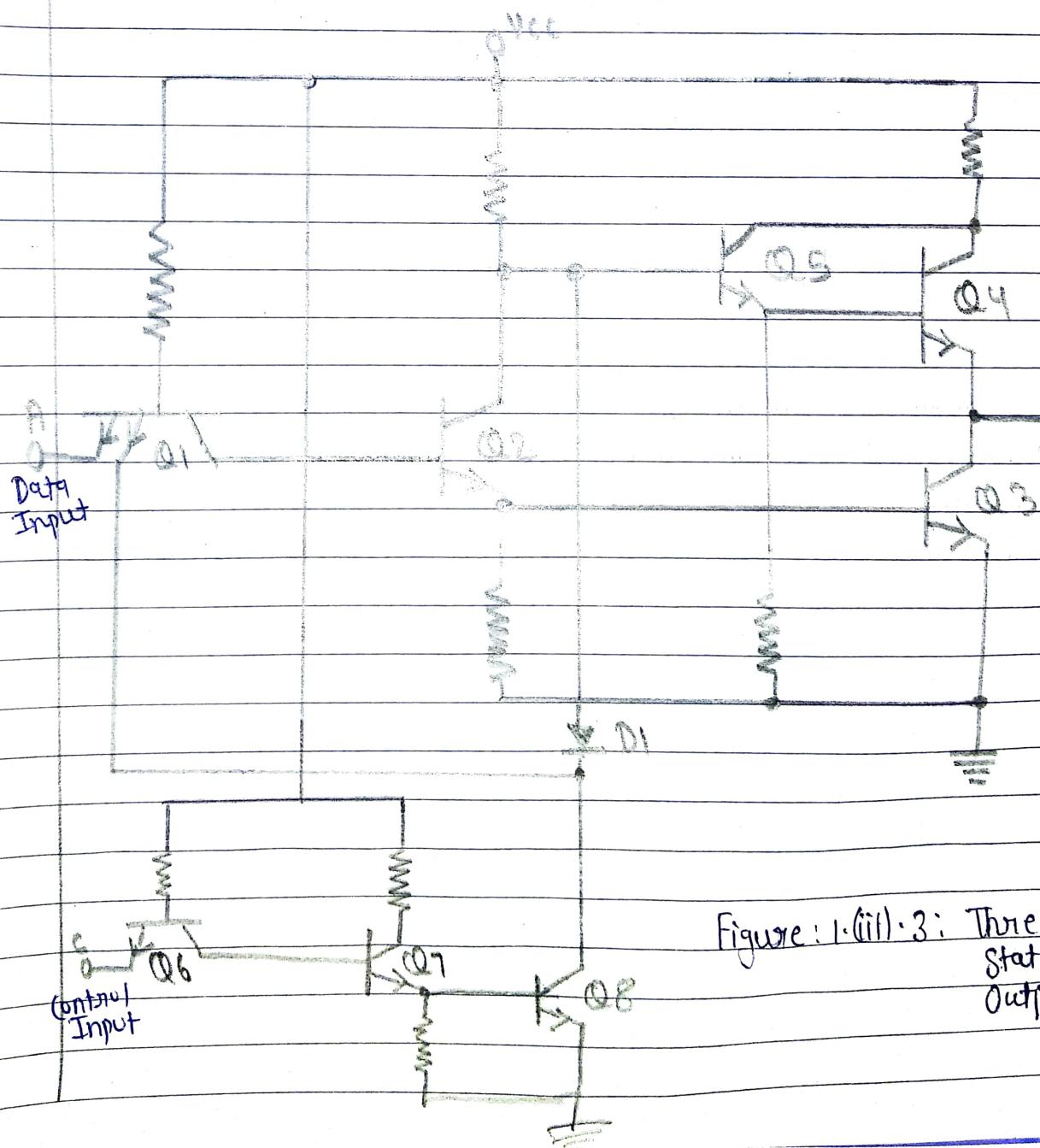


Figure: 1.(iii).2 : Totem Pole Output

- Logic operation is same as the open collector output. Use of transistors Q4 and diode is to provide quick charging and discharging of parasitic capacitance across Q3. Resistor is used to keep the output current to a safe value.

3. **Three State Gate:** It provides 3 states output.

- (i) Low level state when lower transistor is ON and upper transistor is OFF.
- (ii) High level state when lower transistor is OFF and upper transistor is ON.
- (iii) Third state when both transistors are OFF. It allows a direct wire connection of many outputs.



## Features of TTL Family

- Logic low level is at 0.05 to 0.2V
- Logic high level is at 5V
- Typical fan out of 10. It means it can support at most 10 gates at its output.
- A basic TTL device draws a power of almost 10mW, which reduce with use of schottky devices.
- Average propagation delay is about 9ns.
- The noise margin is about 0.4V.

## Advantages of TTL

- The main advantage of TTL IC's is that they are compatible with other IC's
- It has high speed of operation.
- Its small size yields more function on an IC.
- It has low output impedance which improves the fan-out capability.
- It has good noise immunity, in worst case it is 0.4V and typically it touches 1V.
- It is less expensive.

## Disadvantages

- It generates switching transients, which can be eliminated by the use of bypass capacitors.
- Wired output capability is not possible except with low level and open collector IC's.

(iv) MOS

The MOS is a unipolar transistor that depends on the flow of only one type of carrier, which may be electrons (n-channel) or holes (p-channel).

MOS technology is generally categorized in two basic forms:

1. A p-channel MOS is referred to as PMOS.
2. A n-channel MOS is referred to as NMOS.

PMOS

The operations performed by a PMOS logic family can be explained by considering a PMOS NAND gate.

When a low logic is applied to either A or B, the transistor gets activated, this makes a connection between power supply and the output terminal.

The following diagram shows a two input PMOS NAND gate

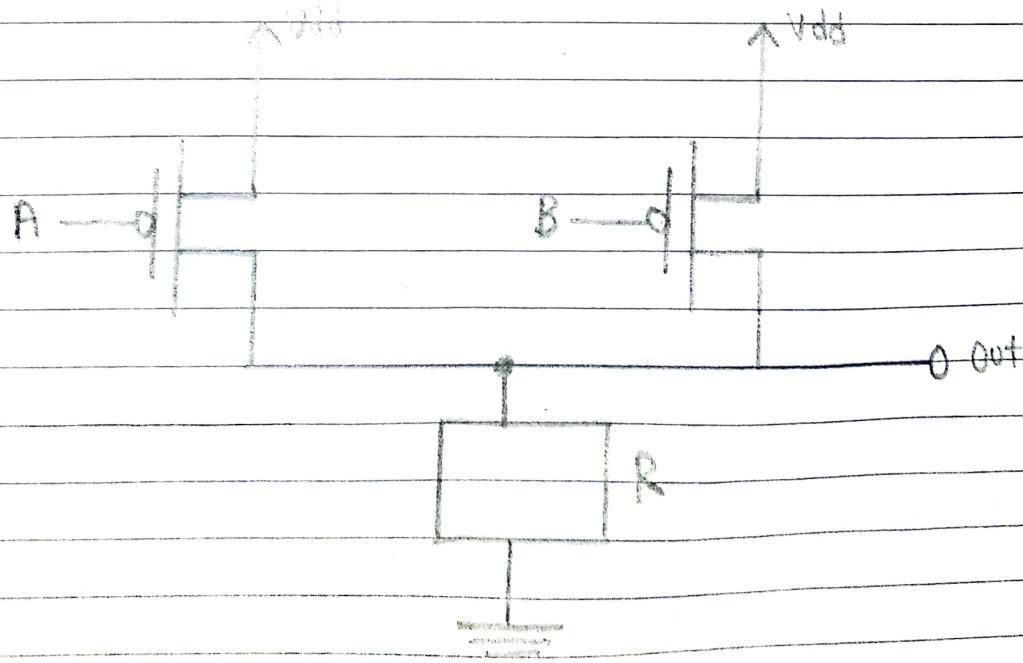


Figure 1.10.1 : PMOS NAND

When a low logic is applied the output is raised to a high logic value. Otherwise, it will remain at logic low in other cases.

The pull-down resistor 'R' maintains the LOW logic unless a low logic is applied to either A or B.

## NMOS

The structure of NMOS logic is similar to that of PMOS. However, instead of using PMOS transistor, here we will use NMOS transistor along with a pull-up resistor R.

The following circuit diagram shows a two input NMOS NAND gate.

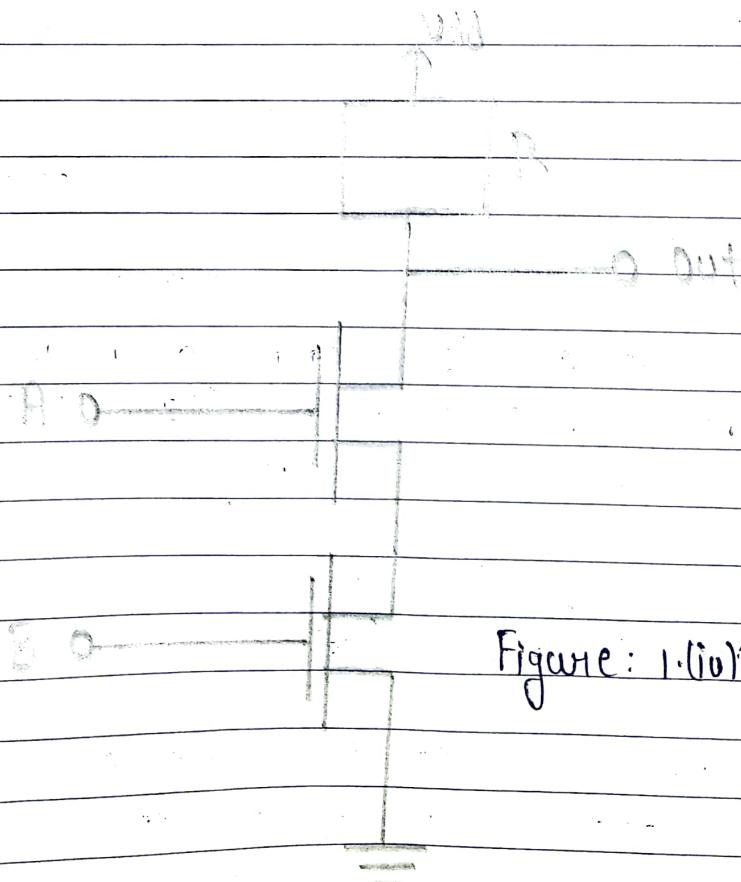


Figure: 1.(i)(-2 : NMOS NAND

As shown in the circuit diagram, on NMOS, NAND gate has two NMOS transistors connected in series from the output to the ground terminal.

A pull-up resistor is connected from the output terminal to power supply.

When a high logic is applied to both inputs, both of the transistors gets activated. This make a connection between the output terminal and ground.

In case, any one of the input is at logic HIGH, and the other one is at logic LOW, the transistor gets deactivated. This terminates the path between the outputs terminal and ground.

## CMOS (Complementary Metal-Oxide Semiconductor)

The complementary MOS or CMOS technology uses PMOS or NMOS transistors connected in a complementary manner in all circuit.

CMOS logic families are highly preferred in large-scale integrated circuits because of its high noise immunity and low power dissipation.

CMOS technology is used in microprocessors, microcontrollers, static RAM and other digital logic circuits.

Q1 and Q2 are the respective NMOS and PMOS transistors connected in a complementary fashion in figure.

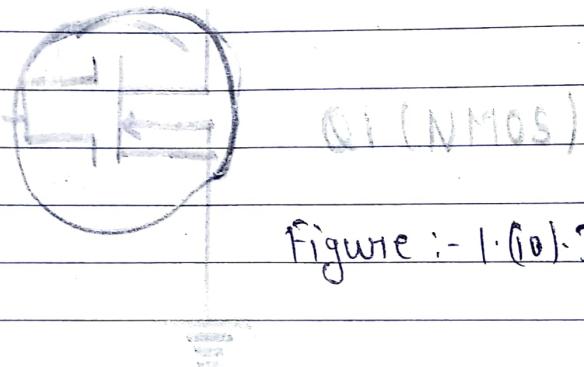
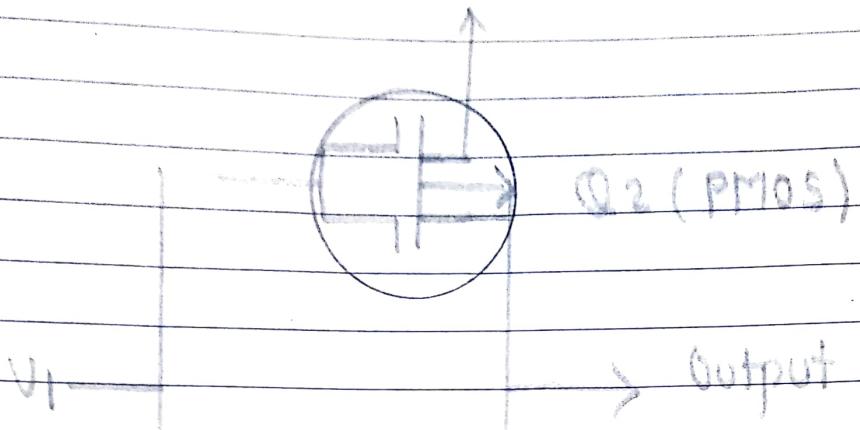


Figure :- 1.10.3 : CMOS

### Advantages of CMOS

- Low Cost
- Simplicity of Design
- Low Heat Dissipation
- Superior Fan-Out and Wide logic swings.
- Good noise margin performed and Wide - Range - Operation.

### Disadvantages of CMOS

- Slower than Bipolar digital ICs such as TTL devices.
- Careful handling for protects from static discharges is needed.