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Computer Organization & Architecture (CER36GT)

Mid Semester Test - III

* Answer of Q. No 1

S. No.	Isolated I/O	Memory Mapped I/O
1.	Memory and I/O have separate address space.	1. Both have same address space.
2.	It is complex due to separate separate logic is used to control both.	2. Simpler logic is used as I/O is also treated as memory only.
3.	Separate instruction control read and write operation in I/O and Memory.	3. Same instructions can control both I/O and Memory.
4.	It is more efficient due to separate buses.	4. It is lesser efficient.
5.	Isolated I/O is larger in size due to more buses.	5. Memory Mapped I/O is smaller in size.

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* Answer of Q. No. 2

- DMA controller - Interface which allows I/O transfer directly between Memory and Device, freeing CPU for other tasks.
- CPU initializes DMA controller by sending memory address and the block size (number of words).
- The DMA controller needs the usual circuits of an interface to communicate with the CPU and I/O device.
- In addition, it needs an address register, a word count register, and a set of address lines.
- The address register and address lines are used for direct communication with the memory.
- The word count register specifies the number of words that must be transferred.
- The data transfer may be done directly between the device and memory under control of the DMA.
- Figure 2.1 shows the block diagram of a typical DMA controller.
- The unit communicates with the CPU via the data bus and control lines.
- The register in the DMA are selected by the CPU through the address bus by enabling the DS (DMA select) and RS inputs.
- The RD (Read) and WR (Write) inputs are bidirectional.
- When the BG input is 0, the CPU can communicate with the DMA register through the data bus to read from or write to the DMA register.
- When BG = 1, The CPU has relinquished the buses and the DMA can communicate directly with the memory by specifying an address an address in the address but and activating the RD or WR control.

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Answer of Q. No. 2.

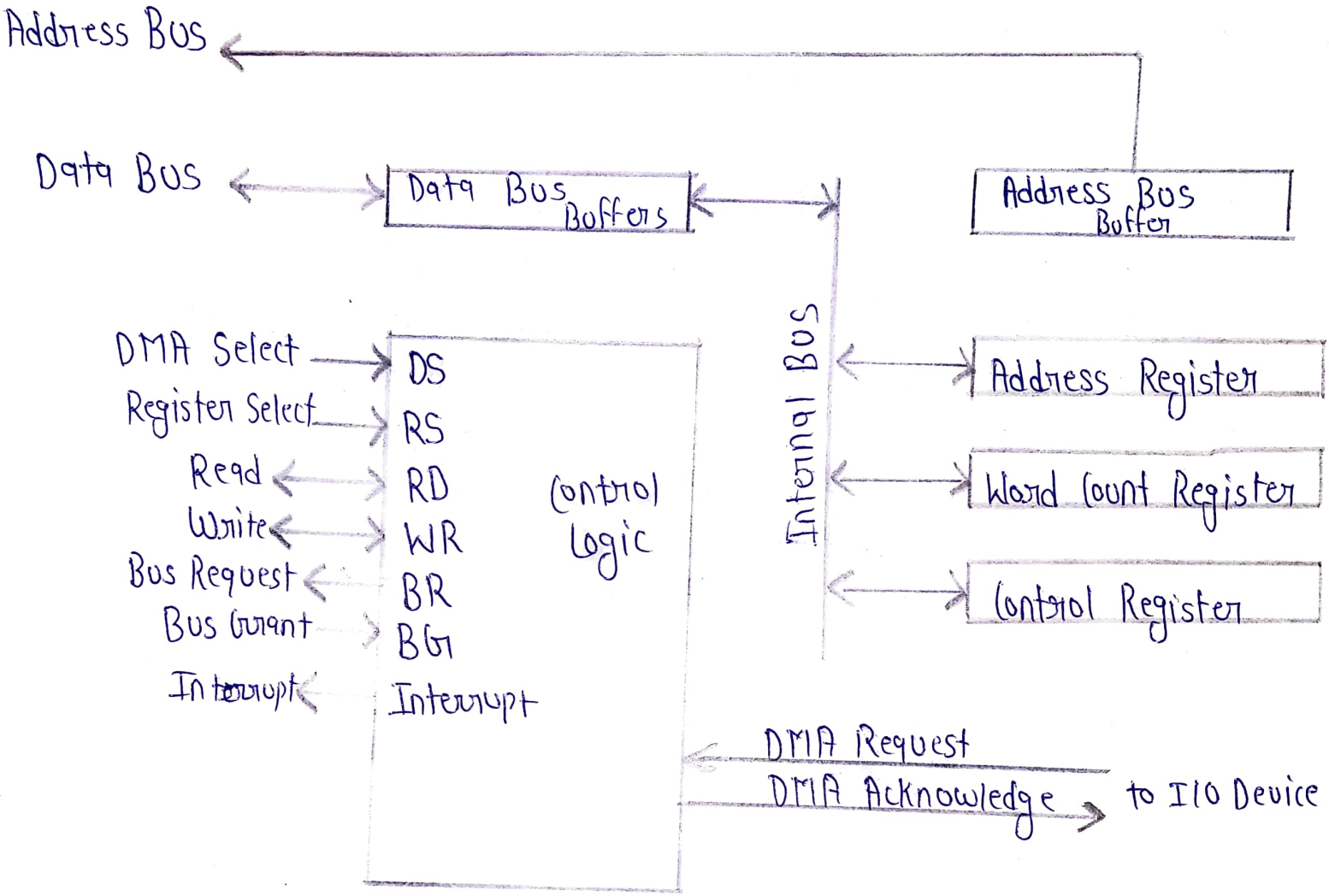

Figure 2.1 : Block Diagram of DMA Controller

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- The DMA communicates with the external peripheral through the request and acknowledge lines by using a prescribed handshaking procedure.
- The DMA controller has three registers: an address register, a word count register, and a control register.
- The address register contains an address to specify the desired location in memory.
- The word count register holds the number of words to be transferred
- The register is decremented by one after each word transfer and internally tested for zero.
- The control register specifies the mode of transfer.
- All register in the DMA appear to the CPU as I/O interface registers.
- Thus the CPU can read from or write into the DMA register under program control via the data bus.
- The DMA is first initialized by the CPU.
- After that, the DMA starts and continues to transfer data between memory and peripheral unit until an entire block is transferred.

Why

DMA stands for direct

In

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Why

In CPU controller and DMA controller. The write and read control lines are "shared" between the DMA controller and CPU controller, they all have to be bidirectional.

So we can say that both the CPU controller and the DMA controller can control (active) these lines when needed.
On the other ~~hand~~ word also we can say that, These control lines running through the data buses and also having control signals, when a DMA controller places a Bus Request input (BR) to CPU and to take the control the over Buses.

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* Answer of Q. No. 3

Von Newmann proposed his computer architecture design in 1945 which was later known as Von Newann architecture. It consisted of a control unit. Arithmetic and Logical Memory Unit (AUL), Registers & Input/Outputs.

Von Newmann architecture is based on the stored program computer concept, where instruction data and program data are stored in same memory. The design is still used in most computer produced today.

A Von Newmann Based Computer Consists:

Uses a single processor
Uses one memory for both instruction and data
Executes program following fetch-decode-execute cycle.

Whatever we do to enhance performance, we cannot getaway from the fact instructions can only be done one at a time and can only be carried out sequentially. Both of these factors holds back the competence of the CPU. This is commonly referred to as the "Von Newmann Bottleneck".

This architecture is very important and is used in our PCs and even in Super Computers.

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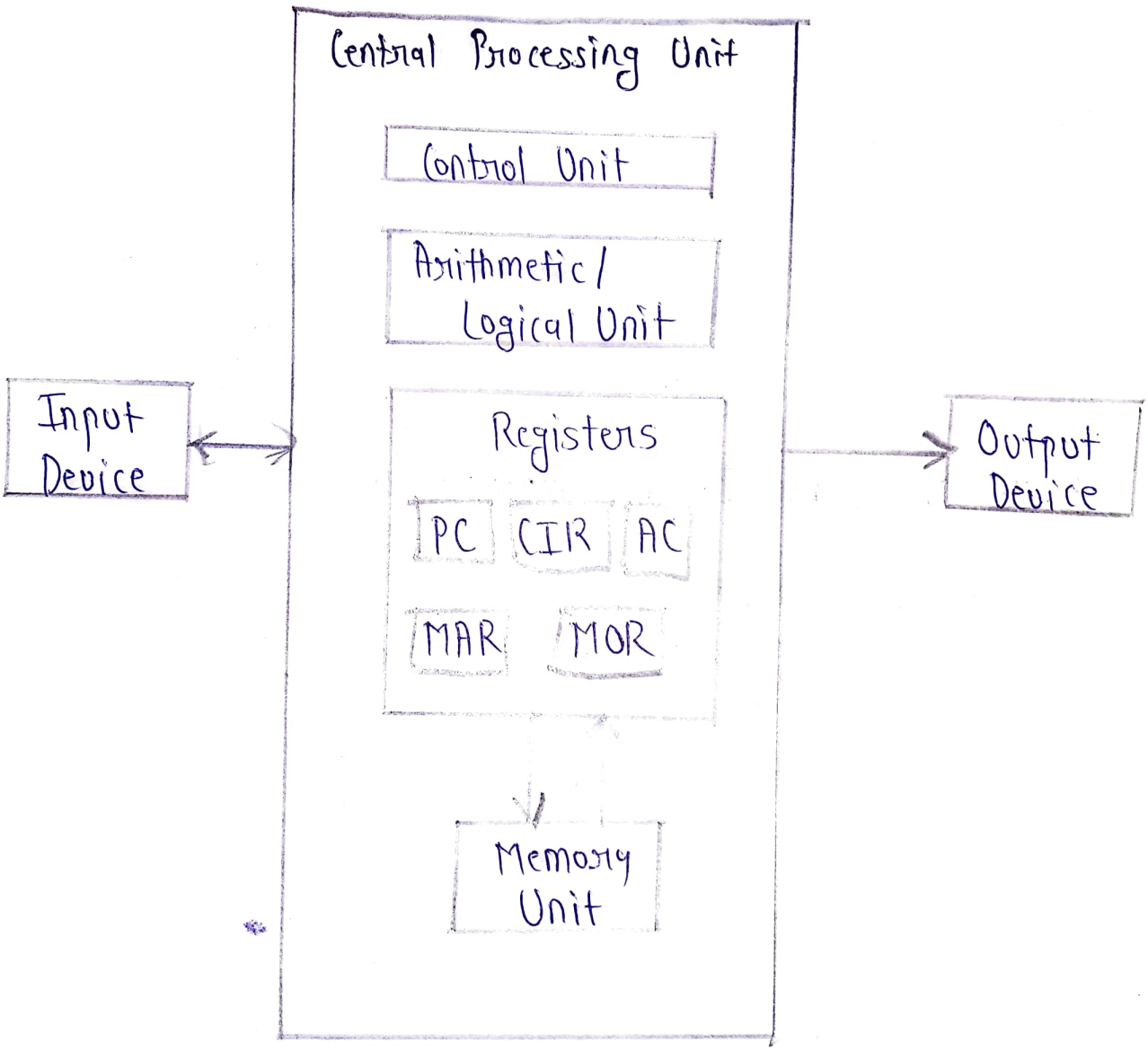

Figure 3.1 : Von-Newmann Basic Architecture

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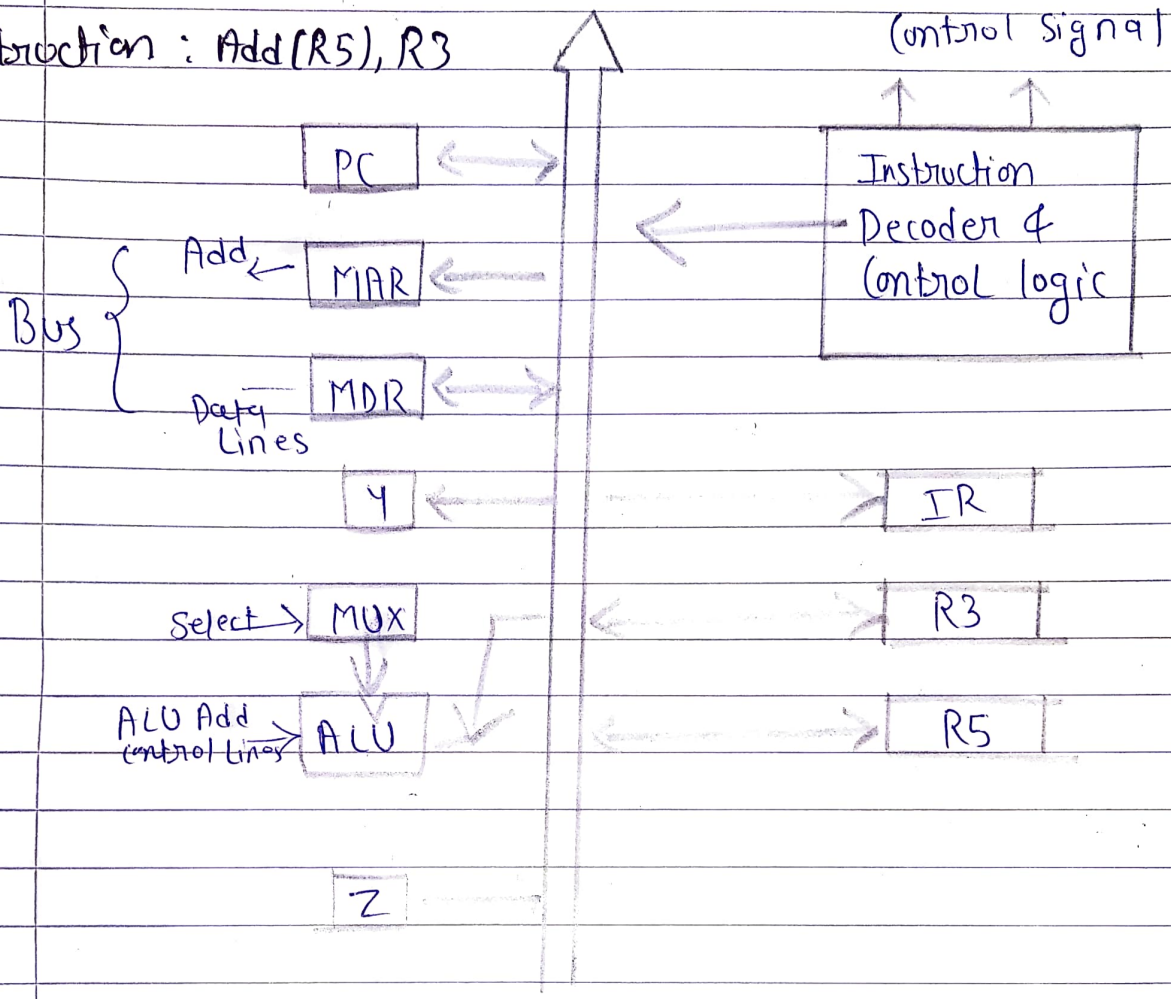
* Answer of Q. No. 4

Instruction : Add (R5), R3



Processor Bus

The processor is as follows

- Program counter will give address
- Address is sent to MAR along with the read signal
- R5 indicates direct address is not given - Read signals will read the address from R5 where data has to be fetched.
- MUX y selects constant as selected addition operation performed in ALU of the constant and data fetched is stored in Z

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- The stored answer is moved from Z to PC. Its is written in Y
- WMFC signal is released in dicating that writing operation is completed
- MDR to IR signal are moved for decoding of instructions
- Original opperand of R3 is fetched and moved to Y & WMFC signals are occur.
- After fade, data is moved out of MDR & data in Y is selected & performed in ALU
- The result is stored in Z
- The resultant is moved from Z to R3 regular.