

End - Sem Examination

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Computer Organization & Architecture (CER361)

* Answer of Q.No. 1(c)

Flynn's Classification

M.J Flynn proposed a classification for the organization of a computer system.

It is based on the multiplicity of Instruction Stream and Data Streams.

Instruction Stream

Sequence of instructions read from memory constitutes an Instruction stream.

Data Stream

The operation performed on the data in the processor constitutes a data stream.

A data stream is sequence of data having input, partial or temporary result.

Based on the multiple data and instruction streams Flynn's classify the digital computers in four categories.

Single Instruction Stream, Single Data Stream (SISD)

Single Instruction Stream, Multiple Data Stream (SIMD)

Multiple Instruction Stream, Single Data Stream (MISD)

Multiple Instruction Stream, Multiple Data Stream (MIMD)

		Number of Data Streams	
		Single	Multiple
Number of Instruction Streams	Single		
	Multiple		

Figure 1-(c)-1 : Flynn's Classification

* Single Instruction Stream, Single Data Stream (SISD)

SISD stands for "Single Instruction and Single Data Stream".

SISD represents the organization of a single computer containing a control unit, a processor unit, and a memory unit.

Instructions are executed sequentially and the system may or may not have internal parallel processing capabilities.

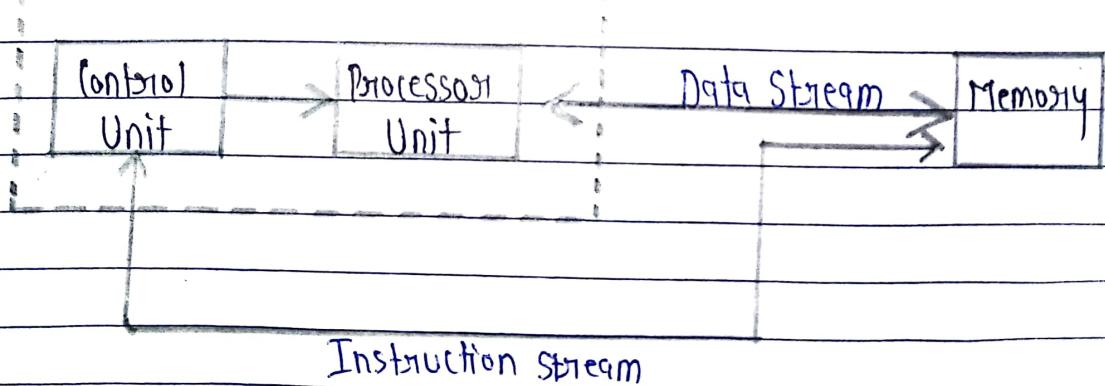


Figure 1-(c)-2 : SISD Organization

In SISD, machine instructions are processed in a sequential manner and computers adopting this model are popularly called sequential computer.

Most conventional computers have SISD architecture like the traditional Von-Neumann computers.

All the instructions and data to be processed have to be stored in primary memory.

Parallel processing, in this case, may be achieved by means of multiple functional units or by pipeline processing.

Instructions are decoded by the control unit and then the control unit sends the instructions to the processing units for execution.

Data stream flows between the processors and memory bi-directionally.

Examples :- Older generation computers, minicomputers, and workstations, IBM PC etc.

* Single Instruction Stream, Multiple Data Stream (SIMD)

SIMD stands for "Single Instruction and Multiple Data Stream".

SIMD represents an organization that includes many processing units under the supervision of a common control unit.

All the processors receive the same instruction from the control unit but operate on different items of data.

The shared memory unit must contain multiple modules so that it can communicate with all the processors simultaneously.

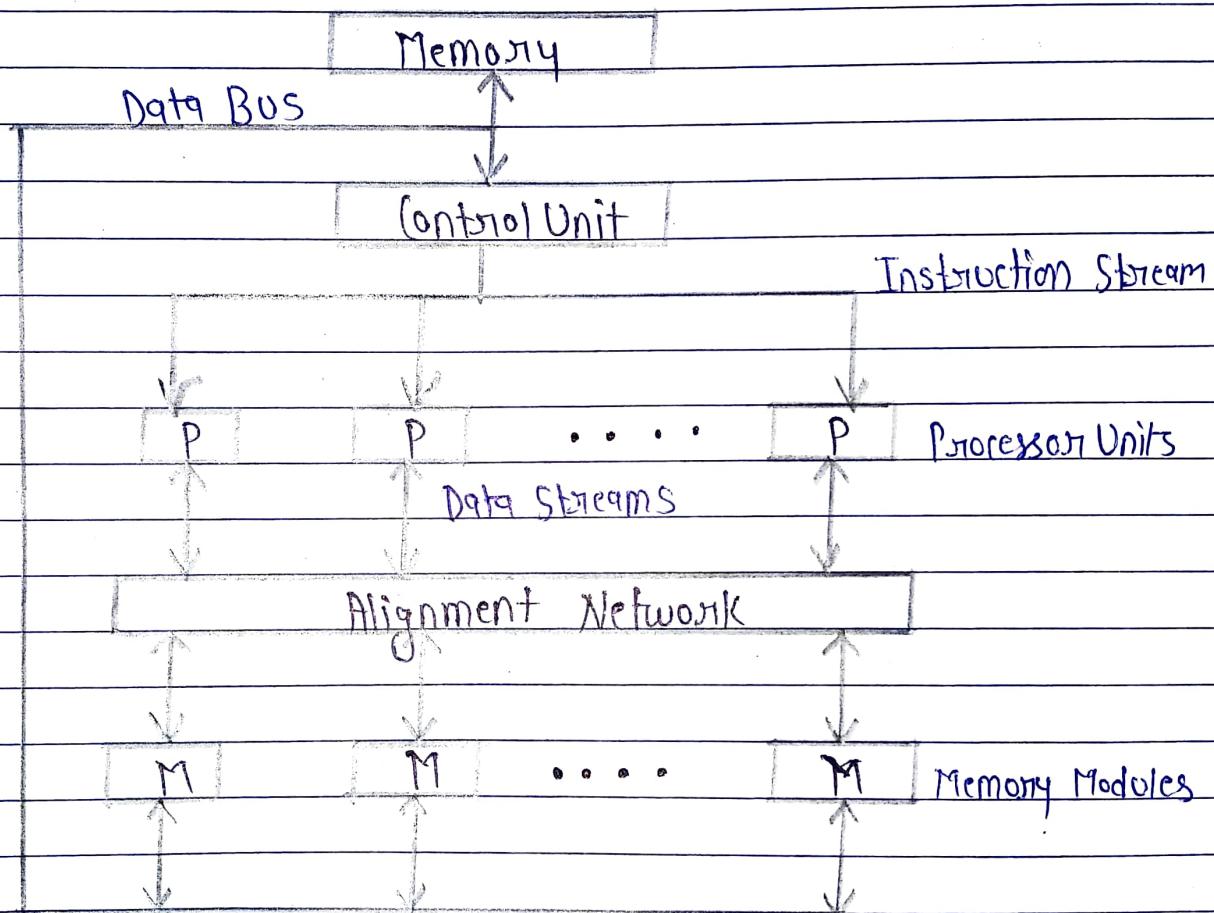


Figure 1-(c)-3 : SIMD Organization

SIMD is mainly dedicated to array processing machines. However, vector processor can also be seen as a part of this group.

Dominant representative SIMD systems is Gray's vector processing machine.

Example :- Wireless MMX Unit

* Answer of Q. 1 (B)

Computer Organization

It refers to the operational unit and the interconnection between them that achieve the architectural specifications. It tells us about different functional blocks of the system. It is basically the realization of architecture and deals with functional structure and various structural relationships.

It deals with the concept that is transparent from the programmer.

It includes physical connection component like circuits with adder and substractors.

Single Accumulator Organisation, General Register Organisation, Stack Organisation are the 3 types of CPU Organisation.

Computer Architecture

It refers to those attributes of the system that are visible to the software programmer and have a direct impact on the logical execution of program like a number of bits used to represent various data types, the instruction set of the computer, technique for addressing, memory method used for input, output etc.

It basically defines the system in an abstract manner. It deals with the concepts that the programmer deals with directly.

It includes logical units like instruction set, different types of addressing modes.

The following 3 main categories are considered while considering design of architecture: System Design (contains hardware components that are used for building the system), Instruction Set Architecture (includes all the instruction provided to the computer system) and Micro Architecture (give minute detail about storage element).

Difference Between Computer Architecture and Organization

Computer Organization

Computer Architecture

- | | |
|-----------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| 1. Computer Organization is concerned with the structure and behavior of a computer system as seen by the user. | 1. Computer architecture is concerned with the way hardware components are connected together to form a computer system. |
| 2. Organization describes how computer does it. | 2. Architecture describes what the computer does. |
| 3. Computer Organization deals with structural relationship | 3. Computer Architecture deals with functional behavior of computer system. |
| 4. It deals with low-level design issue. | 4. It deals with high level design issue. |
| 5. Organization indicates its performance. | 5. Architecture indicates its hardware. |

Computer Organization

6. Computer, For designing a computer, organization is decided after its architecture
7. Computer Organization is frequently called as micro architecture
8. ~~And~~ Computer Organization handles the segments of the network in a system.
9. Computer organization consists of physical units like circuit designs, peripherals and adders.

Computer Architecture

6. For designing a computer, its architecture is fixed first
7. Computer Architecture is also called as instruction set architecture.
8. Architecture coordinates between the hardware and software of the system.
9. Computer architecture comprises logical function such as instruction set, registers, data types, and addressing modes.

Answer of Q. No. 5 (A)

Before pipeling was introduced, the different processes can't be implemented simultaneously i.e. the processes can be executed completely one by one which leads to more time consumed by processor.

Pipelining is a process of arrangement of hardware elements of the CPU such that its overall performance is increased. Here, multiple instructions are overlapped during execution, which allows multiple instructions / processors to start their execution at some time.

Pipelining results in decrement in overall clock cycles required to execute several instruction which leads to high speed without changing the length of one clock cycle. Example, in real life pipelining can be seen in car manufacturing plants, where huge assembly lines are setup at each point, one is installing the engine, at the same time other is doing car body work for another car like this, new car is manufactured every few minutes.

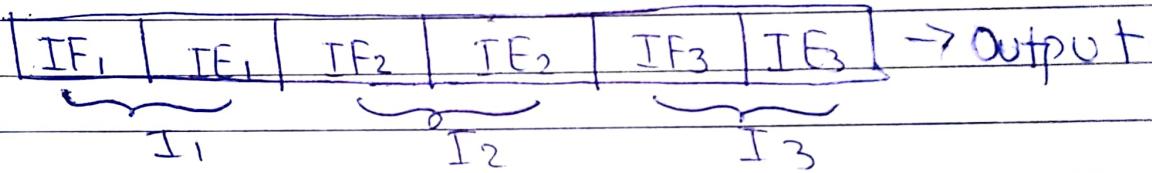
Consider, there are instruction to be executed I₁, I₂ and I₃. Each instruction

can be divided into 2 stages,

IF, Instruction Fetch

IE, Instruction Execution

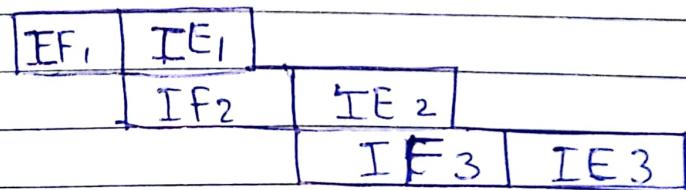
In non pipelined structure, each task is executed in sequential manner i.e. one task is executed before beginning of another task.



Clock Cycles :- 6

In pipelined structure, the whole execution phase can be divided into several levels, stages.

Clock Cycle 1 2 3 4



In clock cycle 2, I_1 is executed at some time, fetch phase of I_2 is being carried out. Some at IE_2 , TF_3 began so at clock cycle 4 all instructions have executed ~~so far~~ successfully

Clock Cycles :- 4

So as per this example we can say that pipelined structure improve performance of a computer system.

Answer of Q. No. 5(B)

Clock rate of non pipelined architecture = 2.5 GHz

Clock period of non pipelined architecture, $T_n = \frac{1}{2.5}$ nanoseconds.

Total Execution time for non pipelined architecture

:- Clock $\times T_n$

T_n (PIN) = (CPI \times cycle per instruction)

$$= 4 \times \frac{1}{2.5}$$

$$= 1.6 \text{ nanoseconds}$$

Clock rate of pipelined architecture = $f_p = 2 \text{ GHz}$

Clock period of pipelined architecture / $T_p = \frac{1}{2} \text{ ns}$

Total Execution time for pipelined architecture = $(P_{IP} \times T_p) / (T_n)$

Pipeline can be assumed to be full so, every cycle executes one instruction.

$$\text{i.e. } (P_{IP} = 1)$$

$$T_n = 1 \times \frac{1}{2}$$
$$= 0.5 \text{ nanoseconds}$$

$$\begin{aligned} \text{Speed} &= T_n = \frac{1.6}{0.5} \\ \text{Factor} &= T_p \\ &= 3.2 \end{aligned}$$

Pipelined architecture is 3.2 times faster than non pipelined architecture.

Answer of Q. No. 4 (A)

Direct Memory Access

Transfer of data under programmed I/O is between CPU and peripheral.

In direct memory access (DMA), Interface transfers data into and out of memory through the memory bus.

The CPU initiates the transfer by supplying the interface with the starting address and the number of words needed to be transferred and then proceeds to execute other tasks.

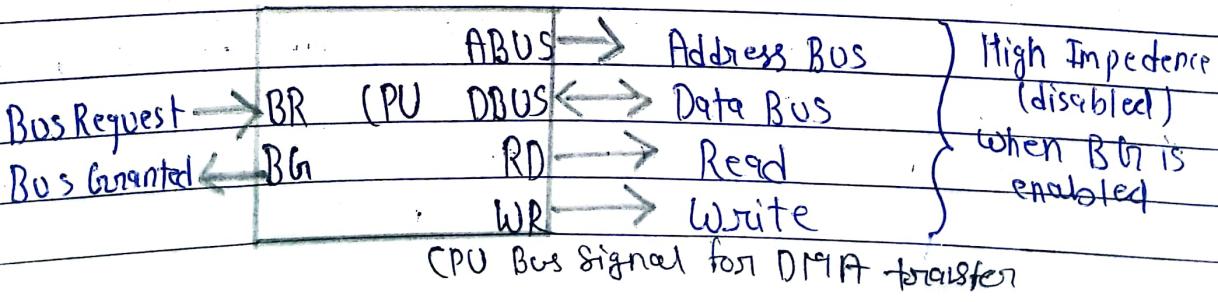
When the transfer is made, the DMA requests memory cycles through the memory bus.

When the request is granted by the memory controller, DMA transfers the data directly into memory.

DMA controller

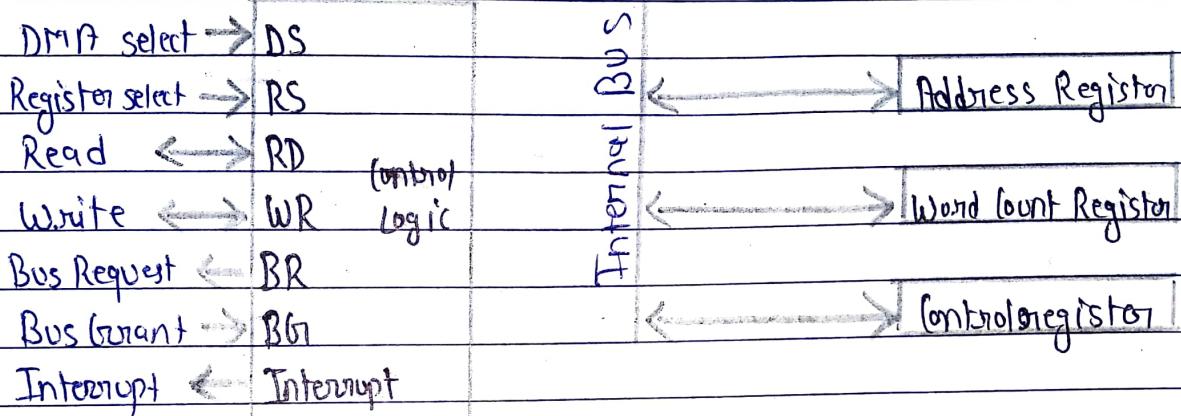
DMA controller - Interface which allows I/O transfer directly between Memory and Device, freeing CPU for other tasks.

CPU initializes DMA controller by sending memory address and the block size (number of words).



Address Bus ← →

Data Bus ← → Data Bus Buffer ← → Address Bus Buffer



DMA Request → I/O Device
DMA Acknowledge ←

Figure : 4.(A).2 : Block Diagram of DMA controller

The DMA controller needs the usual circuits of an interface to communicate with the CPU and I/O device. In addition, it needs an address register, a word count register, and a set of address lines.

The address register and address lines are used for direct communication with the memory.

The word count register specifies the number of words that must be transferred.

The data transfer may be done directly between the device and memory under control of the DMA.

The unit communicates with the CPU via the data bus and control lines.

The registers in the DMA are selected by the CPU through the address bus by enabling the DS (DMA select) and

RS (register select) inputs.

The RD and WR inputs are bidirectional.

When the B7 input is 0, the CPU can communicate with the DMA registers through the data bus to read from or write to the DMA register.

When B7 = 1, the CPU has relinquished the bus and the DMA communicate directly with the memory by specifying an address in the address bus and activating the RD or WR control.

The DMA communicates with the external peripheral through the request and acknowledge lines by using a prescribed handshaking procedure.

The DMA controller has three registers: an address register, a word count register and a control register.

The address register contains an address to specify the desired location in memory.

The word count register holds the number of words to be transferred.

The register is decremented by one after each word transfer and internally tested for zero.

The control register specifies the mode of transfer.

All register in the DMA appear to the CPU as I/O interface register.

Thus the CPU can read from or write into the DMA register under program control via the data bus.

The DMA is first initialized by the CPU.

The CPU initializes the DMA by sending the following information through the data bus.

1. The starting address of the memory block where data are available (for read) or where data are to be stored (for write).
2. The word count, which is the number of words in the memory block.
3. Control to specify the mode of transfer such as read or write.
4. The starting address is stored in the address register.

Answer of Q. No. 4 (c)

Difference Between Isolated I/O and Memory Mapped I/O

S.No.	Isolated I/O	Memory Mapped I/O
1.	Memory and I/O have separate address space.	1. Both have same address space.
2.	It is complex due to separate separate logic is used to control both.	2. Simpler logic is used as I/O is also treated as memory only.
3.	Separate instruction control read and write operation in I/O and memory.	3. Same instructions can control both I/O and memory.
4.	It is more efficient due to separate buses.	4. It is lesser efficient
5.	Isolated I/O is larger in size due to more buses.	5. Memory Mapped I/O is smaller in size.
6.	All address can be used by the memory.	6. Due to addition of I/O addressable memory become less for memory.

7. Separate instruction control read and write operation in I/O and Memory.

7. San

Advantages of Isolated I/O

- All I/O location are addressed in exactly same manner as memory location.
Then overall size of instruction reduced.
- It is efficient
- All arithmetic/ logic operator are performed

Disadvantage of Isolated I/O

- Part of memory space is lost
- larger in size

Advantage of Memory - Mapped I/O

- larger memory address space are available
- small in size.
- Special instruction for I/O operator performance.

Disadvantage of Memory - Mapped I/O

- Data to be transferred to accumulator to perform arithmetic & logic operation
- less Efficient

Answer of Q. No 2 (c)

S.No	RAM	ROM	PROM	EPROM
1.	Stands for Random Access Memory	Stands for Read-Only Memory	Stands for Programmable Read-Only Memory	Stands for Erasable Programmable Read Only Memory
			is a type of ROM	is a type of ROM.
2.	Can read & write data.	Can only be read & can not be changed	Can only be written once	Can be repeatedly erased using UV radiation & written again
3.	Used to store the data inside the data that ROM is burned has to be in the factory currently by a special process by method in ROM CPU manufacturing temporarily	Can be written with the help of a dedicated programmer.	Can be written with the help of a dedicated programmer.	
4.	Data can be changed. Any miscalculation in data can be solved easily.	Data must be stored carefully, as if there's any miscalculation, there's any miscalculation, error or bug, it becomes unusable.	If there's any miscalculation, error or bug, while writing, PROM becomes unusable.	If there's any miscalculation, error or bug while writing it can be used once more by erasing the data.

Answer of Q. No. 2 (B)

5, 2, 23, 8, 6, 19, 23, 8, 16, 34, 4, 92, 8, 3, 16, 23, 7

Fully-associative mapping cache with 8 blocks. The diagram of cache memory will be.

0	B ₅	B ₄
1	B ₂	B ₂₂
2	B ₂₃	
3	B ₈	
4	B ₆	B ₃
5	B ₁₉	B ₇
6	B ₁₆	
7	B ₃₄	

In fully associative mapping word can be placed in any block.

When we place B₅ to B₁₉ there are no hit. So they are placed in cache.

Then B₂₃ and B₈ hit

Then B₆, B₃₄, B₄, B₂₂ miss and since LRU replacement policy is used we can't replace B₂₃ and B₈.

Therefore block 4 is present in cache block number 0.

Answer of Q. NO. 3 (B)

Instruction :- SUB (R1), R2

complete execution of any instruction is divided into 2 phases.

(a) Instruction Fetch Phase

(b) Instruction Execution Phase.

Instruction Fetch Phase

Step 1) Instruction is transferred from PC (program counter) to MAR (memory address register) and Read signal is send to memory. At some time, Select signal is sent to select constant 4 in multiplexer MUX to be added in contents of PC and stored in temporary register Z.

Step 2) contents of Z (updated instruction) is loaded into PC at WMFC (wait for memory function complete). Signal is sent to pause further execution before data is found in memory and MFCS signal to be sent.

Step 3) Once the word is found in memory MFCS signal is sent and contents

of MDR (Memory data register) into IR (Instruction Register) for continuing instruction execution phase.

Instruction Execution Phase

Step 4) Contents of register R1, is transferred into MAR, read signal is sent to search operands in location R1

Step 5) Contents of R1, (which is direct address) hence no need to search again to register 4 and WRF signal is sent

Step 6) Once the operands of R1 are found, they are transferred from MDR to input of ALU, at same time select 4 signal is sent to MUX for selecting contents of 4 (R2) to other input of ALU. Sub signal is sent to ALU for subtraction and result is stored in register Z.

Step 7) Finally the contents of Z are transferred to R2 (final location) and END signal is sent to notify that this instruction has executed and begin cycle from step 1 for next instruction.

Single Bus Data Path for this Instruction

