IInd Yr. COMPUTER ENGINEERING (A&B)

TEST-2, October 2021

CER3G1: COMPUTER ORGANIZATION & ARCHITECTURE

Duration:70min Max. Marks:20

Q1. A computer has an 4 GB memory with 32 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? 5

Q2. A block-set-associative-cache consists of total of 64 blocks divided into 4-block sets.The main memory contains 4096 blocks, each consisting of 128 words. 5

(a). How many bits are there in a main memory address?

(b). How many bits are there in each of the TAG, SET and WORD fields.

Q3. Differentiate Between ROM,PROM and EPROM.(only 5 Points in column) 5

Q4. Consider a fully associative cache with 8 blocks (0-7) and the following sequence of memory block request 5

5, 4, 3, 25, 8, 6, 9, 25, 5, 11, 3, 65, 43, 25, 8, 32,14

If LRU replacement is used, which cache block will have memory block 25? Also find the total number of hit and miss.