



Reliability Test Plan

Sample allocation by EV2 stage

Reference specification

M1071141 Rev E WCS HW Reliability Specification Hardware: WCS and Non-WCS Systems Specification



RE_ Narrow latch re qual at EV2.msg

		EV2	EV2	EV2	EV2	EV2
Baseline test on all samples (Pre-conditioning)		MaxA1 (main)	MaxA2 (2nd)	B1 (32coreMain)	B2 (32core2nd)	MB with narrow latch
Environmental (ESS - Enviromental Stress Screening)						
Non-Operational - Thermal Cycling - Deformation (Robustness)	EV	1	1 => 0	0	1	1 (with narrow MB#1)
Non-operation - High Temperature/Humidity (STORAGE) - 85/85	EV	1	1 => 0	1	1	1 (with narrow MB#2)
Non-Operational Cold & Hot Storage (-40/70°C)	EV	1	1 => 0	2	2	1 (with narrow MB#3)
Thermal profile (IR hot spots & thermo-couple temp measurements)	EV	1 => 0			1	1 (with narrow MB#4)
Electrical - HALT / Biased Power Cycling						
Operational HALT: Temperature stepping up/down to failure (Margin)	EV	1		1	1	
Operational HALT: Vibration stepping up/down to failure (Margin)	EV	1	1		1	
Operational HALT: Combined temperature & vibration change	EV		1 => 0	1	1	1 (with narrow MB#5)
Four-corner voltage/temperature (Margin)	EV	1	1 => 0	1		1 (with narrow MB#6)
Operational and non-operational Altitude tests - (Margin)	EV		1 => 0	2		1 (with narrow MB#4)
Operation - High Temperature/Humidity w/AC power cycling (RDT/DMTBF)	EV	1	1	1		
Mechanical Stresses						
Non-Operating Shock, non-packaged (board level /L10)	EV			2	1	
Non-Operating vibe, non-packaged (board level /L10)	EV			2	1	
Connector durability	EV			1	1 => 0	1 (with narrow MB#3)
High Speed Cable Requirements	EV			(1)	(1)	



N

Reliability Test Plan

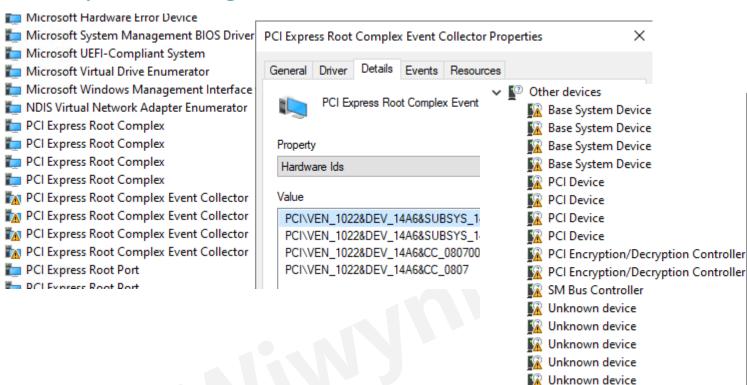
Sample arrival status

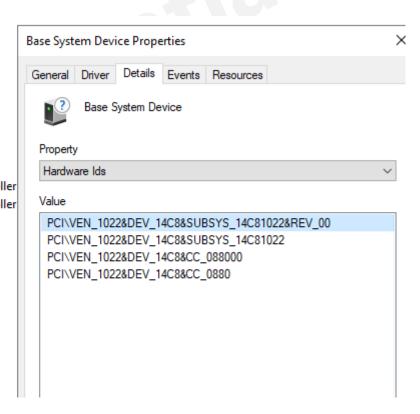
Date	SKU - A1	SKU - A2	SKU - B1	SKU - B2
2022/01/28	2	1	4	4
2022/02/15	-	-	3	3
Total	2	1	7	7

Remark: Based on PM's update, they would try to provide all samples before end of 2/18 for reliability test.

Reliability Test Plan

All yellow bang device were from AMD vendor.





Unknown device
Unknown device
Unknown device
Unknown device
Unknown device

Connector Durability

Test Item	Description / Test Condition
Connector Durability	Follow connector list to do connector insertion and extraction 30 times each.

Connector Durability

(Non-Op Test, L10 level)

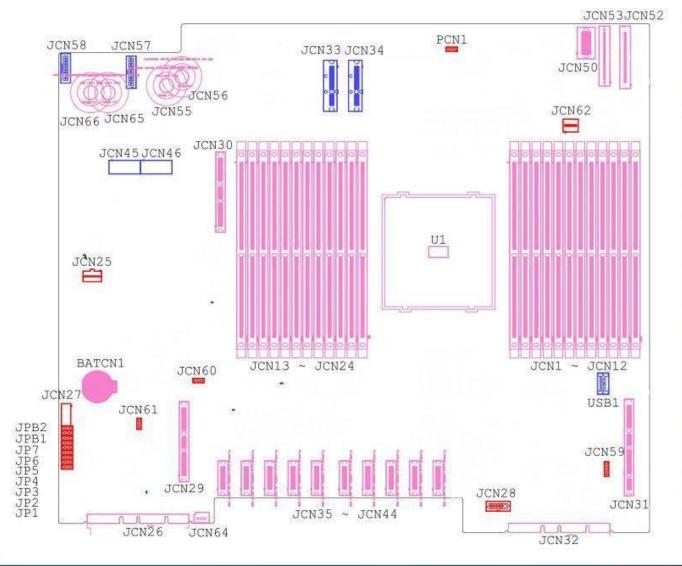
Baseline test
12 hrs

No function error

Quick test
30 mins

Connector Durability

Test cover all connectors.



Note:

- 1. Pink: New
- 2. Blue: Leverage C2080
- 3. Red: Debug use

New part function introduction:

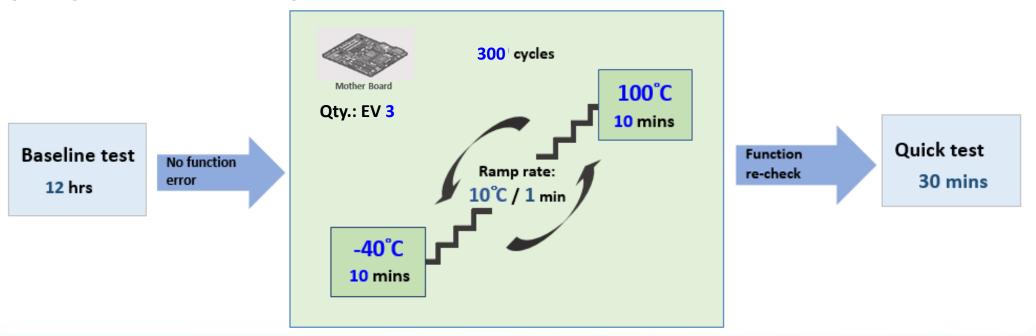
- 1.JCN55, JCN56, JCN65, JCN66
- -> Rapid lock (PSU power connector)
- 2.JCN50
- -> 12V power connector for 2U PDB
- 3.JCN53
- -> 1U/2U singal rotor fan connector
- 4.JCN52
- -> 1U dual rotor fan connector
- 5.JCN29, JCN30
- -> 4C 140P connector for PCIe x16
- 6.JCN31
- -> 4C+ 168P connector for PCIe x16
- 7.BATCN1
- -> Battery holder
- 8.JCN1 ~ JCN24
- -> DDR5 DIMM socket
- 9.U1
- -> SP5 CPU socket
- 10.JCN35 ~ JCN44
- -> 1C 56P connector for EDSFF x4
- 11.JCN26, JCN32
- -> 4C+ 168P connector for SCM, OCP NIC
- 12.JCN64
 - -> Intrusion header

Thermal Cycling

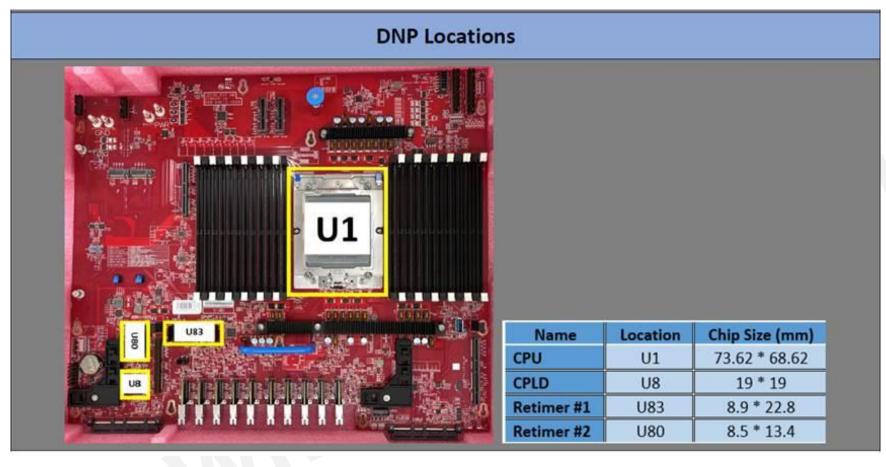
Test Item	Description/ Test Condition
Thermal Cycling (non-operating) Ref: JESD22-A104 JESD22-A106	Thermal cycling from -40°C to 100°C. Ramp rate: 10°C/min. Soaking at each temperature extreme for a minimum 10min or until thermal equilibrium is reached. Total 300 cycles
	 Functional test at room temperature. Dye and Pry and/or cross section critical components at the end of the test.

Thermal Cycling

(non-operational & PCBA level)



Thermal Cycling – DnP location



Follow standard - IPC-9704:

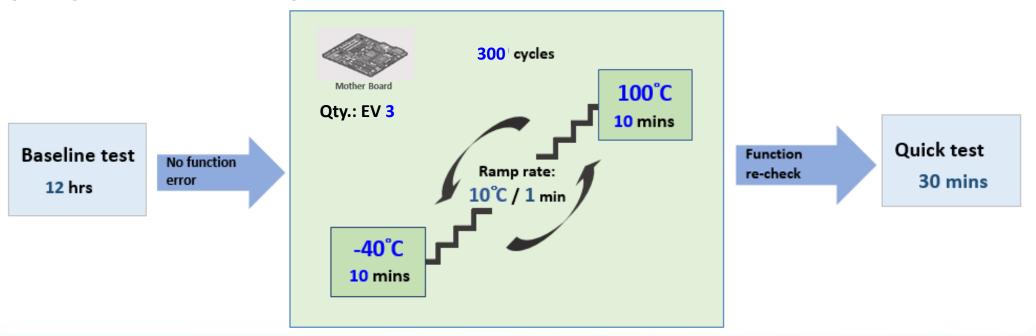
3.2.1 Area Array Components It is recommended that any area array device with a package body size equal to or larger than 27 x 27 mm or finer pitch components (0.8 mm pitch and below) with body size > 10 mm should be evaluated. If there are several fine pitch components, then, at a minimum, the three worst case locations should be tested based on engineering judgment, history of damage, or finite element analysis.

Thermal Cycling

Test Item	Description/ Test Condition
Thermal Cycling (non-operating) Ref: JESD22-A104 JESD22-A106	Thermal cycling from -40°C to 100°C. Ramp rate: 10°C/min. Soaking at each temperature extreme for a minimum 10min or until thermal equilibrium is reached. Total 300 cycles
	 Functional test at room temperature. Dye and Pry and/or cross section critical components at the end of the test.

Thermal Cycling

(non-operational & PCBA level)

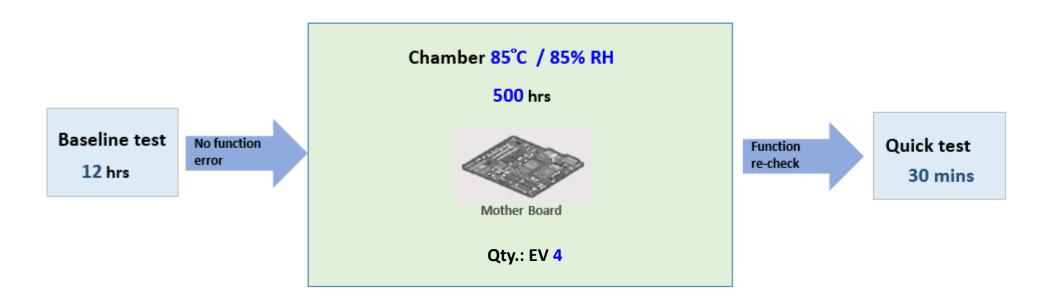


High Temperature / Humidity (Storage) - 85/85

Test Item	Description/ Test Condition
Storage (non-operational): High Temperature/ Humidity Ref: JESD22-A103	85°C / 85%RH for 500hrs for connectors. Follow proper temperature and humidity ramping procedures to avoid condensation on Device under test (DUT)

Storage High Temperature/Humidity

(non-operational & PCBA level)



Cold and Hot Storage

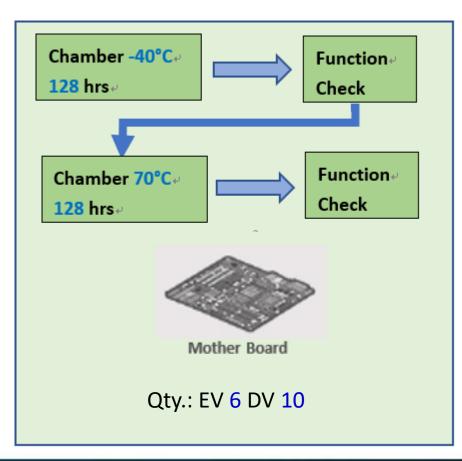
Test Item	Description / Test Condition
Cold and hot storage (Ref. JEDEC JESD22-A119)	 Cold and hot temp. for a minimum of 128hrs at each temp. Test temperature: -40°C and 70°C

Cold and hot storage

(Non-op Test, PCBA level)

Baseline test
12 hrs

No function
error

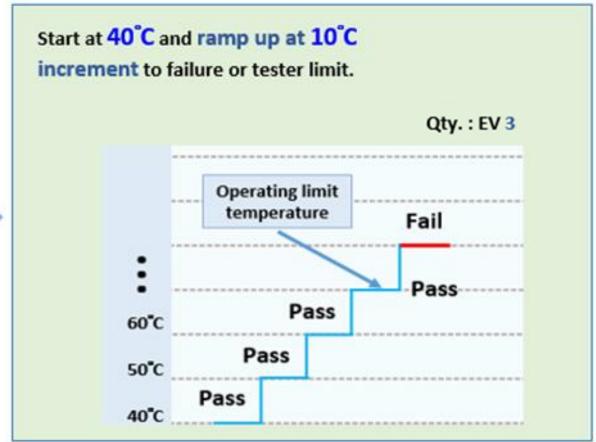


TV.

HALT (UOL)

Test Item	Description/ Test Condition
Operational HALT: Upper Operational Limit (UOL)	Start at 40°C and ramp up at 10°C increment to failure or tester limit.

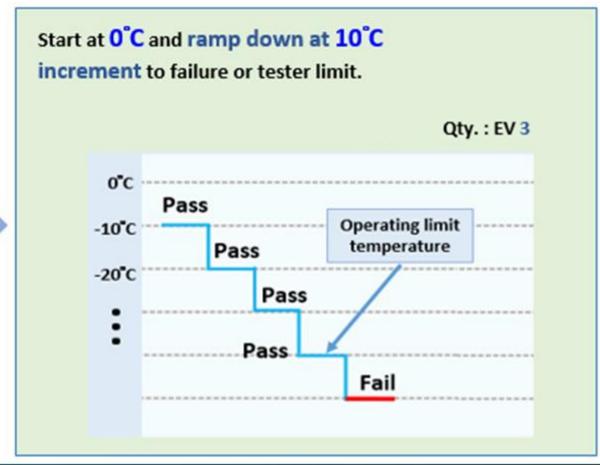




HALT (LOL)

Test Item	Description/ Test Condition
Operational HALT: Lower Operational Limit (LOL)	Start at 0°C and ramp down at 10°C increment to failure or tester limit.

Baseline test
12 hrs
No failures

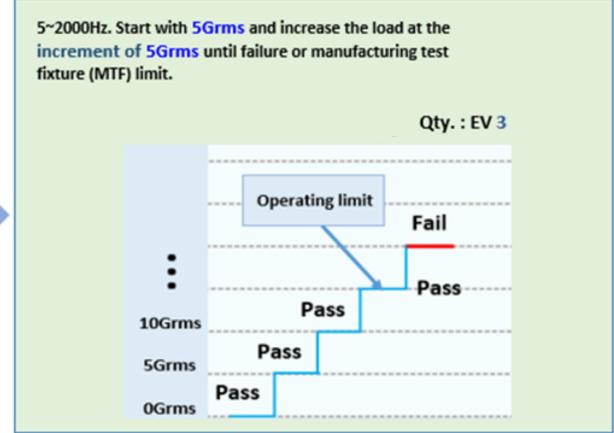


W

HALT (VOL)

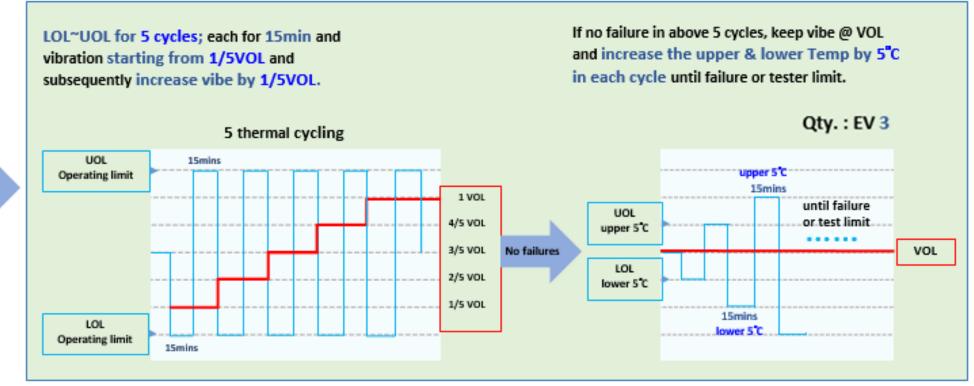
Test Item	Description/ Test Condition
Operational HALT: Vibration	5~2000Hz. Start with 5Grms and increase the load at the increment of 5Grms until failure or manufacturing test fixture (MTF) limit.





HALT (Combined)

Operational HALT: Combined @ 1st cycle and subsequen	wel at LOL and UOL for 15min and vibration starting from 0.2VOL
5°C in each cycle until failur	rly increase vibe by 0.2VOL . Voles, keep vibe @ VOL and increase the upper & lower Temp by e or tester limit.



No failures

Baseline test

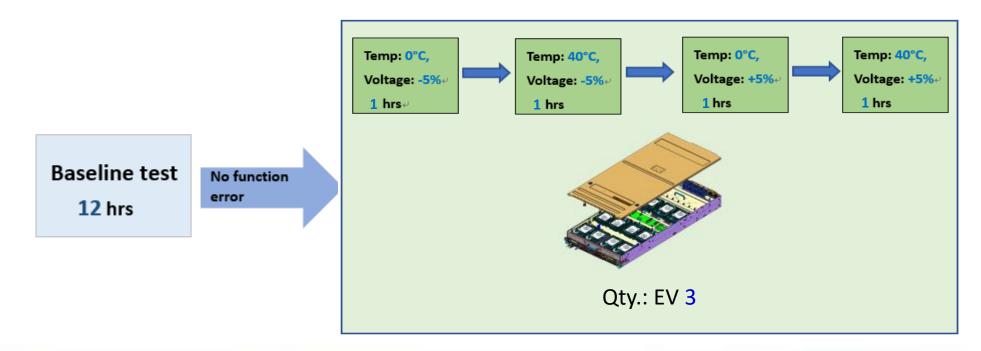
12 hrs

Four Corner

Test Item	Description / Test Condition
FOUR-CORNER VOITAGE/TEMN (MARGIN)	To ensure motherboard work normally at high & low temperature (0°C , 40°C) and \pm 5% voltage bias limit.

Four-corner voltage/temp (margin)

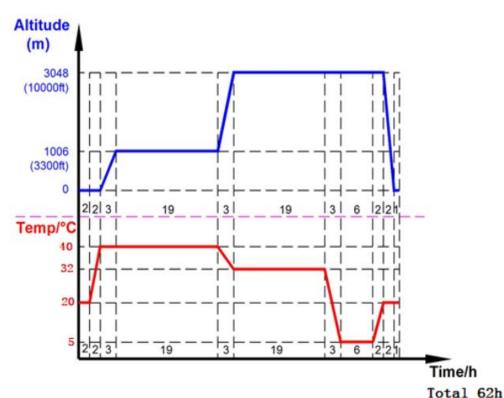
(Operational Test, L10 level)



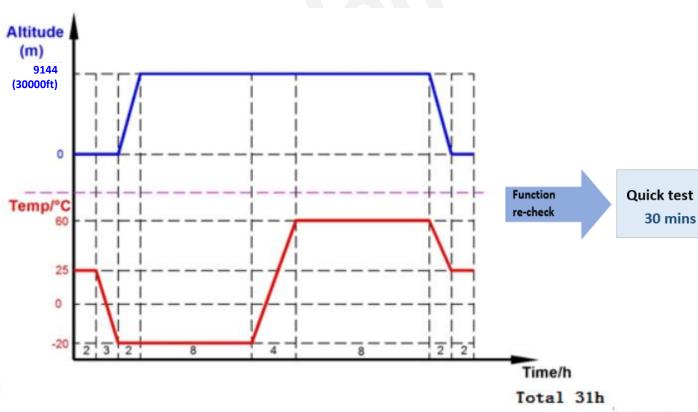
Operational and Non-operational Altitude Tests

	Test Item	Description / Test Condition
•	nai and Non-operational Altitude Tests	 Operating – 3,300 ft & 10,000 ft maximum with 5°C, 32°C and 40°C Non-operating – 30,000 ft maximum with -20°C and 60°C Rate of change less than 1500 ft./min (457m/min)

Operating Altitude Test



Non-Operating Altitude Test

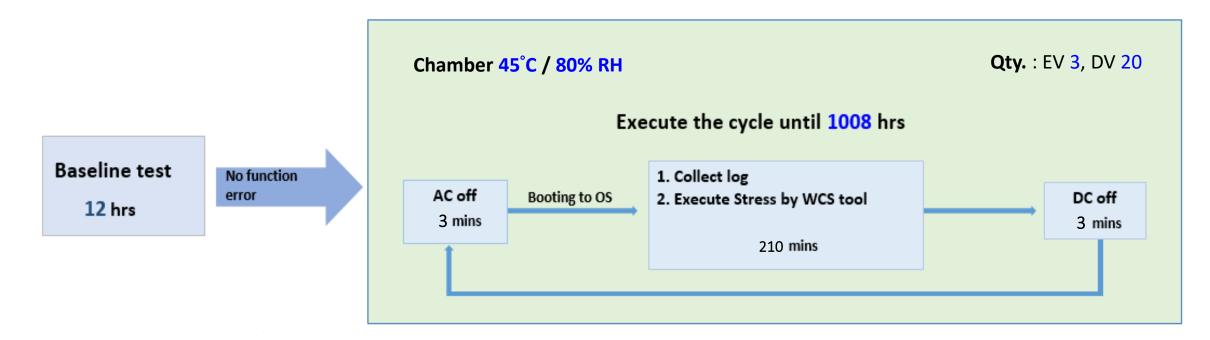


Qty.: EV 3

RDT – Reliability Demonstration Test

Test Item	Description / Test Condition
RDT (Ref. JESD22-A101/102)	45°C/80%RH @ nominal power input & max. workload for 1008hrs

Operational High Temperature/Humidity with AC Power Cycling (RDT)







Back Up