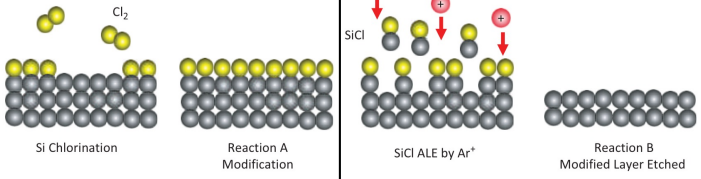
Atomic Layer Etching

Cl_2 (g) + Si (s) ➔ $SiCl_x$ (s)



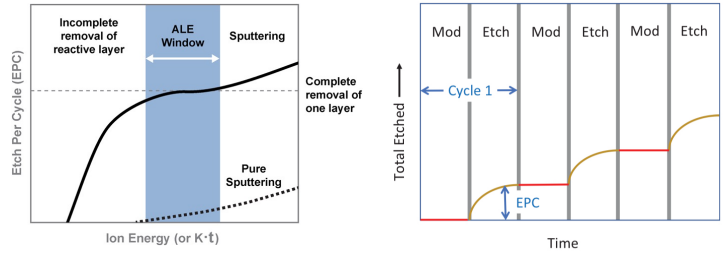
Cl_2 introduction
Chemisorption to saturation
Purge of Cl_2

Ar plasma
Selective removal of the surface layer

Purge of Ar

Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023

Atomic Layer Etching (2)



K. J. Kanarik et al., J. Vac. Sci. Technol. A. 2020;39(1). doi:10.1116/6.0000762

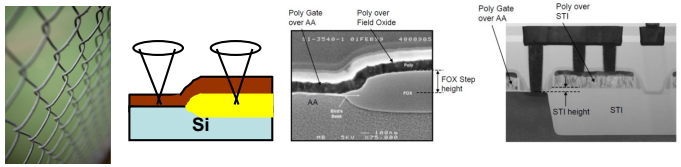
Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023

Chemical Mechanical Planarization or Chemical Mechanical Polishing (CMP)

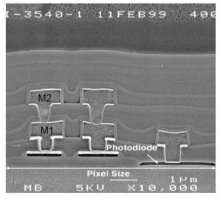
- CMP involves removal of materials by a combination of chemical and abrasive action to achieve highly planar surfaces that are also very smooth
- CMP processes aim to minimize and eliminate direct material removal either by mechanical abrasion or by chemical etching.

M. Krishnan et al., Chem. Rev. 2010, 110, 1, 178–204

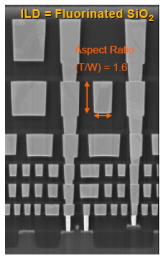
Why Planarize?



Another example is backend interconnect.

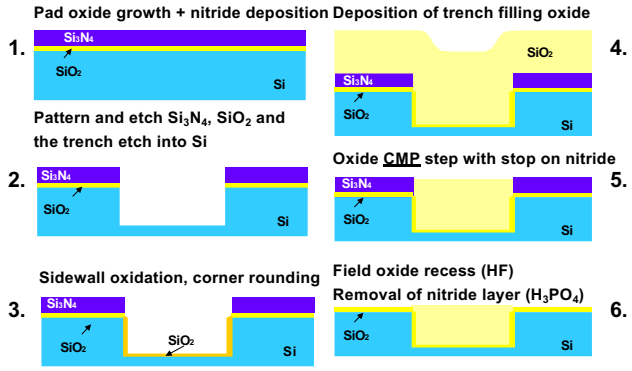


metal6
via5
metal5



Shauly, E.N.; Rosenthal, S,. *J. Low Power Electron. Appl.* **2021**, *11*, 2.

Shallow Trench Isolation (STI)



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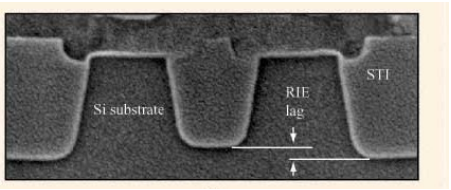
STI: Shallow Trench Isolation



Agnello, IBM Journal of research and development, no. 2/3 2002

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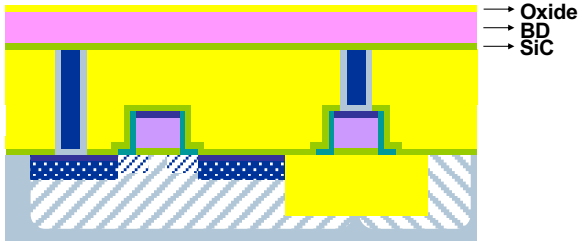
Copper Single Damascene



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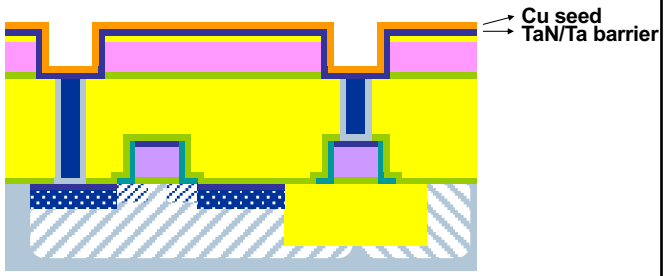
Copper Single Damascene (2)



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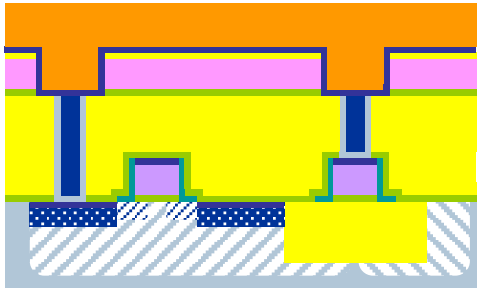
Copper Single Damascene (3)



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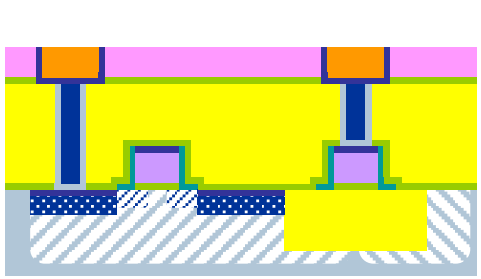
Copper Single Damascene (4)



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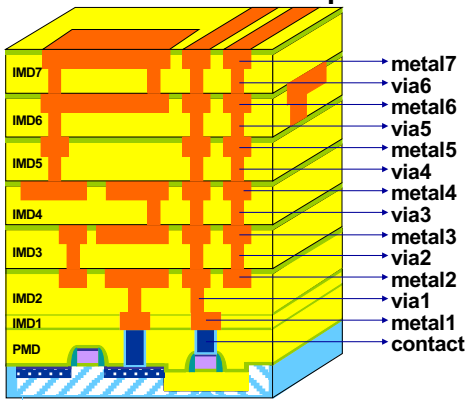
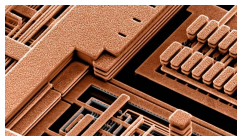
Repeat





Courtesy: IBM

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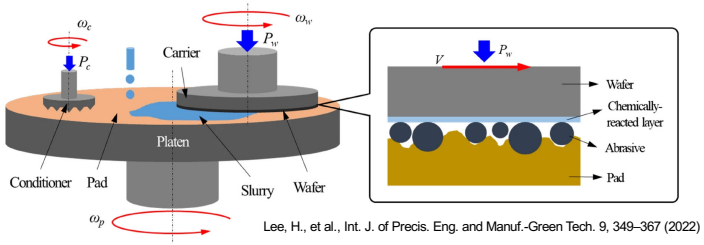
CMP process and material removal mechanism



Lee, H., et al., Int. J. of Precis. Eng. and Manuf.-Green Tech. 9, 349–367 (2022)

Slurry:

Abrasives: silica, alumina, ceria, ….
Chemicals for pH control, surfactants, dispersants,…

Pads:

Polymers

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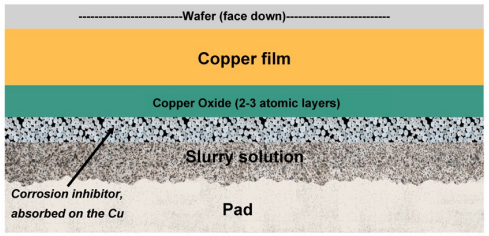
CMP process and material removal mechanism

Oxide CMP: $(SiO_2)_x + 2H_2O \rightleftarrows (SiO_2)_{x-1} + Si(OH)_4$

Copper CMP:



Shauly, E.N.; Rosenthal, S,. *J. Low Power Electron. Appl.* **2021**, *11*, 2.

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Applications of CMP in ULSI

- Polishing of silicon wafer after cutting of ingot
- Shallow trench isolation
- Replacement gate process
- Planarization of pre-metal and interlayer dielectrics (between metals)
- Removal of W, TiN/TaN layers (tungsten plug process)
- Copper damascene process
- …..

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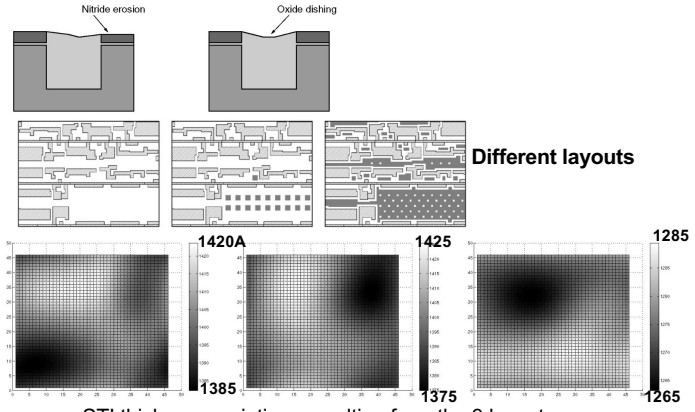
Challenges: dishing and erosion, e.g. STI



STI thickness variations resulting from the 3 layouts

Kang et al., Proc. 2006 International Conference on Computer-Aided Design (ICCAD'06), November 5-9, 2006

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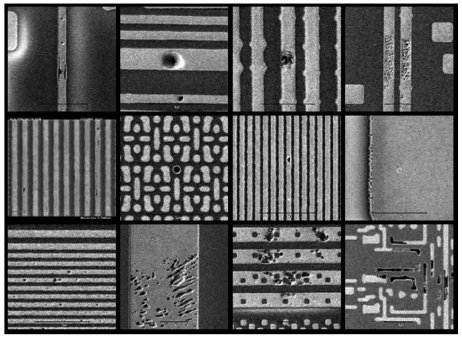
Challenges: Corrosion



Various forms of corrosion in Cu CMP.

M. Krishnan et al., Chem. Rev. 2010, 110, 178-204

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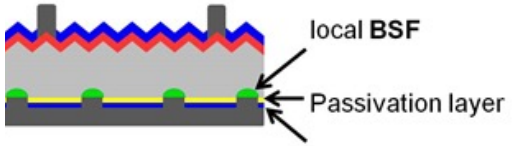
Process integration for device fabrication: silicon solar cell

Passivated emitter and rear contact (PERC) solar cell



Passivation layer

SiN_x capping layer

Exercise:

Write a process sequence for the fabrication of the device.