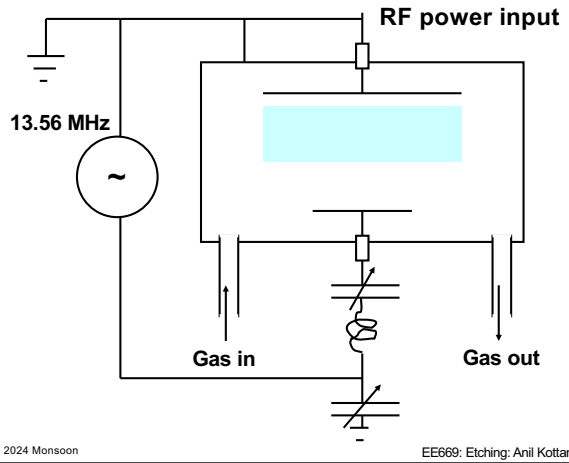
Dry Etch or Reactive Ion Etch



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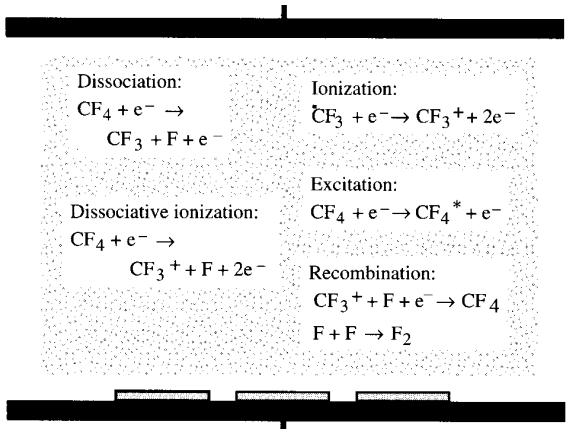
Dry Etch or Reactive Ion Etch: Si etch



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Types of Etch

Classification

- **Chemical etch:**
  - **caused by chemical reaction of the free radicals like F, CF3, … with materials on the wafer surface**
  - **isotropic, highly selective**
- **Physical etch:**
  - **caused by bombardment of high energy ions on the wafer surface**
  - **anisotropic, not selective**
- **Ion enhanced etch:**
  - **ions and free radicals acting together**
  - **anisotropic and selective**

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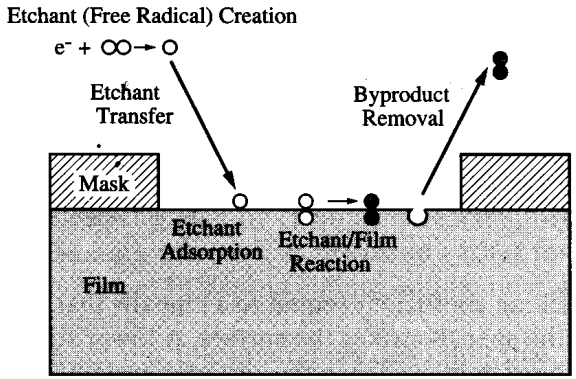
Chemical Etch Process



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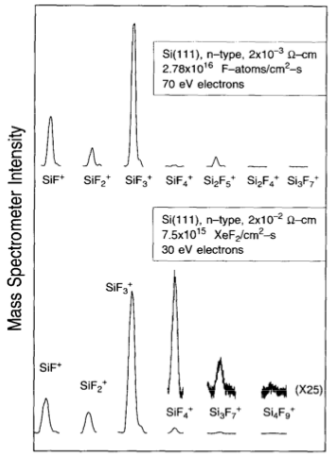
Chemical Etch Process: Si – F system



Si related species observed in the plasma:

- **SiF**
- **SiF_2**
- **SiF_3**
- **SiF_4**
- **Si_2F_5**
- **Si_2F_4**
- **Si_3F_7**
- **Si_4F_9**

H. F. Winters and J. W. Coburn, Surface Science Reports, 14 (1992), 161- 269

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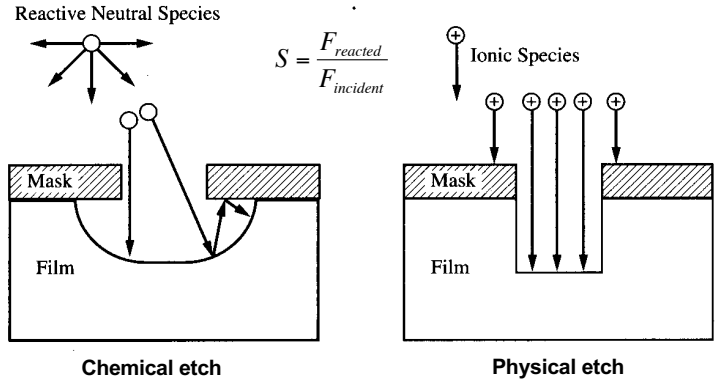
Chemical versus Physical etch



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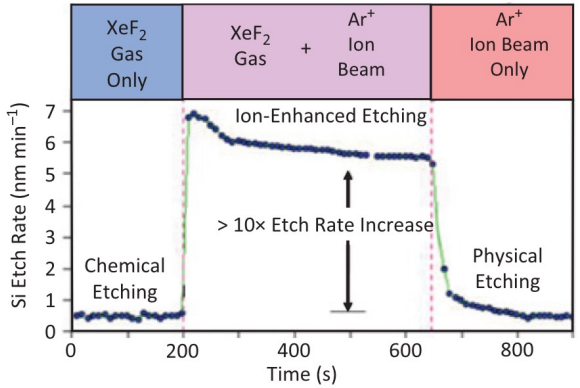
Ion Enhanced Etch



Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023

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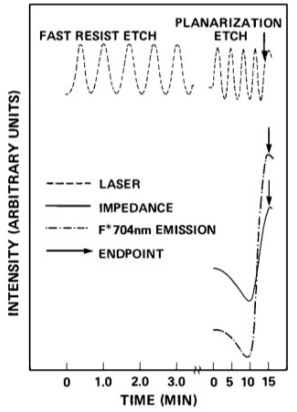
End Point Detection in RIE



$CF_4 + O_2$ plasma for resist etch

photoresist
SiO_2
Si

- **Laser interferometry: measure thickness of the remaining material**
- **Measure the optical emission corresponding to atomic fluorine**
- **Measure the plasma impedance**

J. P. Roland et al., Journal of Vacuum Science and Tech. A., 3, 631, (1985)

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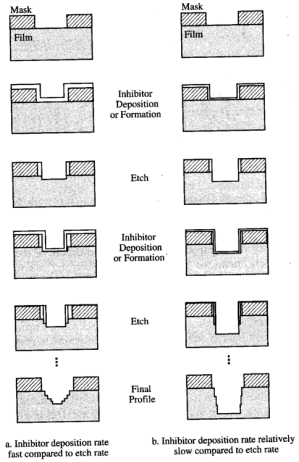
Reactive Ion Etch: Role of Inhibitors



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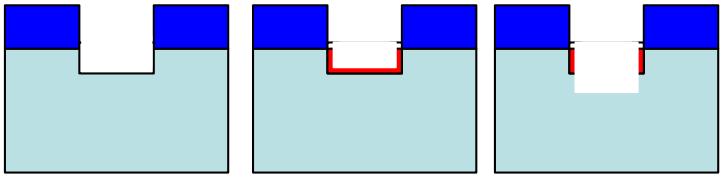
Reactive Ion Etch: Bosch process



SF6 plasma etching (physical and chemical)

C4F8 plasma exposure Thin fluoro carbon deposition

SF6 plasma etching (physical and chemical)

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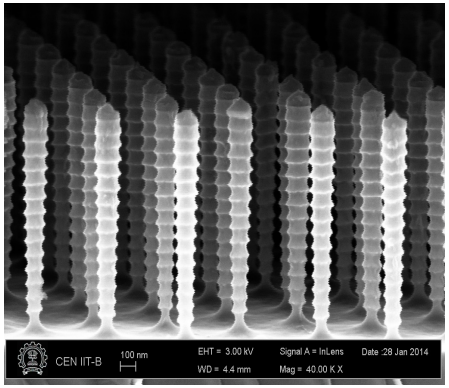
Reactive Ion Etch: Bosch process



Sreejith K. P., M. Tech thesis, NCPRE/EE, 2016

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Self Study: All Dry Etch Processes Described in Plummer

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Case Study: Poly-Si Etch for Small Gate Length

Resist trim: Isotropic etching of the resist to reduce the feature size in resist

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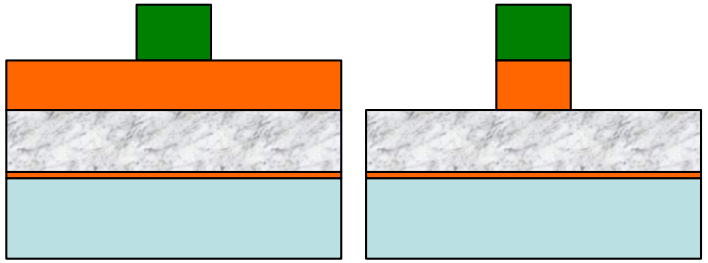
Case Study: Poly-Si Etch for Small Gate Length



Hard mask etch and in-situ resist strip: Transfer the pattern to hard mask

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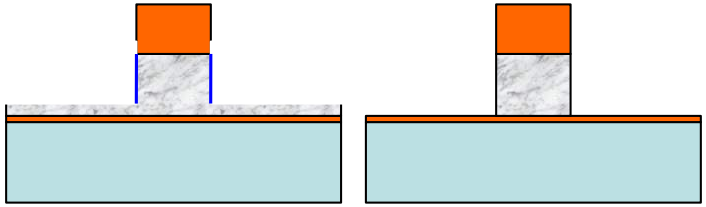
Case Study: Poly-Si Etch for Small Gate Length



Poly-Si etch, step 1: Straight 90° profile, highly anisotropic etch, side walls protected by inhibitors

Poly-Si etch, step 2: More isotropic etch, highly selective

Step 3: Oxide HM etch in HF

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Case Study: Poly-Si Etch for Small Gate Length

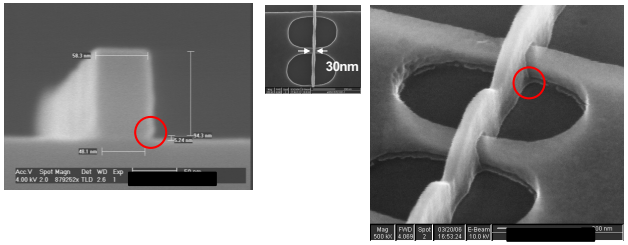

Image courtesy: IMEC

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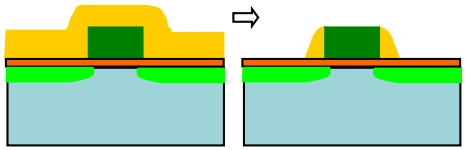
Case Study: Spacer Etch



- Typical spacer used in VLSI: Si_3N_4
- Poor etch selectivity between Si_3N_4 and Si
- So a SiO_2 liner is used between the nitride and Si
- Anisotropic etching of Nitride ➔ same thickness etched everywhere in the vertical direction

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Case Study: Spacer Etch

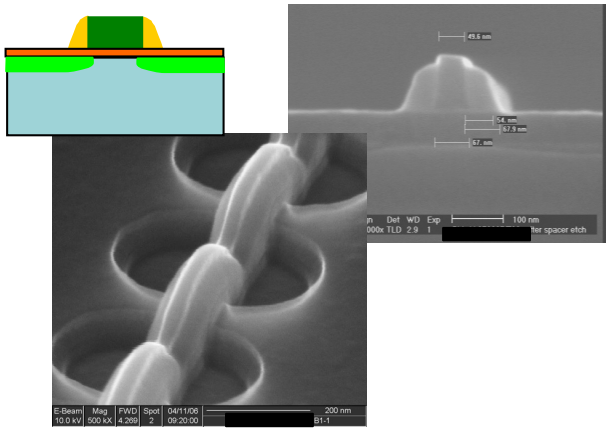

Image courtesy: IMEC

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Resist Strip After Etch

- Subsequent to etch, photoresist used as mask (if at all) should be removed
- The resist hardens during exposure to plasma
  - Due to temperature increase, chemical or physical transformation in the resist
  - Chemical and physical transformation of the resist due to interaction with plasma
- Oxygen plasma treatment to burn the resist: CO and CO_2 are produced
- Wet chemical etch
  - H_2SO_4:H_2O_2 etch (piranha clean or SPM)
  - NH_4OH:H_2O_2:H_2O etch (APM)
- Usually a combination of dry strip (O_2 plasma) and wet strip are used.

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