Si Wafer Manufacturing

- Si – 2nd most abundant material on earth's crest (~ 28%)
- But in the form of SiO_2 – quartz – sand (SiO_2 + impurities)
- VLSI grade: impurity levels typically ppb or 10^{13} cm^{-3} (~10^{15} cm^{-3} carbon & 10^{18} cm^{-3} oxygen are acceptable in certain applications)
- Single crystal is required for electronic and photovoltaic applications
- Desired resistivity (doping) and orientation
- Required in the shape of circular wafers for VLSI and square for solar cells
- Mechanical properties
  - smooth mirror finish top surface (lithography and interfaces) for VLSI. As-cut, rough surface for solar cells
  - minimal bow and taper
  - thickness of the wafer to give mechanical strength

Quartz to Metallurgical Grade Silicon

~ 2000C & 13 kWh/kg

SiO_2 + 2 C ➔ Si + 2CO

quartzite coke /coal

Metallurgical grade ~ 98% purity

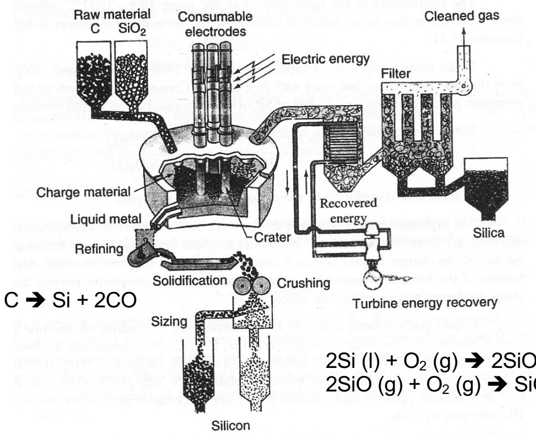
Typical impurities in metallurgical grade Silicon (in ppm by weight)

O:100 – 5000	V: 1 - 300
Fe: 300 – 5000	B: 5 – 70
Al: 300 – 5000	P: 5 – 100
Ca: 20 – 2000	Cu: 5 – 100
C: 50 – 1500	Cr: 5 – 150
Mg: 5 – 200	Ni: 10 – 100
Ti: 100 – 1000	Zr: 5 – 300
Mn: 10 – 300	Mo: 1 – 10

The use of metallurgical grade silicon:
38% for aluminum alloys, 37% by chemical industry for various silicones etc., 25% by PV (22%) and VLSI(3%) industries.

1. Luque and S. Hegedus, Handbook of Photovoltaic Science and Engineering, Wiley, 2011
2. Guo et al., An overview of the comprehensive utilization of silicon-based solid waste related to PV industry, Resources Conservation and Recycling, 2021

Arc furnace for metallurgical grade silicon production



SiO_2 + 2 C ➔ Si + 2CO

2Si (l) + O_2 (g) ➔ 2SiO (g)
2SiO (g) + O_2 (g) ➔ SiO_2 (g)

A. Luque and S. Hegedus, Handbook of Photovoltaic Science and Engineering, Wiley, 2011

Metallurgical grade to electronic grade silicon

Si + HCl

MGS, powder

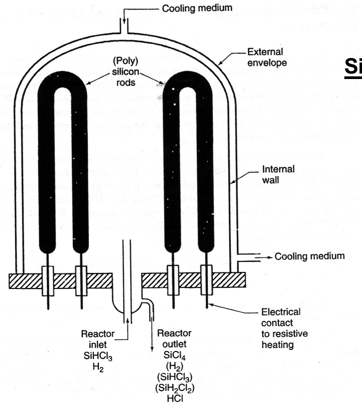
➔ SiH_4 + Cl_2
➔ SiH_3Cl + Cl_2
➔ SiH_2Cl_2
➔ $SiHCl_3$ + H_2
➔ $SiCl_4$ + H_2

High temperature

catalysts

Further purification by fractional distillation
Silane is a gas at room temperature, boiling point of -112C
SiH_3Cl : boiling point -30.4C
SiH_2Cl_2 : boiling point 8.3C
$SiHCl_3$: boiling point 33C
$SiCl_4$: boiling point 57.6C

Siemens process for production of electronic grade Silicon



Siemens process reactions

$SiHCl_3 + H_2 \rightarrow Si + 3HCl$
$2SiHCl_3 \rightarrow SiH_2Cl_2 + SiCl_4$
$SiH_2Cl_2 \rightarrow Si + 2HCl$
$HCl + SiHCl_3 \rightarrow SiCl_4 + H_2$

90 % energy lost to the cold walls

Purity of poly-Si obtained: 11' 9s

Single crystal wafers required.

A. Luque and S. Hegedus, Handbook of Photovoltaic Science and Engineering, Wiley, 2011

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Si Ingot Manufacturing

- Two techniques for fabrication of single crystal Si ingots
  - Czochralski method
    - Large ingot diameter possible
    - High Oxygen (~10^{18} cm^{-3}) and Carbon (~10^{15} cm^{-3}) content
    - Most electronic grade silicon made by Cz process
  - Float-Zone method
    - Smaller ingots
    - Low impurity concentrations
    - High resistivity wafers
      - Detectors (dark current in photodiodes)
      - Power semiconductor devices (breakdown voltage)
      - Highest efficiency solar cells (dark current)
- Purification by concentration change by segregation during the liquid – solid transition

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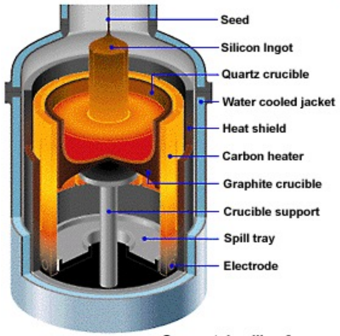
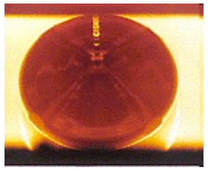
Si Ingot Manufacturing (2)

Czochralski Method



Cz crystal pulling furnace

Chunk polysilicon in melt phase



http://www.processpecialties.com/siliconp.htm http://www.memc.com/co-as-description-crystal-growth.asp

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Dopant incorporation in the crystal in the CZ process

Segregation

Due to different solubilities of the dopant (or impurity) in the solid and liquid phases, the dopant would segregate to the phase in which the solubility is higher

$$\frac{C_S}{C_M} = K\left(1 - \frac{W}{W_M}\right)^{K-1}$$

Where,
- C_L is the concentration by weight of the dopant in the liquid at time "t"
- C_S is the concentration by weight of the dopant in the solid at time "t"
- The segregation coefficient K is defined as $K = \frac{C_S}{C_L}$
- W is the weight of the crystal grown in time "t"
- W_M is the initial weight of the melt

See supplementary slides for derivation

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Dopant incorporation in the crystal in the CZ process (2)

Segregation coefficient of common dopants & impurities of interest in Si

Impurity	Segregation coefficient
As	0.3
C	0.07
O	0.5
P	0.35
Sb	0.023
Al	2.8×10^{-3}
Ga	8×10^{-3}
B	0.8
Au	2.5×10^{-5}

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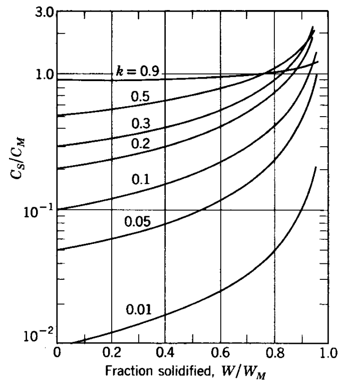
Dopant incorporation in the crystal in the CZ process (3)



Exercise: Assuming that the initial concentration of the dopant in the melt is 10^{16} cm^{-3}, calculate and plot the doping concentration along the length of a Si Cz ingot of 12-inch diameter and 2 meters tall, for the following dopants or impurities:

B, Ga, P, Au

S. K. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, 2nd ed., John Wiley and Sons, 2008

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Oxygen incorporation in the crystal during the Cz process

- In CZ process, oxygen dissolves into the melt from the quartz crucible
- Typical concentrations are in the range of $5 \times 10^{17} – 10^{18}$ cm^{-3}
- There are four effects of oxygen in silicon, two of which are discussed below. For the rest, please see supplementary information.

1. Oxygen donors:
   - SiO_4 complexes which act like donors.
   - Can increase the resistivity of lightly p-type doped Si by compensation.
   - Forms in the temperature range of 400 – 500 ^{0}C and is unstable above 500 ^{0}C
2. Oxygen forms complexes with boron, which are efficient recombination centers

J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001

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Carbon incorporation in the crystal during the CZ process

- In CZ process, oxygen dissolves into the melt from the quartz crucible and some of the oxygen would form SiO which is then evaporated from the surface of the melt
- SiO reacts with the graphite parts to form CO which gets dissolved in the melt and gets incorporated in the crystal
- Typical concentrations are in the range of 10^{16} cm^{-3}
- The following C related effects are possible in Si

1. C is a group 4 atom and hence can occupy a substitutional site without any harm
2. C is smaller than Si so there is a local contraction at the site. Oxygen precipitation results in local expansion.
   - So the precipitation of C and SiO_2 can go hand in hand
   - It would be difficult to create oxygen free regions in the wafer which has large C concentration

J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001

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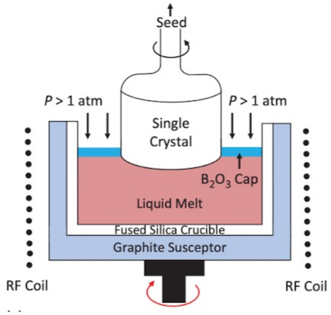
Liquid Encapsulated Cz Process for GaAs & InP



- GaAs melts at 1240℃, As preferentially evaporates compared to Ga
- B_2O_3 melts at 460℃
- InP melts at 1062℃, P preferentially evaporates compared to In

Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023.

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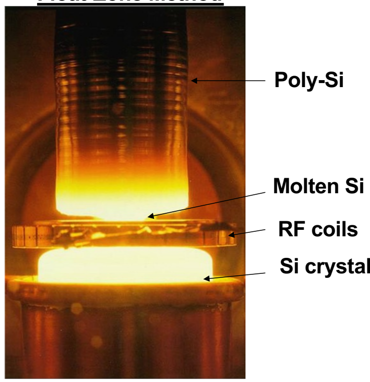
Si Ingot Manufacturing (3)

Float-Zone Method



- **EGS (poly-Si) rods**
- **No crucibles**
- **Heating by Eddy currents**
- **Low contamination**

http://www.topsil.com/410

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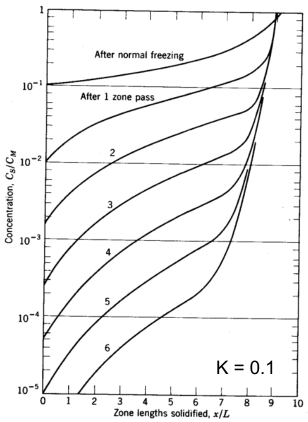
Impurity segregation in the crystal during the FZ process

- An analysis similar to that in CZ process can be carried out.
- The rod can be subjected to more than one zone refining pass which result in highly pure material at one end of the rode
- Reasonably uniform doping of the crystal can be obtained by a reverse pass after the initial pass for crystallization



S. K. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, John Wiley and Sons, 1983

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Doping of the FZ ingots

- If the initial poly-Si rod has a uniform doping, reasonably uniform doping of the crystal can be obtained by a reverse pass after the initial pass for crystallization
- Carrying out the process in an ambient containing diluted gaseous compounds of the dopants like PH_3, B_2H_6 can be used for doping of the crystal
- Neutron transmutation doping: Si contains native ^{30}Si isotope (~ 3%), part of which can be converted to ^{31}Si by neutron radiation. ^{31}Si decays to ^{31}P with a half life of 2.62 hrs. 5 – 10 Ω cm doping can be achieved.

S. K. Ghandhi, VLSI Fabrication Principles – Silicon and Gallium Arsenide, John Wiley and Sons, 1983

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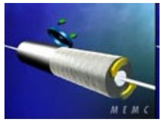
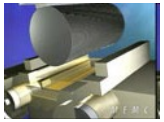
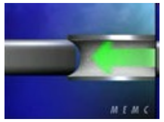
Si Wafer Manufacturing for VLSI (4)


Grinding the ingot

Flats or notches are ground on the ingot


Wafer slicing


Edge profiling

Kerf loss of ~ 60 μm

https://youtu.be/innXZa_hWq4?si=i_YYmlznj1H-FN3k
Accessed 2024

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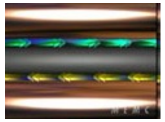
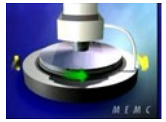
Si Wafer Manufacturing for VLSI (5)


Wafer lapping
Al_2O_3 + water + glycerine
Removes bow & taper
Flat wafer

Si etch
HNO_3 + HF +
acetic acid
Removes
mechanical
damage


Wafer polish
NaOH + SiO_2
CMP
Mirror finish


Epitaxy
High quality Si
on top for devices

http://www.memc.com/index.php?view=Process-Animations-
Accessed in 2013.

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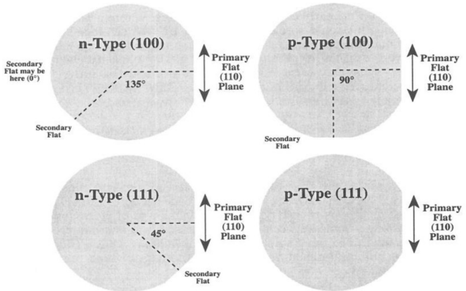
Primary and secondary flats on silicon wafers



- Flats are not universal standards
- It is likely that you find wafers of the above kind with just one flat
- Wafers above 6" diameter typically do not have flats, instead they have a notch.

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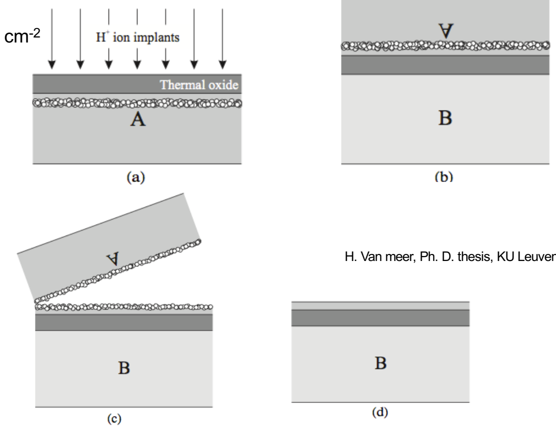
Silicon on insulator (SOI) wafers

- Smart-cut

5×10^{16} cm^{-2}



500°C

H. Van meer, Ph. D. thesis, KU Leuven, 2002

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