EE 669 VLSI TECHNOLOGY

ASSIGNMENT 4:

SOLUTION OF EXERCISE QUESTIONS LECTURE 14-23
OPTOLITHIUM SIMULATIONS
PROBLEM 10.4 ICF-SAT PLUMMER GRIFFIN

KARTIK CHIKKANAGOUDAR

21D170023

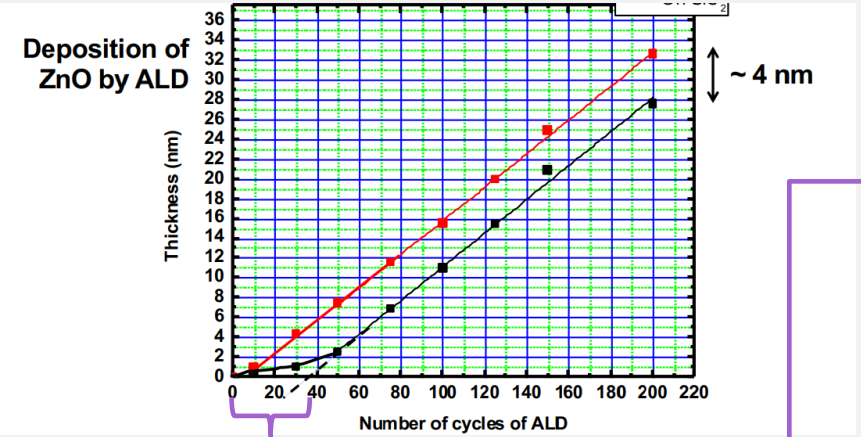
EXERCISE ANSWERS

L14- S5

Thin film and material	Deposition process
Pad Oxide : SiO2	Wet thermal oxidation
Silicon Nitride : Si3N4	Chemical Vapor Deposition
Photoresists at any step	Spin coating
Trench oxide (SiO2)	Chemical Vapor Deposition
Poly-Silicon (Poly-Si) Gate	Low-pressure chemical vapor deposition (LPCVD)
Spacer Dielectric (Oxide and Nitride layers)	Conformal deposition via Plasma-Enhanced Chemical Vapor Deposition (PECVD)
Silicide Formation (Ti, Co/Ti, Ni)	Metal sputtering followed by Rapid Thermal Processing (RTP) for silicidation
Interlayer Dielectric (SiO_2)	Plasma-enhanced chemical vapor deposition (PECVD)
Nitride Etch Stop Layer (Si_3N_4)	Plasma-enhanced chemical vapor deposition (PECVD)
Barrier Layer (TiN, WN)	Sputtering or Atomic Layer Deposition (ALD)
Tungsten (W) Deposition	Sputtering or Atomic Layer Deposition (ALD)
Barrier Layer (TaN, Ta)	Sputtering or Atomic Layer Deposition (ALD)
Copper Seed Layer	Sputtering
Copper Interconnect	Electroplating

EXERCISE ANSWERS

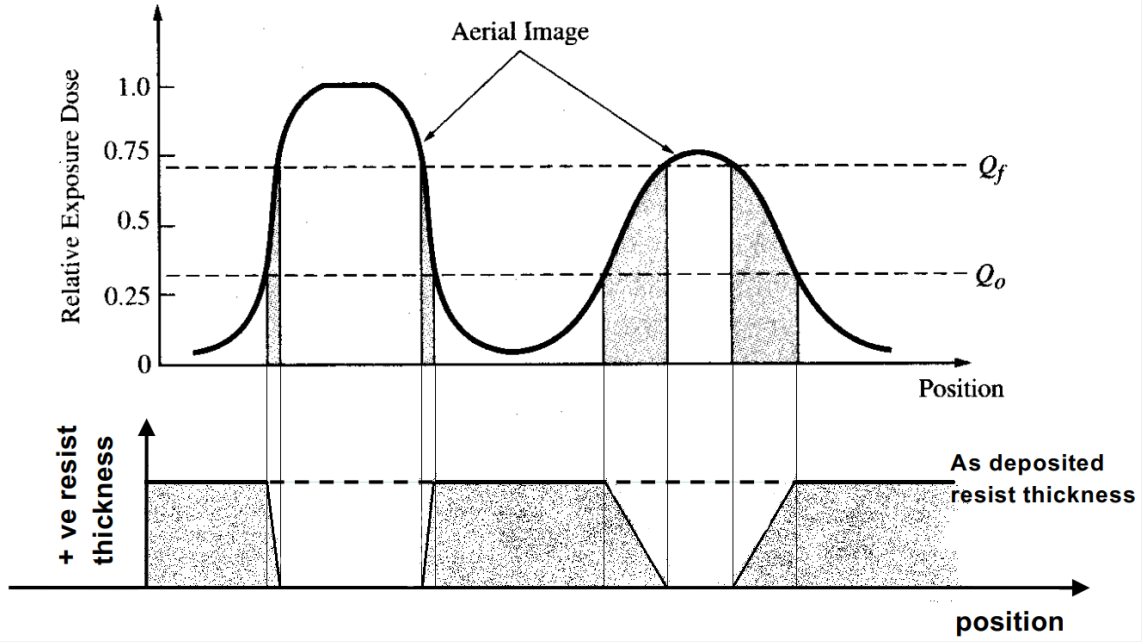
L15- S24



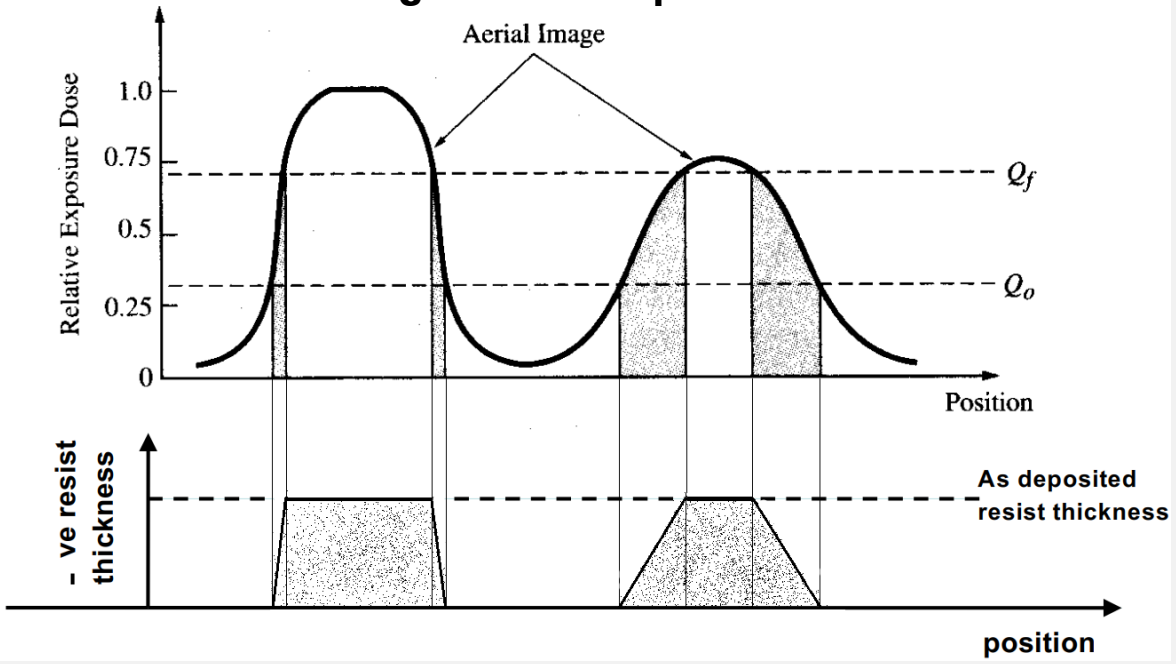
Nucleation delay (in no of cycles) ≈ 40 cycles

L23- S4

Positive resist profile

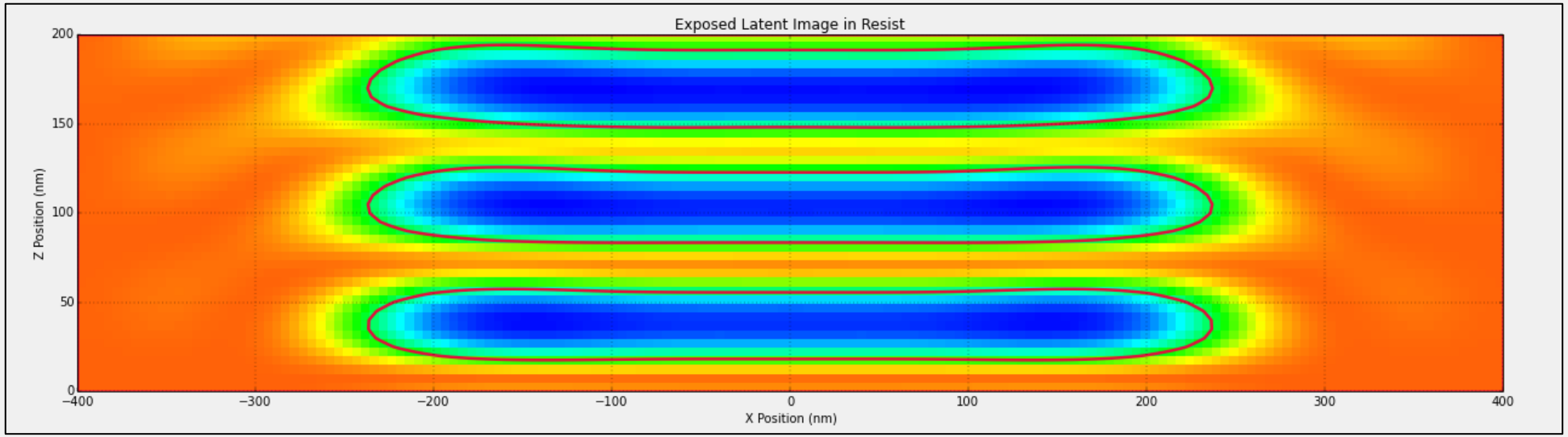


Negative resist profile

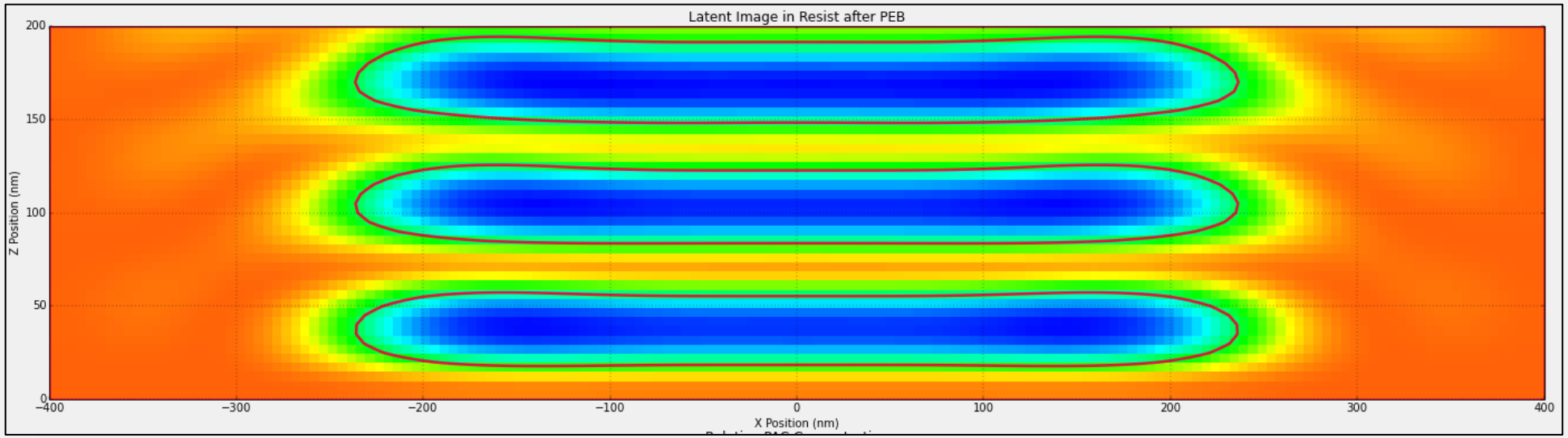


OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 1 sec

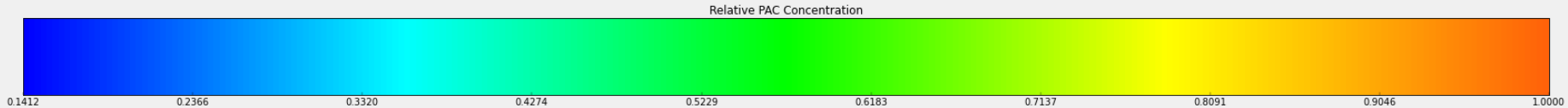


Standing waves seen in PAC concentration in resist after exposure to light



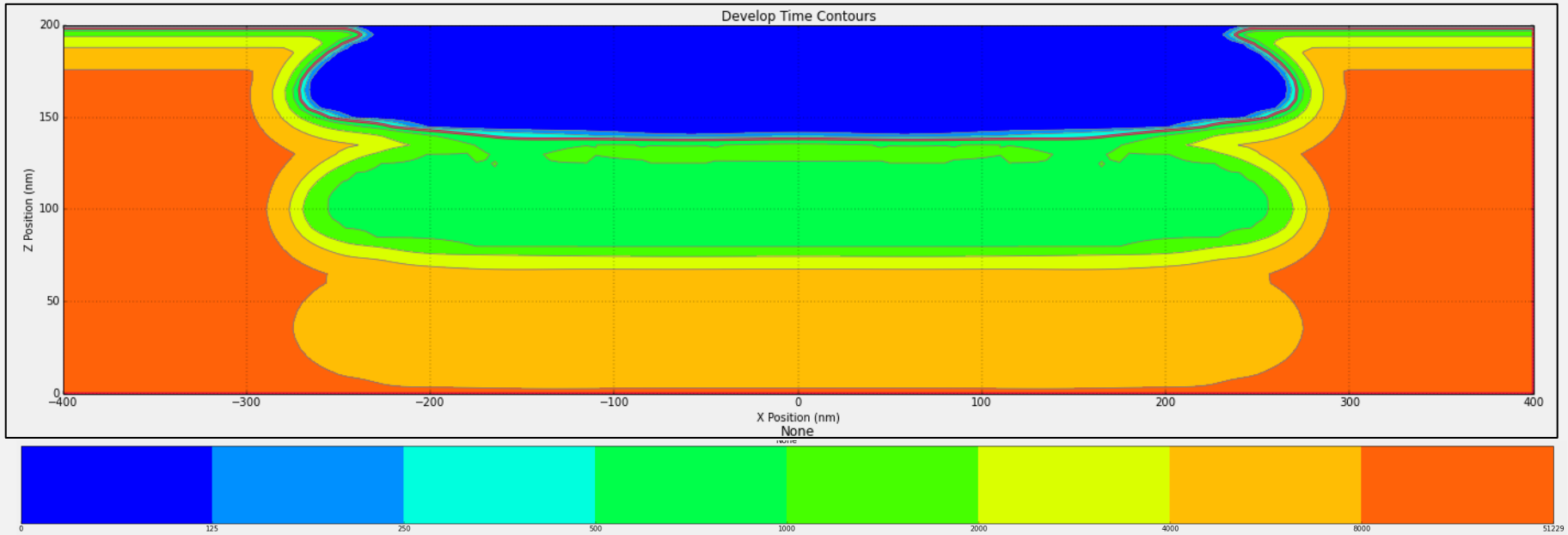
Standing waves in resist after post exposure bake of 1sec

Such a short exposure bake does not cause any significant change

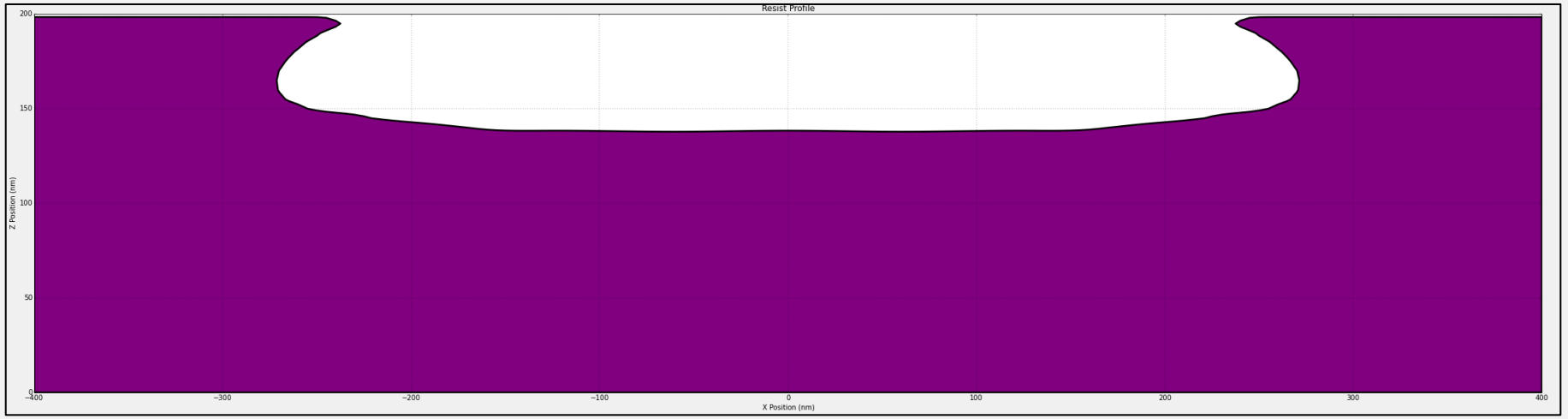


OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 1 sec



Time contours of development of the resist after PEB of 1 sec

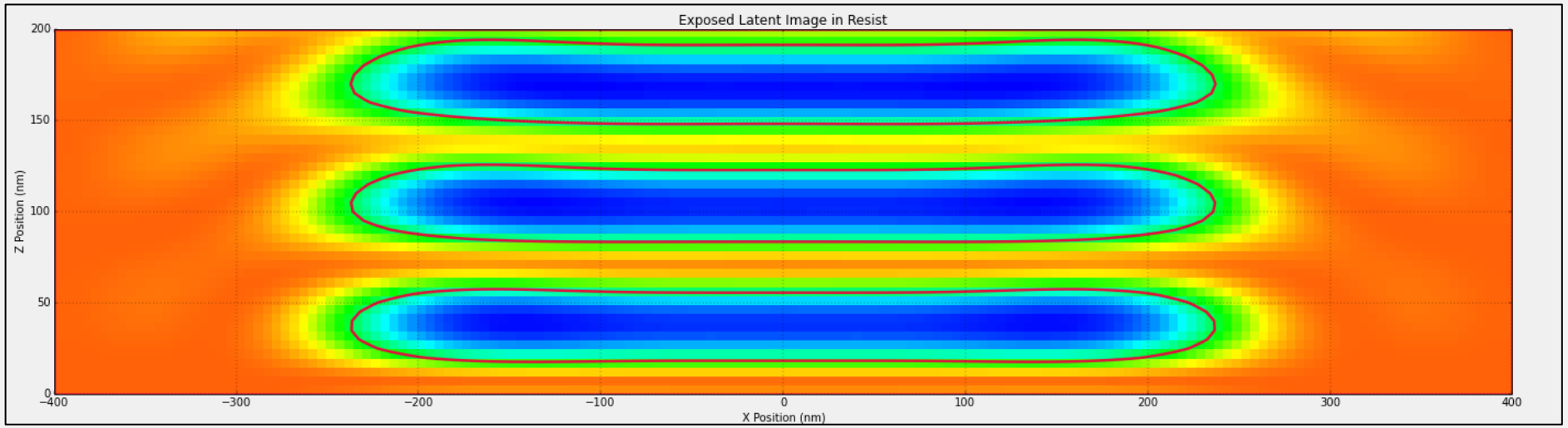


Final resist profile post development and cleaning.

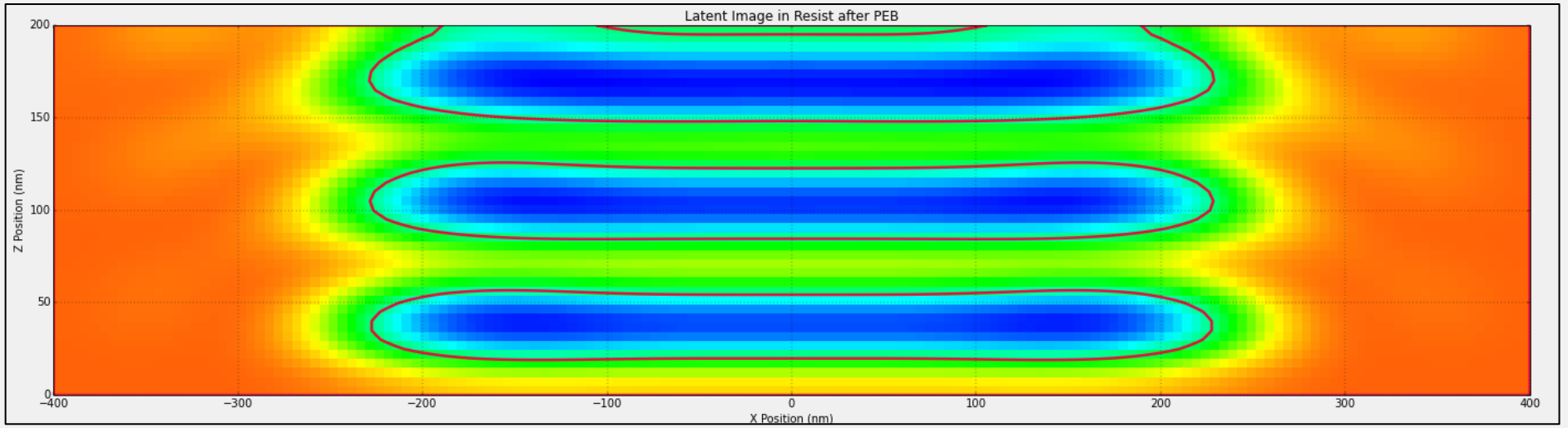
We can observe that due to the short post-exposure bake we get a very bad resist profile.

OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 10 sec

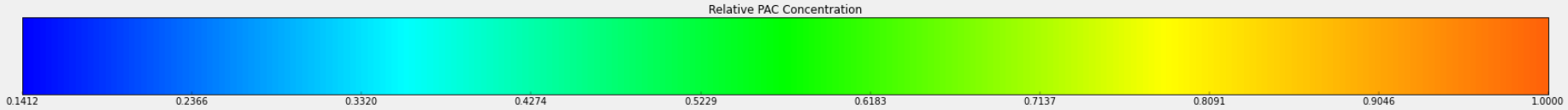


Standing waves seen in PAC concentration in resist after exposure to light



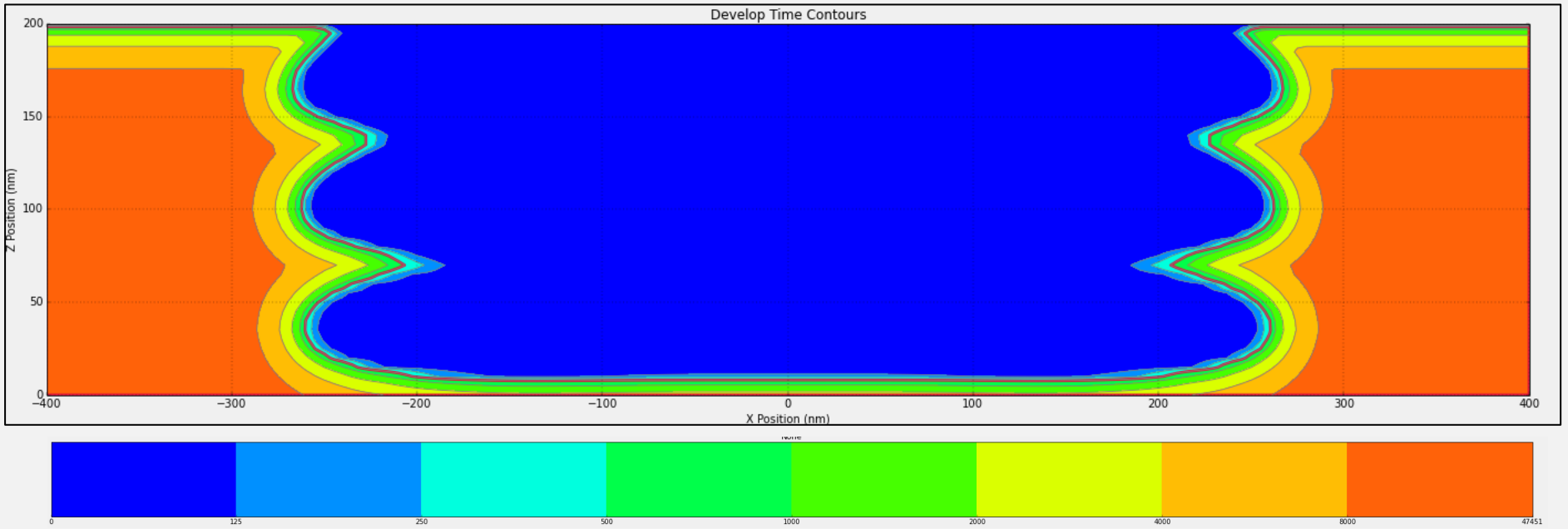
Standing waves in resist after post exposure bake of 10 sec

We can see a diffusion of light exposed region by the relative increase in size of the green region.

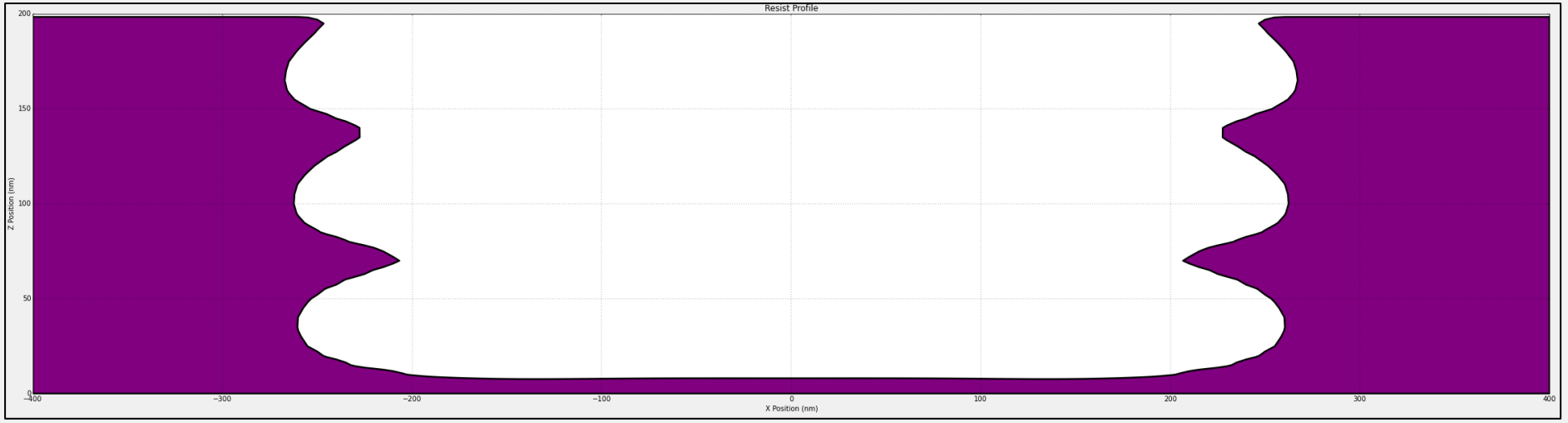


OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 10 sec



Time contours of development of the resist after PEB of 10 sec

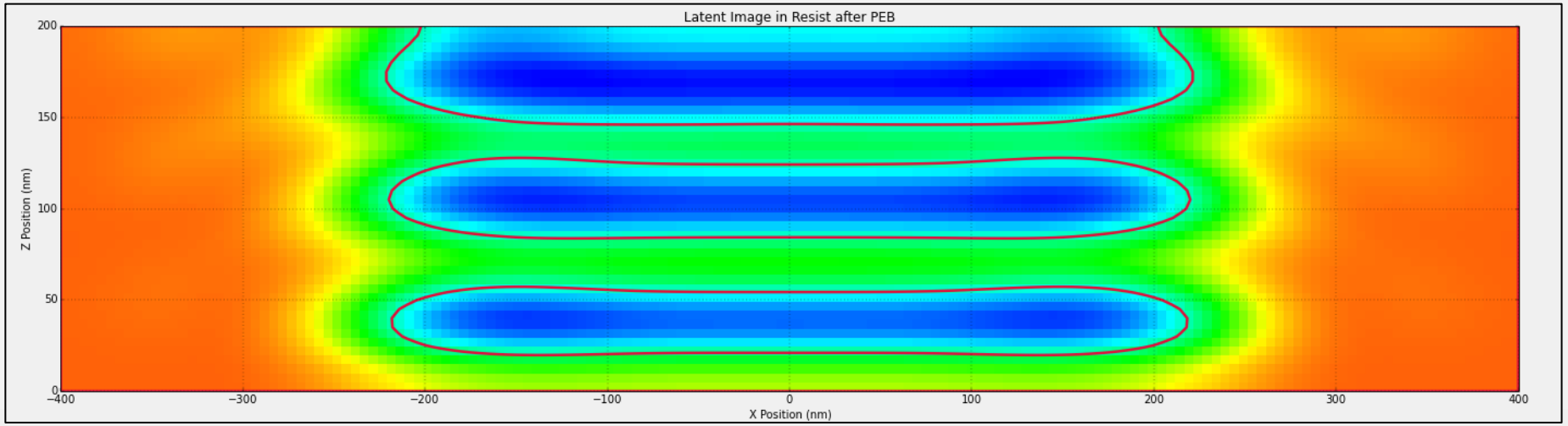


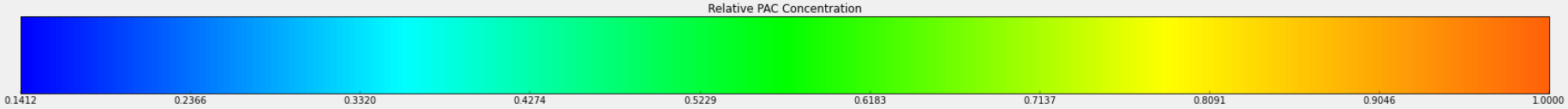
Final resist profile post development and cleaning.

We can observe that due to the 10 sec PEB we are able to remove the resist to almost the required depth but side wall profile is still undesirable.

OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

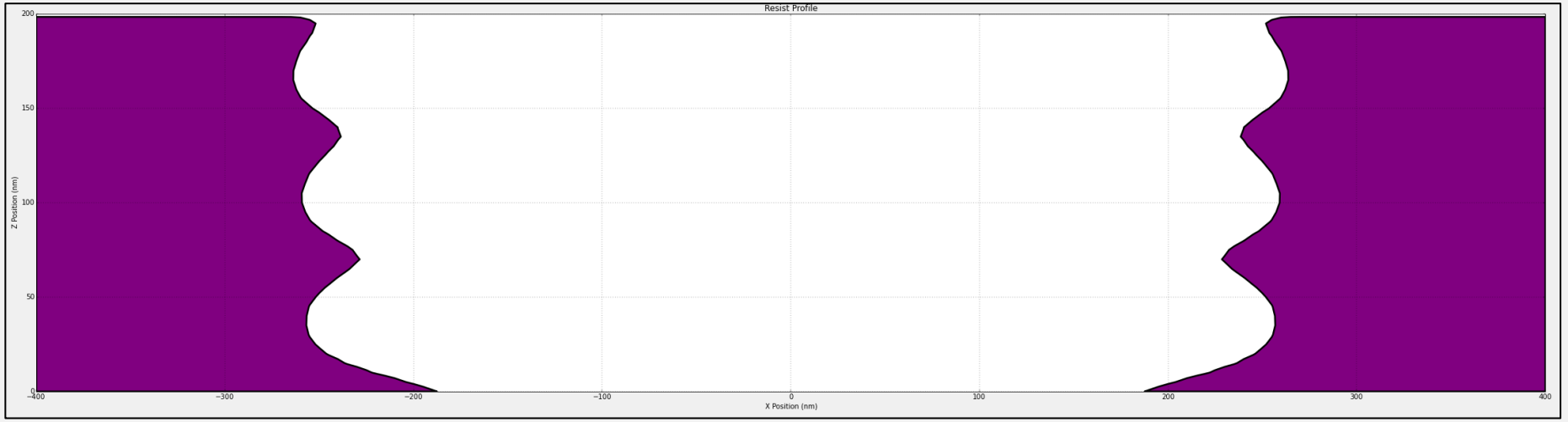
Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 20 sec





Standing waves in resist after post exposure bake of 20 sec

We can see a significantly higher amount of diffusion of light exposed region but the standing wave nodes are still present in the latent image.

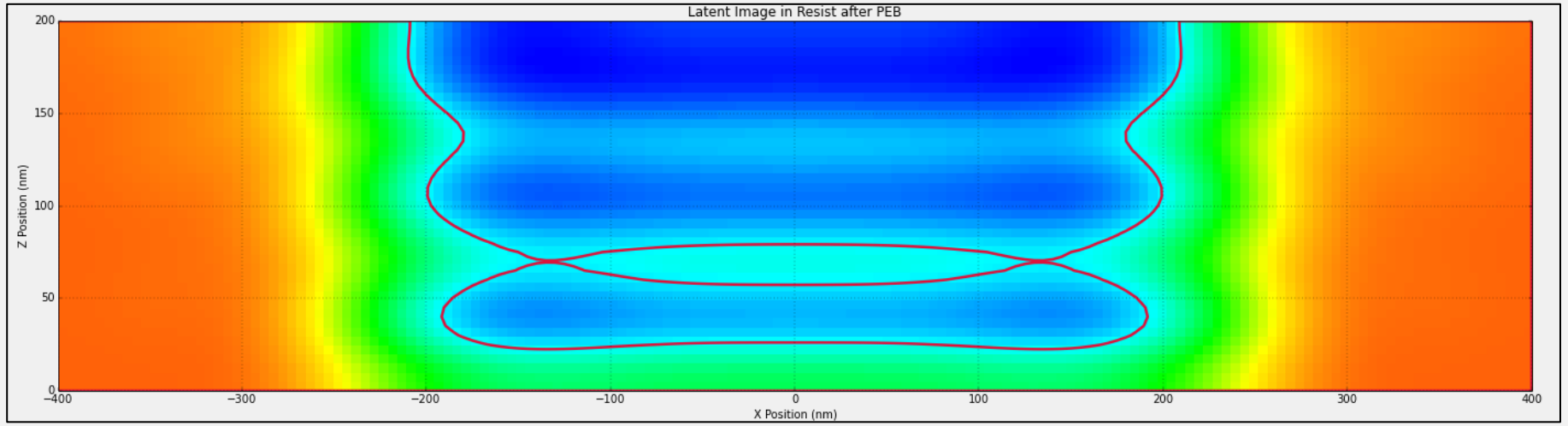


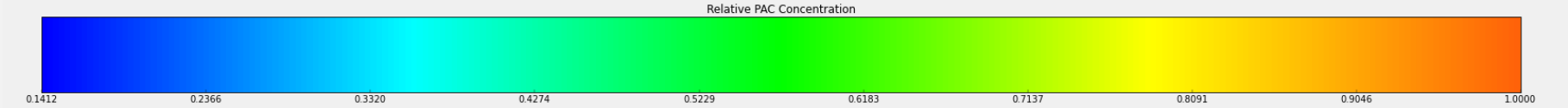
Final resist profile post development and cleaning.

We can observe that due to the 20 sec PEB we are able to remove the resist completely to the required depth but side wall profile is still undesirable.

OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

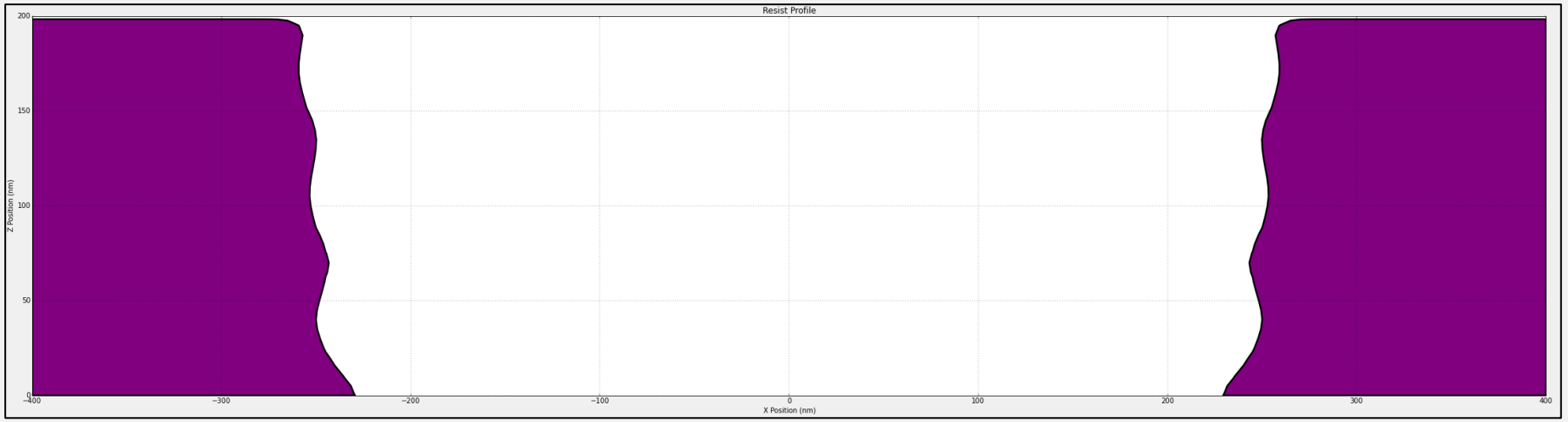
Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 50 sec





Standing waves in resist after post exposure bake of 50 sec

We can see a significantly higher amount of diffusion of light exposed region. The standing wave nodes are no longer distinct and merge to form an almost smooth profile

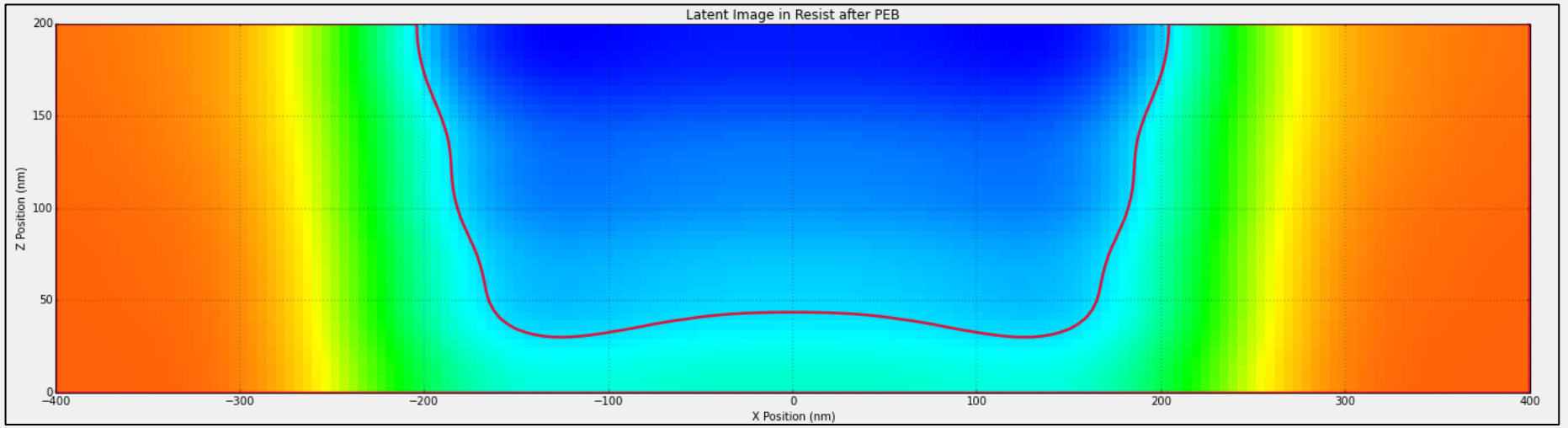


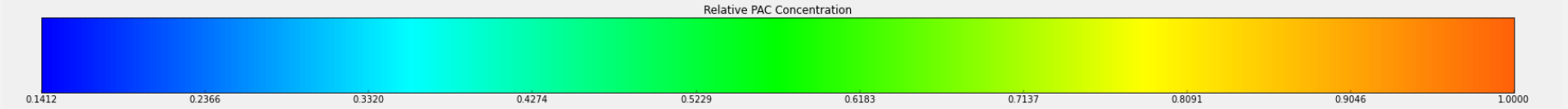
Final resist profile post development and cleaning.

We can observe that due to the 50 sec PEB we are able to remove the resist completely to the required depth with an improved side wall profile.

OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

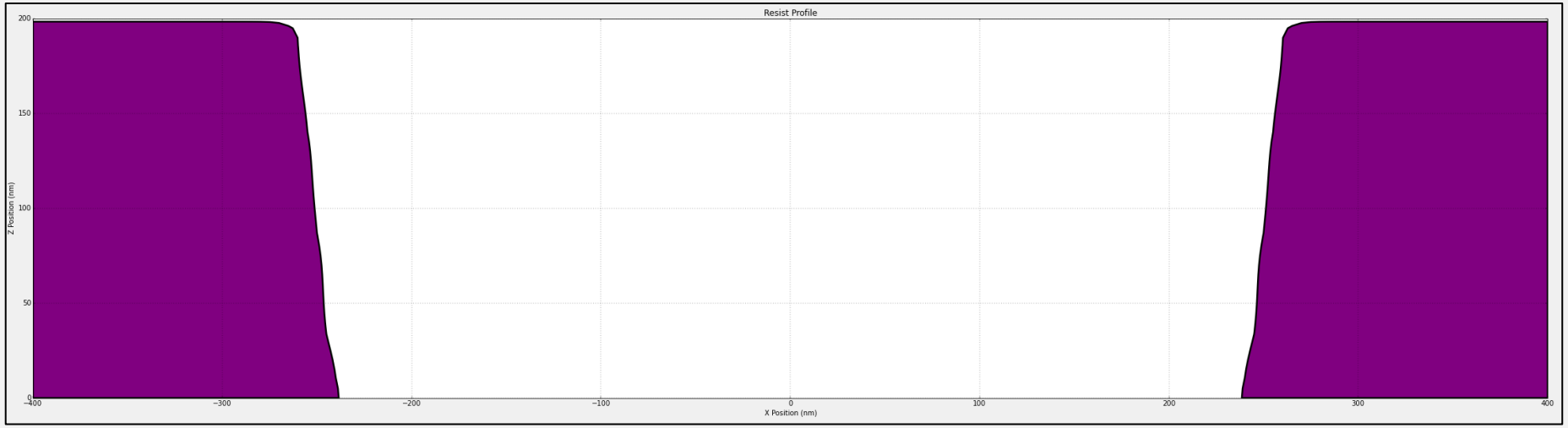
Reduction of the impact of standing waves using post exposure bake : Bake temperature = 120 C and Bake time = 100 sec





Standing waves in resist after post exposure bake of 100 sec

We can see almost uniform diffusion of the light exposed region over the entire etch area. The standing wave nodes are no longer distinct and merge to form a smooth profile

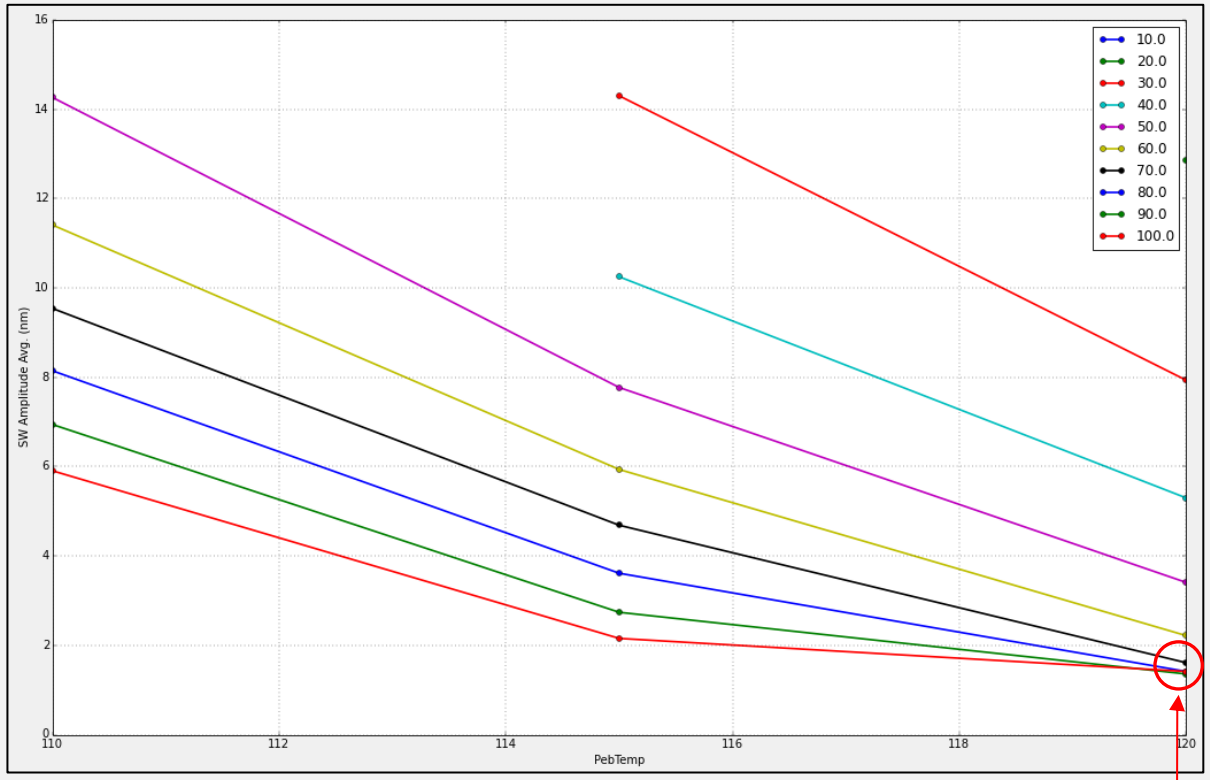


Final resist profile post development and cleaning.

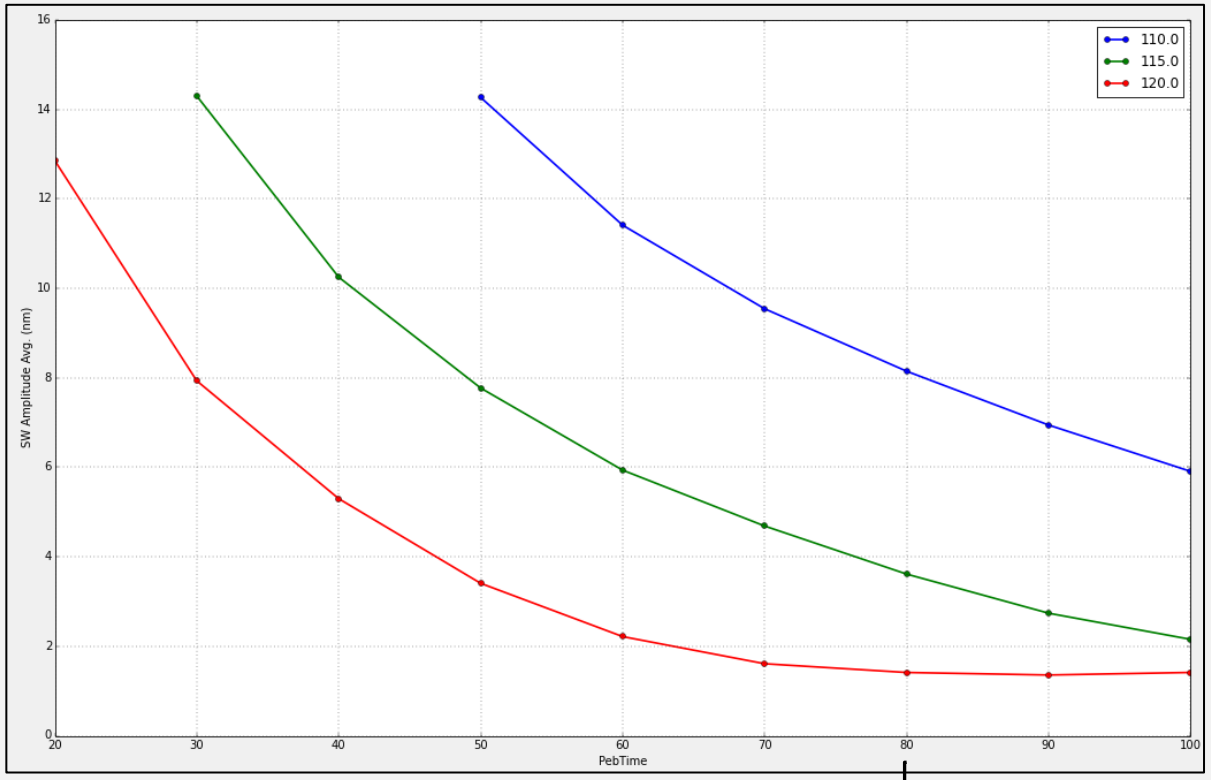
We can observe that due to the 100 sec PEB we are able to remove the resist completely to the required depth with an we also get a flat sidewall profile as desired.

Optimization of the PEB time by PEB time sweep

SW amplitude vs PEB temperature for different PEB time :



SW amplitude vs PEB time for different PEB temperature :



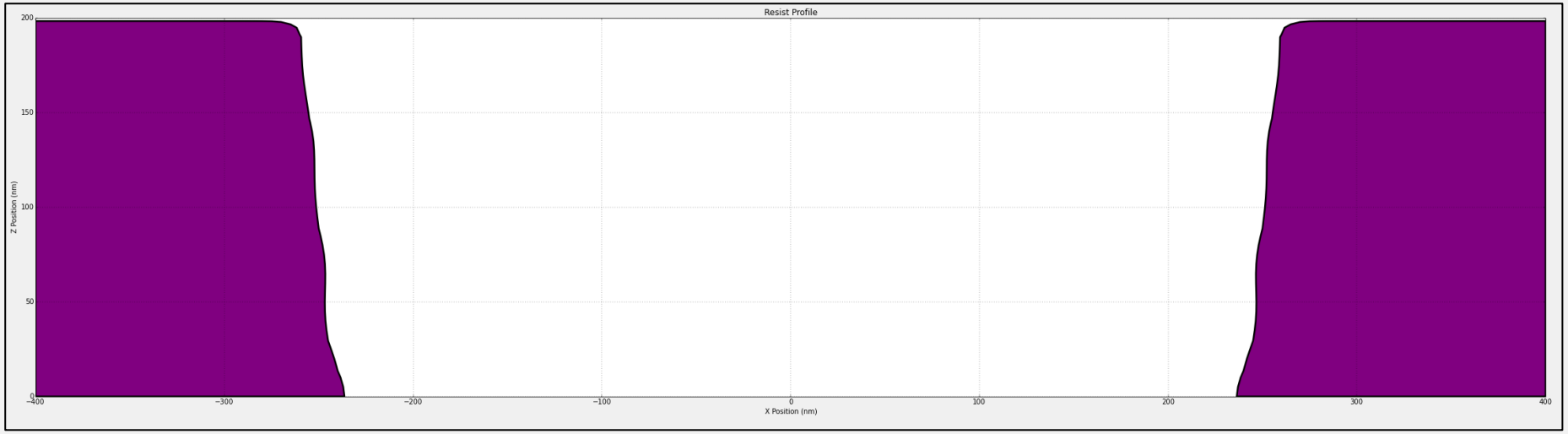
Variation of SW amplitude with PEB temperature for different PEB time periods

At 120 C we can see that the the lowest value of average SW amplitude saturates after time of 80 secs.

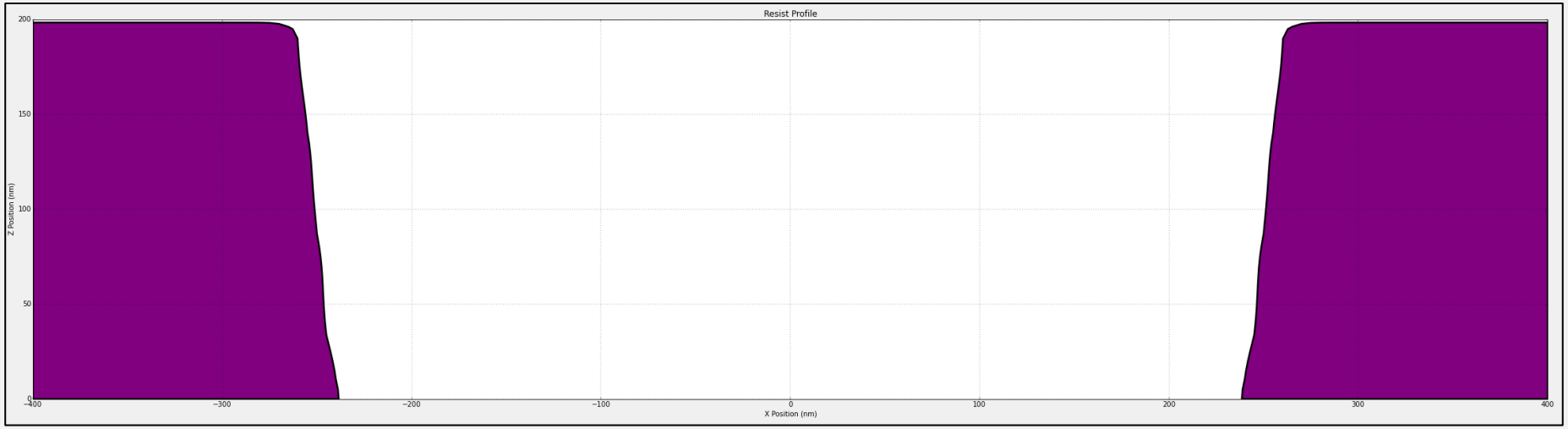
Therefore minimum PEB time for lowest average SW amplitude is 80 sec

OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Optimization of the PEB time by PEB time sweep : Minimum PEB time = 80 sec



Resist profile for PEB temperature = 120 C and PEB time = 80 sec.

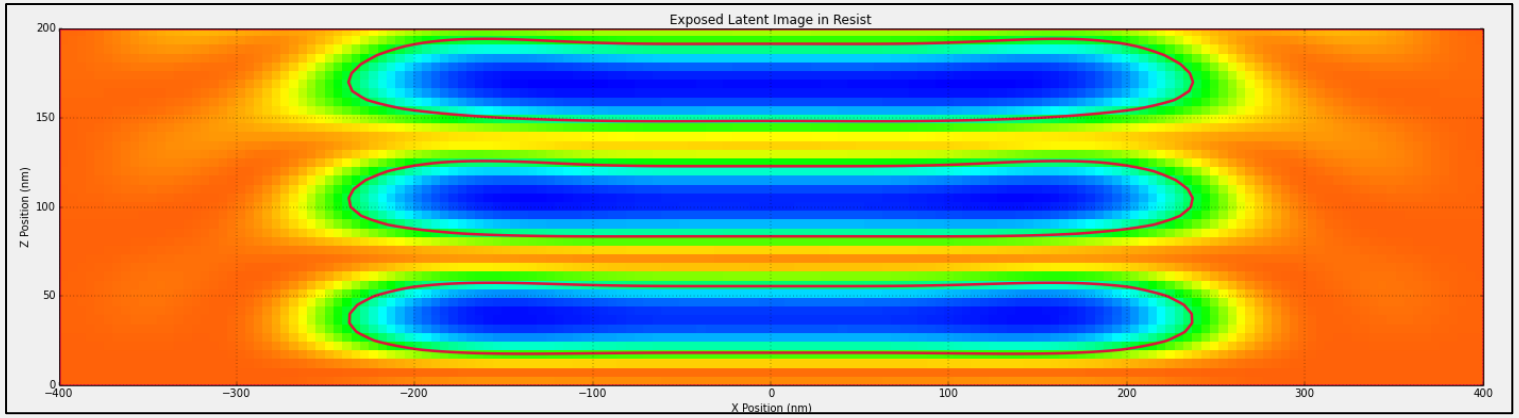


Resist profile for PEB temperature = 120 C and PEB time = 100 sec.

We can observe that the resist profile are very similar and although the sidewall profile for 80 second PEB time is comparatively more rough, the average value of the sidewall amplitude is approximately the same.

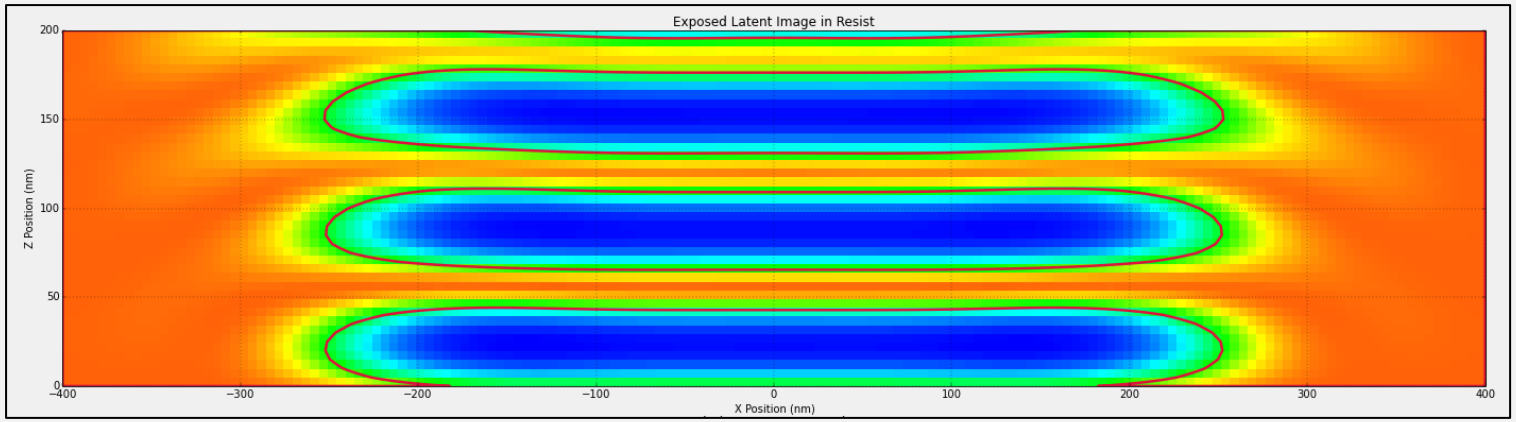
OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Reduction of the standing waves using an ARC layer



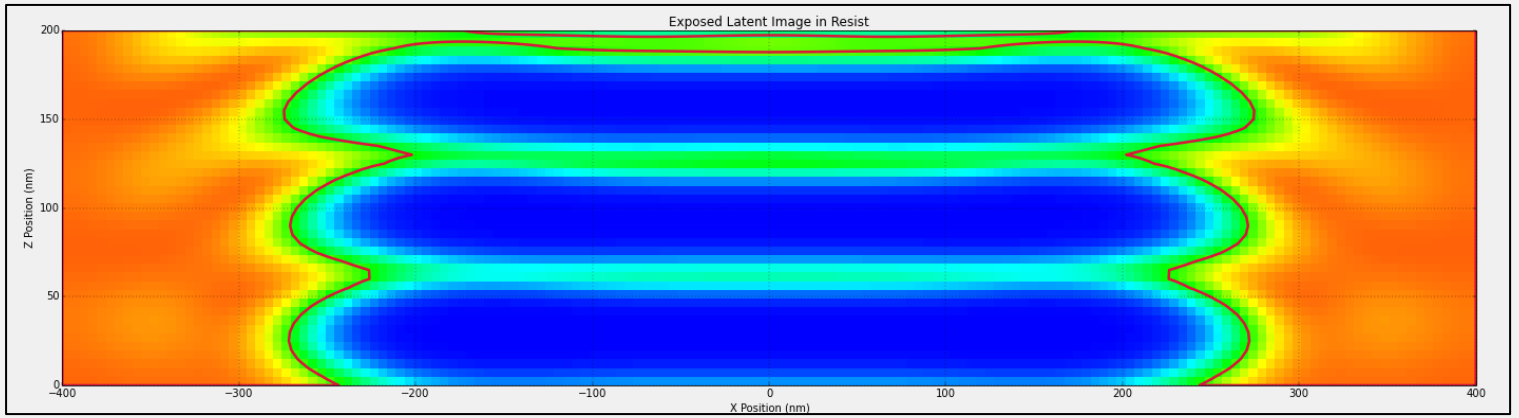
Standing waves in resist without SiON anti-reflection layer.

We see formation od distinct standing waves in the PAC concentration



Standing waves in resist with 25 nm SiON anti-reflection layer

We see a shift away from the standing wave pattern since there is an increase in the light exposed region, suggesting a decrease in reflection of light

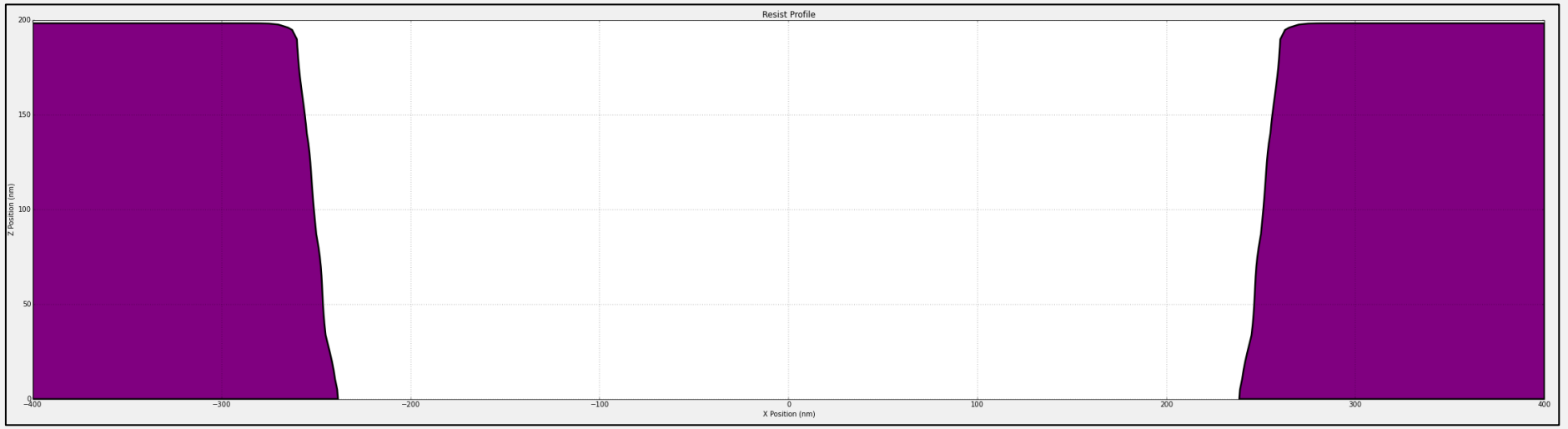


Standing waves in resist with 100 nm SiON anti-reflection layer.

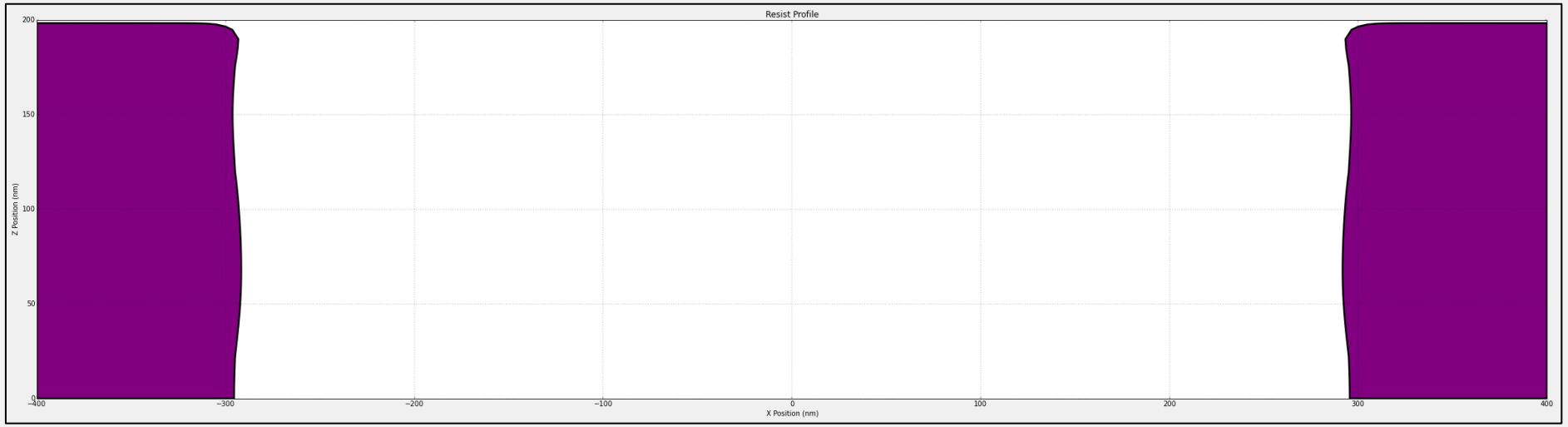
We can that the standing wave pattern is almost non-existent suggesting very low reflection due to the thick SiON layer

OPTOLITHIUM SIMULATIONS : SIMULATION OF STANDING WAVES PATTERNS IN RESIST

Reduction of the standing waves using an ARC layer



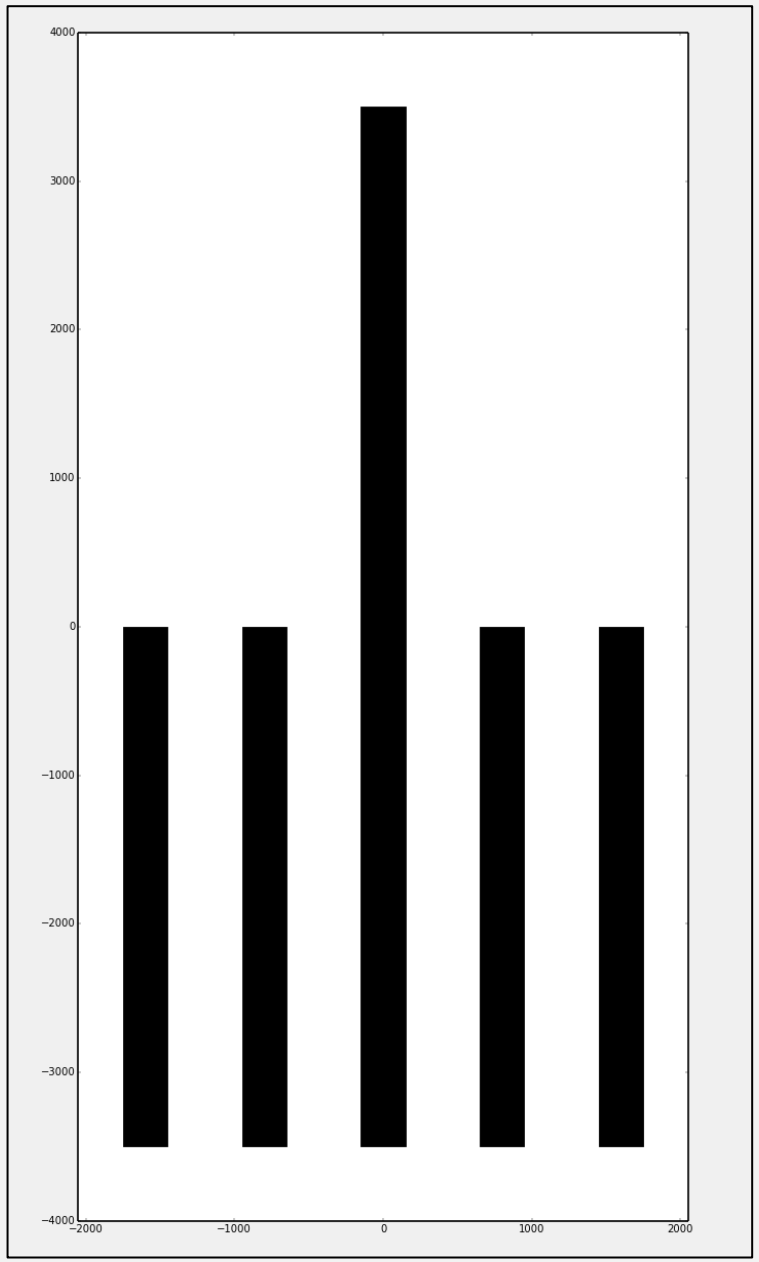
Resist profile without SiON anti-reflective layer for PEB time = 100 sec



Resist profile with 100 nm SiON anti-reflective layer for PEB time = 100 sec

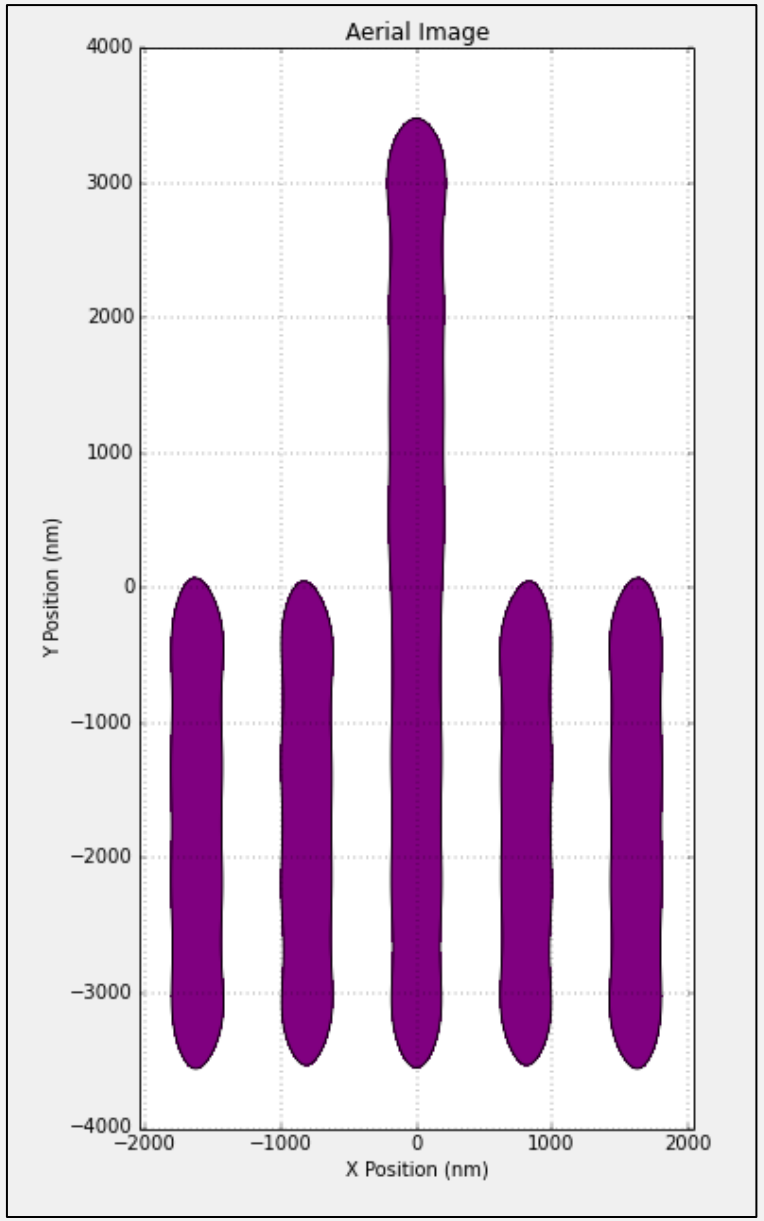
We can observe that the profile formed without SiON ARC layer has a slope to its side wall whereas the with the ARC layer, the side wall is almost vertical. We can infer that with the ARC layer, incident light can penetrate through the entire resist layer uniformly allowing more accurate formation of pattern for etch or deposition

Understanding proximity effect



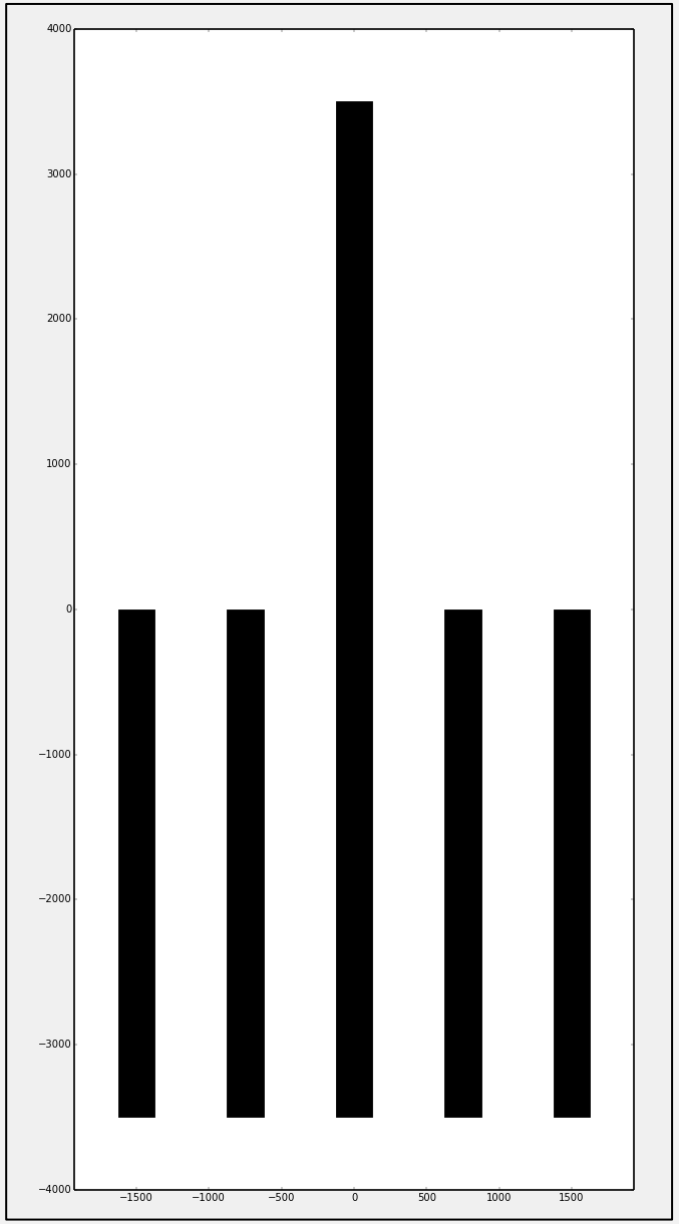
Design of mask for the lithography. We note that the shapes in the mask have sharp edges. The black region is 0% transmittance. The white region is 100 % transmittance.

We can see the aerial image of the image created by the mask. The proximity effect can be observed in this image as the curving of the pattern at the corners of the pattern due to insufficient resolution of incident light. At the corners the incident light exposure is higher due to exposure from multiple direction causing a curved edge to form. We can also observe that thickness of the central finger is lower in the region where it is surrounded by the other two fingers



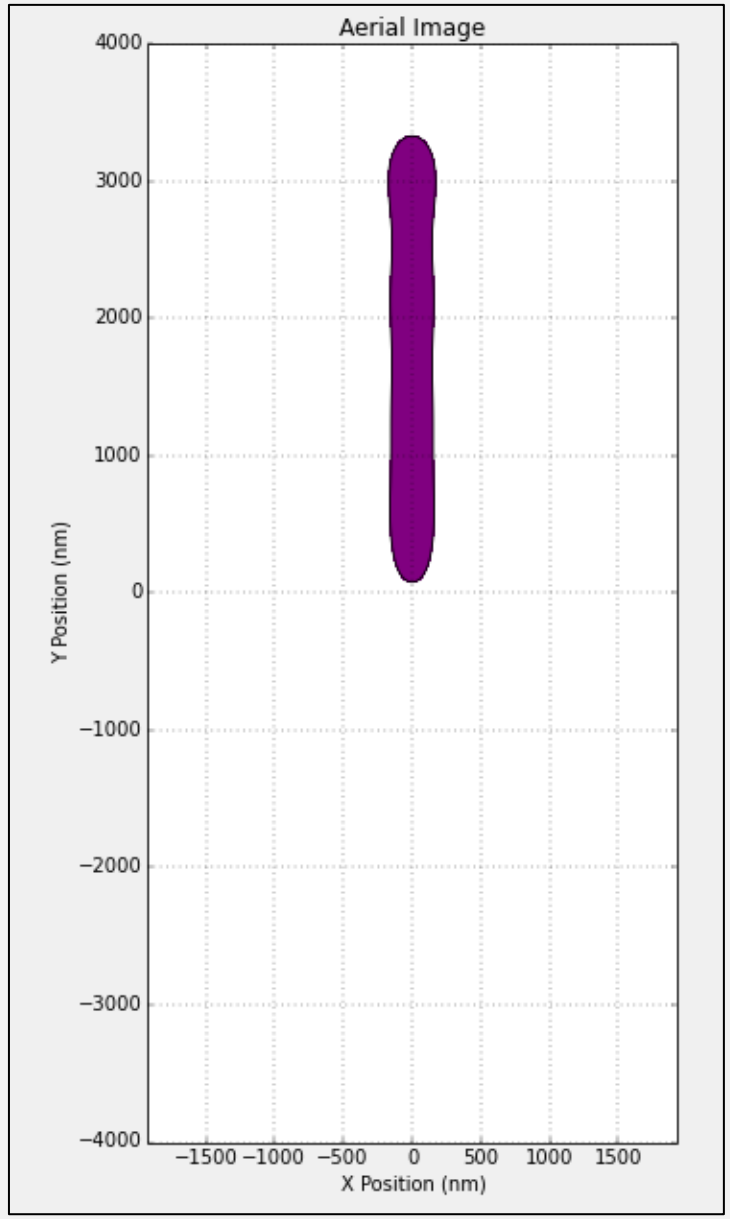
OPTOLITHIUM SIMULATIONS : SIMULATION OF PROXIMITY EFFECTS

How do proximity effects vary with feature sizes : Mask feature width = 250 nm



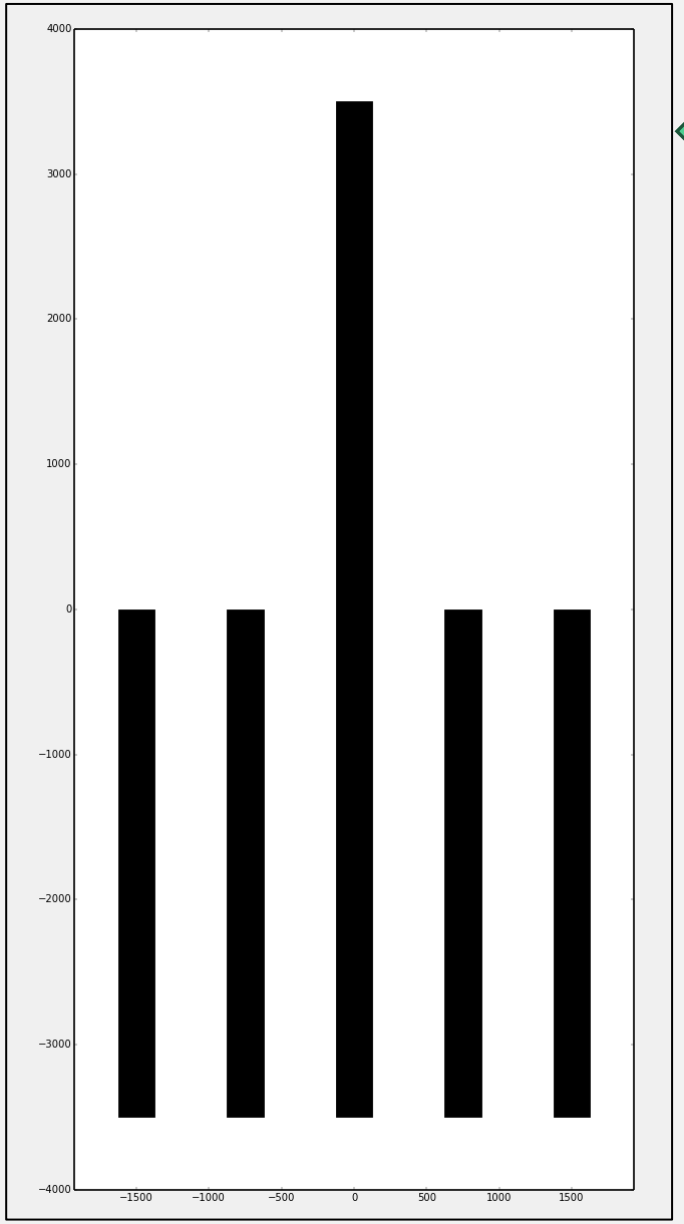
Design of mask for the lithography. We note that the shapes in the mask have sharp edges and we have significantly reduced the feature dimensions in the mask. The black region is 0% transmittance. The white region is 100 % transmittance.

We can see the aerial image of the image created by the mask. The low feature width causes the entire lower half of the mask to be etched due to the proximity effect caused by closely spaced fingers. Therefore at smaller feature dimensions the proximity effect has a comparatively larger impact.



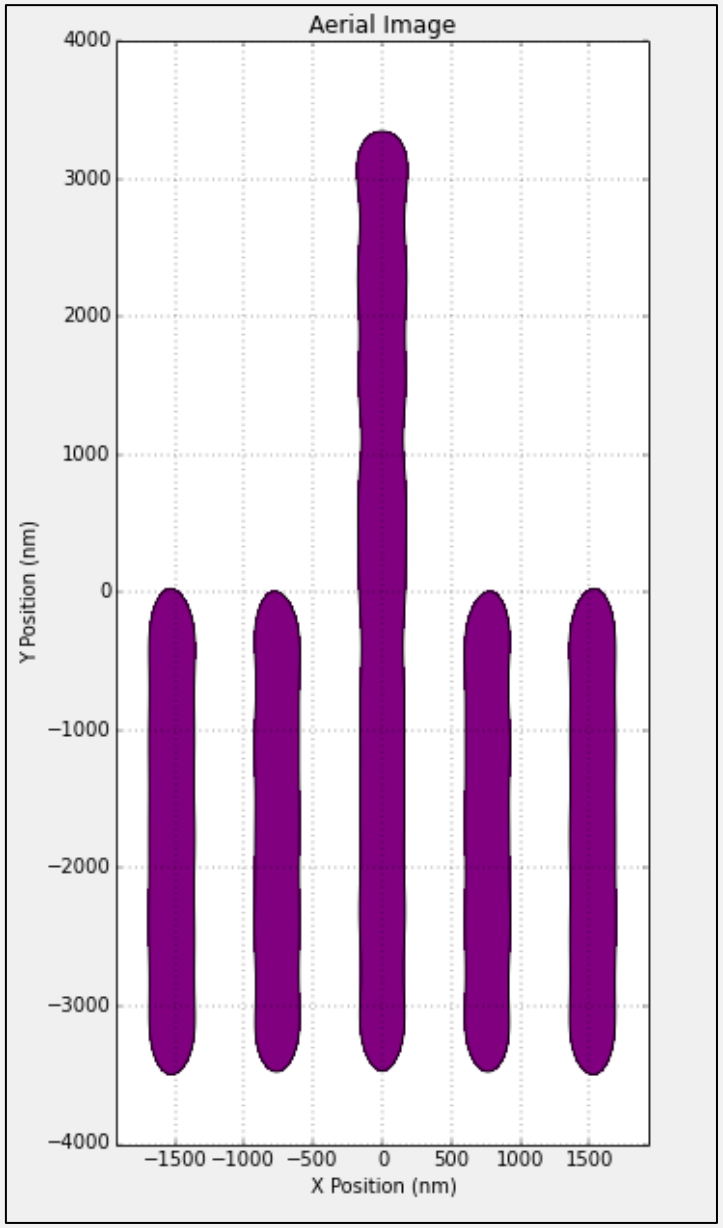
OPTOLITHIUM SIMULATIONS : SIMULATION OF PROXIMITY EFFECTS

How do proximity effects vary with feature sizes : Mask feature width = 250 nm and numerical aperture = 0.5



Design of mask for the lithography. We note that the shapes in the mask have sharp edges and we have significantly reduced the feature dimensions in the mask but we have also increased the numerical aperture of the lens for patterning. The black region is 0% transmittance. The white region is 100 % transmittance.

We can see the aerial image of the image created by the mask. The increase in numerical aperture causes a decrease in the proximity effect which allows for the lower half of the pattern to be etched according to the design of the mask. This can also be observed as a decrease in the radius of curvature at the corners of the mask.



PROBLEM 10.4 ICF-SAT (PLUMMER, GRIFFIN)

Given :

$$k_s = 1 * 10^7 * e^{-\frac{1.9eV}{kT}} \frac{cm}{sec} = 1 * 10^7 * e^{-\frac{1.9\ eV}{8.62*10^{-5}\ *1173\ eV}} \frac{cm}{sec} = 0.069 \frac{cm}{sec}$$

Also $h_g = 10 \frac{cm}{sec}$

Since $k_s \ll h_g$ we can say that the deposition rate is controlled by the surface reaction and system will be in the surface reaction controlled regime. The diffusion of precursors through the boundary layer of the gas phase is fast enough that it does act as the rate limiting step. Thus we can stack the wafers since gas transport variations will not cause uniformity problems and stacking will allow for maximum throughput. Since the deposition rate depends on surface reaction rate , it is sensitive to the temperature of the wafer. In a hot-walled system good temperature control can be achieved and thus I would recommend a **hot-walled, stacked wafer type CVD system**.

Assumption:
We are assuming that mass transfer is very fast relative to the reaction rate for all position on a wafer, independent of its size. This need not always be true since the reactants from the gas stream have to pass through a stagnant layer between the wafers, which reduces hg as the gas particles travel further. Therefore for depending on wafer size, the spacing between the wafers and pressure in the chamber have to be adjusted to keep the system in the surface reaction controlled regime.