EE669: VLSI Technology

A Typical CMOS Process Flow

Anil Kottantharayil
Department of Electrical Engineering
IIT Bombay

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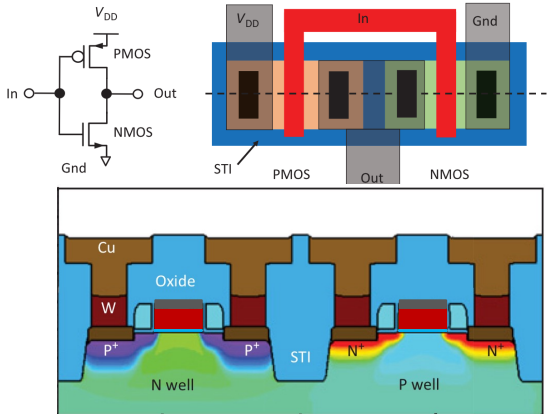
What do we aim to make?



Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023.

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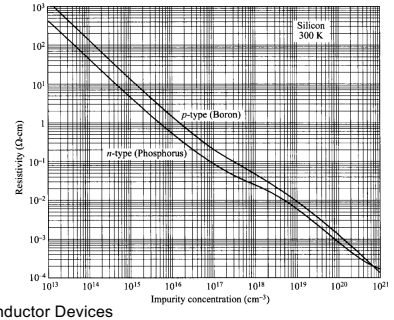
Choice of wafers

- Wafer diameter
- Crystal orientation
- Wafer doping type
- Doping concentration in the wafer



S. M. Sze, Physics of Semiconductor Devices

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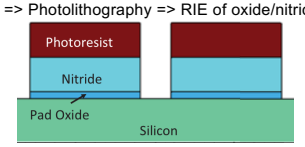
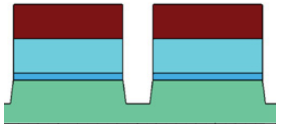
STI: Shallow Trench Isolation

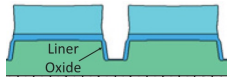
Pad oxide growth => nitride deposition
=> Photolithography => RIE of oxide/nitride



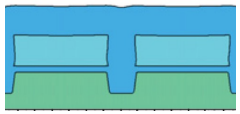
Trench etching by RIE



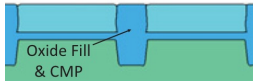
Sidewall oxidation, corner rounding



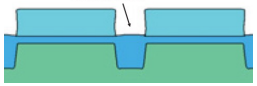
Oxide fill by CVD



CMP for planarization



HF
Oxide Etch



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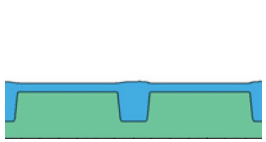
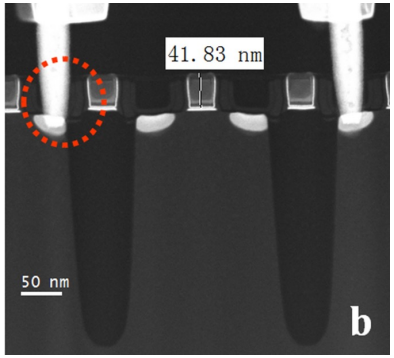
STI: Shallow Trench Isolation (2)





Zhao *et al.* Study of the yield improvement and reliability of 28 nm advanced chips based on structural analysis. *J Mater Sci: Mater Electron* **32**, 18076–18086

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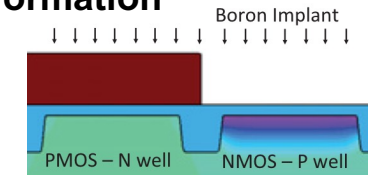
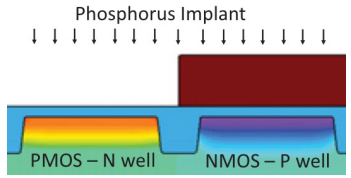
Well Formation

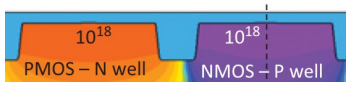
Mask n-well by resist
p-type implants
Strip resist



Mask p-well by resist
n-type implants
Strip resist



Thermal anneal
To remove implant damage
& diffuse dopants



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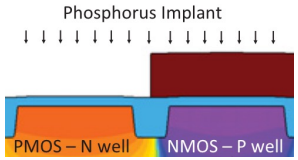
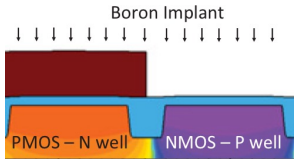
Threshold Voltage Adjust Implant

Mask p-well by resist
n-type implants
Strip resist



Mask p-well by resist
n-type implants
Strip resist



Short thermal anneal
To remove implant damage

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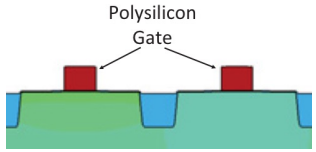
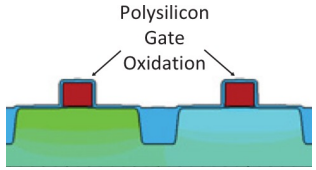
Gate oxide and poly-Si Gate

Remove implant screening Oxide
RCA Cleaning
Gate oxidation
LPCVD poly-Si layer
Remove backside layers



Gate lithography
RIE of poly-Si
Strip resist
RCA clean
Re-oxidation



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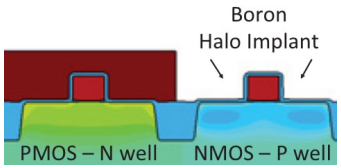
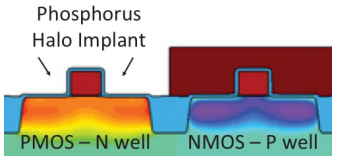
Halo implants

N-well mask litho
p-type HALO implant
Strip resist



P-well mask litho
n-type HALO implant
Strip resist
RT anneal



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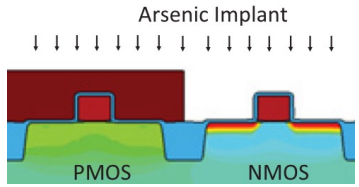
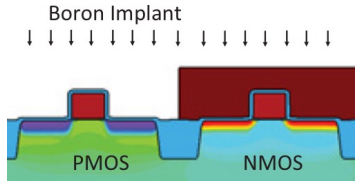
Source/drain extension implants

N-well mask litho
p-type extension implant
Strip resist



P-well mask litho
n-type extension implant
Strip resist
RT anneal



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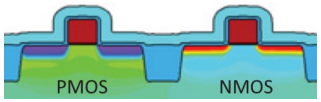
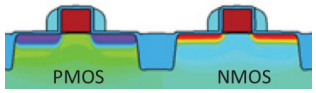
Spacer Formation

Conformal deposition of dielectric layer(s) : oxide and nitride
remove backside layers



anisotropic dry etching



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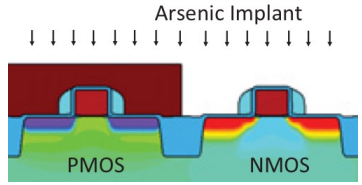
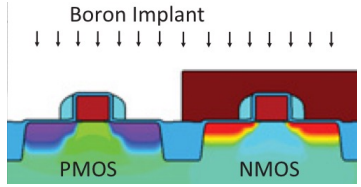
Deep source/drain implants

N-well mask litho
n-type implant
strip resist



P-well mask litho
p-type implant
strip resist
RT anneal



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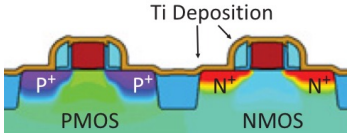
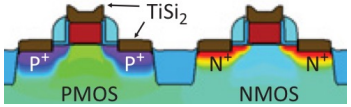
Self aligned silicide (salicide) contacts

Wet/dry etch oxide metal sputter : Ti, Co/Ti, Ni



Silicidation RTP treatment
Selective etch
(Opt.) 2nd RTP treatment



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Exercise

From the 45 nm technology node (introduced in ~ 2007) onwards, high-k/metal gates are used in CMOS technology. Due to thermal and other concerns, a replacement gate process was used for the integration of high-k/metal gates. Using "Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023" as the reference, study the replacement gate process, and write down the sequence of process steps starting after the S/D contact formation, required for the realization of the transistor. Only process steps before the backend of line should be mentioned. Note that in a replacement gate process, a silicide is typically not grown on the poly-Si dummy gate. Instead, the poly-Si is capped to prevent silicidation.

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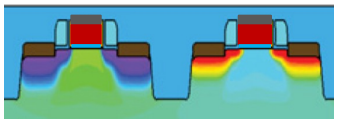
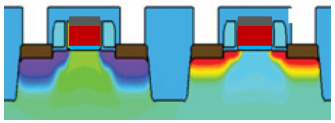
Metal Interconnects (backend of line process)

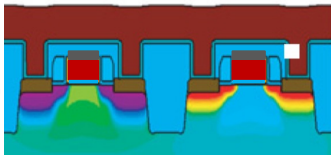
Interlayer dielectric (SiO_2)
PECVD
Planarized by CMP



Lithography
Anisotropic RIE



Barrier layer deposition (TiN, WN) sputtering or ALD
W deposition by sputtering or ALD



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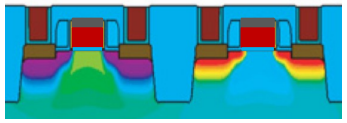
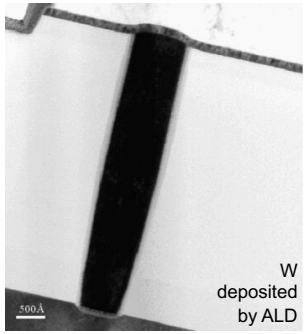
Metal Interconnects (2)

W CMP





W deposited by ALD

Luoh et al., Advanced tungsten plug process for beyond nanometer technology, Microelectronic Engineering, vol. 85, No. 8, 2008, pp. 1739-1747.

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