Metal Interconnects – Damascene Process

https://aramkingdom.com/history-of-the-damascene/

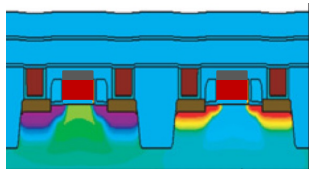
https://www.ethnicjewellery786.com

Damascening is the art of inlaying different metals into one another—typically, gold or silver into a darkly oxidized steel background—to produce intricate patterns, **and was first developed into an art form before 2000 BC,** in Damascus, Syria. *More recently*, the term is also used to describe the use of inlaid copper interconnects in integrated circuits.

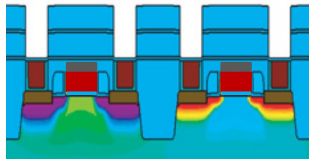
www.wikipedia.org

Dual Damascene Copper Interconnect Process

Si_3N_4 etch stop layer (PECVD)
Interlayer dielectric, SiO_2 (PECVD)
Si_3N_4 etch stop layer (PECVD)
Interlayer dielectric, SiO_2 (PECVD)

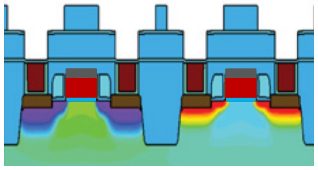


Photolithography
RIE to open vias stopping on second nitride

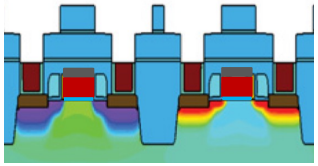


Dual Damascene Copper Interconnect Process (2)

Photolithography
RIE to open vias stopping on nitride

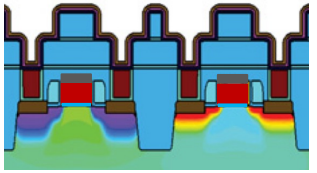


RIE to etch nitride

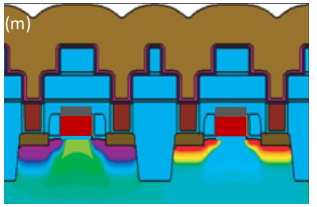


Dual Damascene Copper Interconnect Process (3)

Adhesion/barrier layers of TaN/Ta deposited conformally (sputter or ALD)
Cu seed layer by sputtering



Copper electroplating

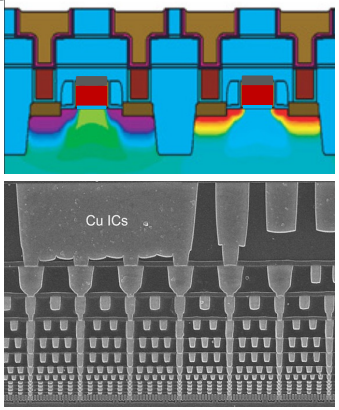


Dual Damascene Copper Interconnect Process (4)

Copper CMP

Repeat as many times as there are interconnect levels

Intel 14 nm Broadwell architecture



https://www.embeddedrelated.com/showarticle/1568.php

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Exercise (2)

In the dual damascene process discussed in the previous slides, two lithography steps are required. The second lithography is carried over the large topography created by the first RIE process. This can be a quite demanding process. A modified process sequence that avoids this issue is given in chapter 11, Fig. 11.19 of "Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023". Study this process. Draw the schematic of the structures before the second lithography in the two cases side-by-side. Comment on the relative topographies in the two cases.

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Exercise (3)

You will attempt to create a sprocess input deck for simulating the process sequence to create a 180 nm gate length n-channel MOSFET in this exercise.

The process sequence, along with the commands in the script and explanations can be found in https://kolegite.com/EE_library/books_and_lectures/Автоматизация%20на%20Проектирането%20в%20Електрониката/Sentaurus_Training/sp/sp_3.html

Notes:

1. No dielectric isolation is included.
2. The thickness of the silicon substrate can be reduced to 3 um without any difference to the result of the simulation.
3. You are expected to submit the code (in an ascii text file, with an extension "cmd").
4. Clarifications, if any will be addressed in a tutorial session to be conducted later. Students should note down their doubts while going through the exercise.
5. You may download the sprocess manual from https://kolegite.com/EE_library/books_and_lectures/Автоматизация%20на%20Проектирането%20в%20Електрониката/Sentaurus_manuals/PDFManual/data/sprocess_ug.pdf

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