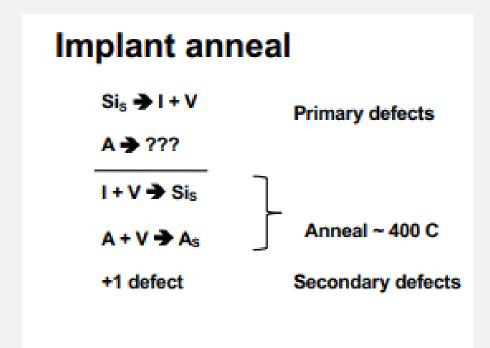
# EE 669 VLSI TECHNOLOGY

# ASSIGNMENT 5: SRIM

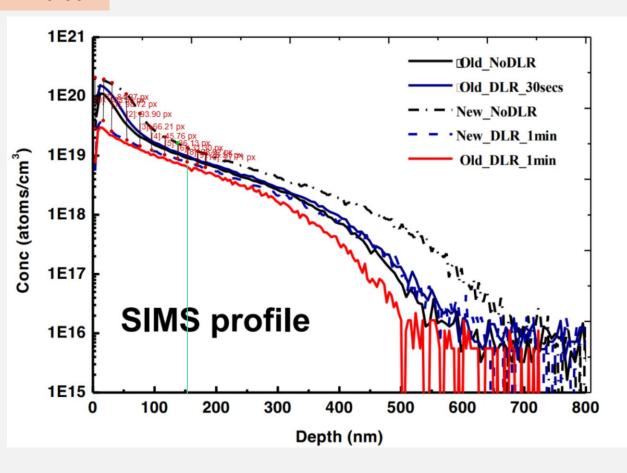
KARTIK CHIKKANAGOUDAR

21D170023



The question mark in the image represents a vacancy (V). During the implant anneal process, the acceptor atom (A) is displaced from its lattice site, creating an interstitial (I) and a vacancy (V). This vacancy (V) is represented by the question mark in the image.

L26-S8



# Difference values 0, 103.5271739130435 1, 98.71929651925994 2, 93.90445550790851 3, 66.20923913043478 4, 45.76040200693185 5, 36.134188270505504 6, 31.29891304347825 7, 84.27490251165112 8, 28.916372729416832 9, 26.511040724664483 10, 27.713657303897026

New_DLR_1	min values	New_NoD	DLR values
6.635071	2.85E+19	4.739336	1.92E+20
11.37441	3.43E+19	18.95735	1.75E+20
23.69668	2.66E+19	33.17536	1.52E+20
35.07109	2.27E+19	45.49763	1.24E+20
49.2891	1.89E+19	57.81991	9.42E+19
63.50711	1.61E+19	67.29858	6.99E+19
74.88152	1.44E+19	77.72512	4.96E+19
87.20379	1.25E+19	87.20379	3.44E+19
		93.83886	2.79E+19
94.78673	1.14E+19	107.109	2.33E+19
106.1611	1.04E+19	120.3791	1.94E+19
118.4834	9.73E+18	133.6493	1.65E+19
129.8578	8.88E+18	148.8152	1.34E+19
141.2322	8.29E+18	160.1896	1.25E+19
151.6588	7.4E+18	173.4597	1.07E+19
163.981	6.6E+18	186.7299	9.75E+18
175.3555	5.88E+18	200.9479	8.7E+18
188.6256	5.49E+18	215.1659	7.94E+18
200.9479	5.01E+18	232.2275	7.08E+18

Assuming that the DLR ends where the difference between the NoDLR and 1 min DLR concentrations stabilises we observe that the length of the dead layer is 150 nm

#### L26-S10

- 1. Si Iso Etch (Trilogy Etch) 126 parts  $HNO_3$ :60 parts  $H_2O$ :5 parts  $NH_4F$ , uses two-step process:  $HNO_3$  oxidizes silicon then HF etches oxidized compound.
- 2. KOH 29% KOH by weight at 80°C, etch rate varies with temperature (activation energy 0.59 eV), optimal for orientation-dependent etching with 160:100:1 ratio for (110):(100):(111) planes.
- 3. 10:1 HF Mixed from H<sub>2</sub>O and 49% HF, etch rate increases linearly with HF concentration below 10M, requires polypropylene/HDPE/PTFE/PVDF containers.
- 4. BHF (5:1) 33% NH<sub>4</sub>F and 8.3% HF by weight, pH ~3, better photoresist adhesion than concentrated HF, reaction:  $SiO_2 + 4HF + 2NH_4F \rightarrow (NH_4)_2SiF_6 + 2H_2O$ .
- 5. Pad Etch 4 Commercial NH₄F/CH₃COOH mix, etches silicon dioxide with selectivity to aluminum pads.
- 6. Phosphoric Acid 85% at 160°C, activation energy 0.99 eV, uses reflux system, reaction hydrolyzes nitride to hydrous silica and ammonia.
- 7. Al Etch A 80%  $H_3PO_4$ , 5%  $HNO_3$ , 5%  $CH_3COOH$ , 10%  $H_2O$  at 50°C, two-step process:  $HNO_3$  oxidizes aluminum then  $H_3PO_4$  etches oxide.
- 8. Ti Etch 20:1:1  $H_2O/H_2O_2/HF$ , forms oxide from water and peroxide which is then etched by HF.
- 9. CR-7/CR-14 Commercial cerium-based chromium etchants at room temp, CR-14 has less undercut but shorter shelf life.
- 10. Moly Etch Mix of  $H_3PO_4/CH_3COOH/HNO_3/H_2O$  at room temp, targets molybdenum with moderate photoresist etch.
- 11. Cu Etchants FeCl<sub>2</sub>-based (CE-200) or persulfate-based (APS 100) at room temp, both compatible with photoresist.
- 12. Gold Etchants Diluted aqua regia (HCl/HNO $_3$ /H $_2$ O) or iodine-based AU-5 at room temp.
- 13. NiCr TFN Commercial cerium-based etchant for nickel-chromium alloy, also attacks pure metals.
- 14. Piranha  $H_2SO_4/H_2O_2$  at 120°C, oxidizes organics and removes metals by forming complexes, doesn't affect  $SiO_2$  and  $Si_3N_4$ .
- 15. Strippers Acetone breaks down photoresist structure making it soluble, effectiveness decreases if PR heated above 120°C.

#### L27-S12

#### Ion Milling (Purely Physical Etching):

- Uses a directional ion beam, typically argon ions, to sputter atoms directly from the substrate.
- Highly anisotropic, making it effective for precise vertical etching.
- Lacks selectivity and doesn't rely on volatile byproducts, making it suitable for any material.
- Primarily used in research applications due to its limitations in selectivity.

#### Ion-Enhanced Chemical Etching:

- Combines chemical reactions with ion bombardment to enhance etching rate.
- Ion bombardment assists the chemical etching process, improving directionality.
- Offers a balance of selectivity and anisotropy, widely applied in semiconductor fabrication.

#### Bosch Process (Deep Silicon Etching):

- Alternates between deposition (C4F8) and etching (SF6) steps to achieve deep, directional etching.
- Deposition phase creates a polymer that prevents lateral etching, while the etching phase clears material at the feature bottom.
- Essential for MEMS and through-silicon via (TSV) applications due to its precision in deep silicon structures.

#### High-Density Plasmas:

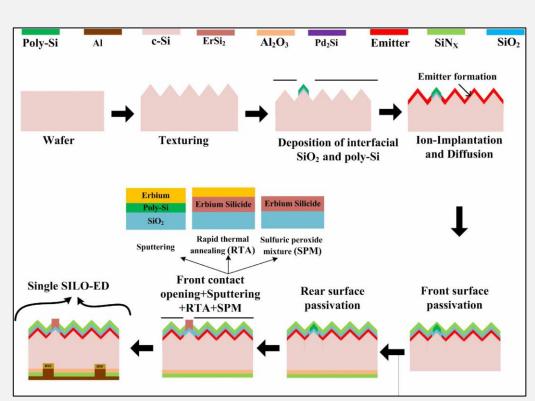
- Utilizes high-density plasma sources, like inductively coupled plasma (ICP), allowing independent control of ion energy and plasma density.
- Delivers high etch rates with minimal substrate damage, enhancing process flexibility and selectivity.
- Commonly used in advanced semiconductor manufacturing due to its precision and control.

#### Atomic Layer Etching (ALE):

- Provides precise, atomic-scale etching by alternating surface modification and material removal steps.
- Each cycle removes a controlled, thin layer, offering exceptional uniformity and feature control.
- Ideal for applications requiring minimal variation in etched features, critical in modern semiconductor fabrication.

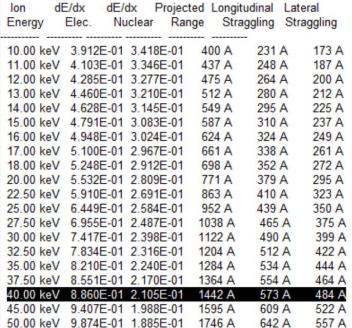
#### L29-S17

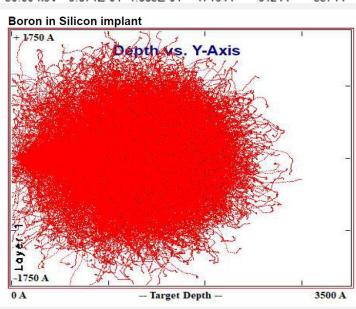
- 1. **Wafer Preparation**: Start with a silicon wafer as the base substrate, which provides the foundation for the solar cell structure.
- 2. **Texturing**: Use a texturing process on the wafer surface to create a rough texture (typically pyramid-shaped) that enhances light absorption by reducing reflectivity. This step is crucial for improving the efficiency of the solar cell.
- 3. **Interfacial Layer Deposition**: Deposit a thin layer of silicon dioxide (SiO<sub>2</sub>) as an interfacial layer to reduce recombination at the surface, followed by a layer of polycrystalline silicon (poly-Si) on top. This poly-Si layer will later be used to form the selective emitter region.
- 4. **Emitter Formation**: Perform ion implantation and diffusion of dopants into the poly-Si layer to form the emitter. This creates a junction that allows for efficient charge separation, critical for solar cell operation.
- 5. Erbium Silicide Formation:
- **Sputtering**: Apply an erbium layer using sputtering onto the poly-Si and  $SiO_2$  layers, allowing for the formation of a metal-silicide layer that enhances electrical contact properties.
- Rapid Thermal Annealing (RTA): Use rapid thermal annealing to form erbium silicide (ErSi<sub>2</sub>) by reacting erbium with silicon, providing a low-resistance contact for improved conductivity.
- **Sulfuric Peroxide Mixture (SPM) Treatment**: Treat the surface with a sulfuric peroxide mixture to clean and prepare it for subsequent layers, ensuring better layer adhesion and performance.
- 6. **Front Contact Opening and Formation**: Open contact regions on the front side of the cell for electrical connection. Follow this with sputtering, rapid thermal annealing, and SPM treatment to create a high-quality, low-resistance contact layer for efficient charge collection.
- 7. **Rear Surface Passivation**: Apply passivation layers on the rear surface of the cell, using materials like SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> to reduce carrier recombination. This passivation layer helps improve the open-circuit voltage and overall cell efficiency.
- 8. **Front Surface Passivation**: Add passivation layers on the front surface of the cell, commonly using SiO<sub>2</sub> and silicon nitride (SiN<sub>x</sub>) to minimize surface recombination and improve optical properties by acting as an anti-reflection coating.
- 9. **Single SILO-ED** (Selective Ion-implanted Layer Overlap Emitter-Device): Finalize the solar cell structure with a selective ion-implanted layer that overlaps the emitter, allowing for optimized charge collection and passivated emitter regions. This configuration includes well-defined front and rear contacts, as well as passivated surfaces to enhance the overall efficiency of the solar cell.



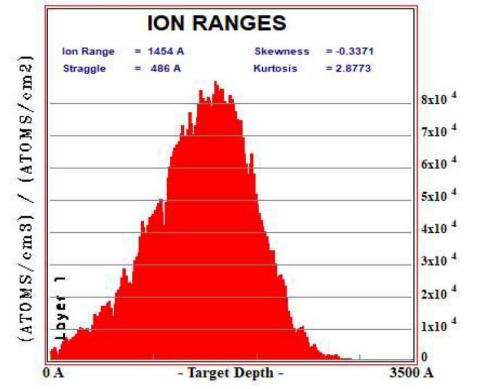
Ref: Savita Kashyap, Rahul Pandey and Jaya Madan - 25.7% efficient PERC solar cell using double side silicide on oxide electrostatically doped (SILO-ED) carrier selective contacts: process and device simulation study, *Semicond. Sci. Technol.* **38** 055010

### Dependence of the skew of the profile on the ion mass: Boron in Silicon Implantation





#### **Boron in Silicon implant**



Ion Type = B Ion Energy = 40 keV Ion Angle = 0

#### Calculation Parameters:

Transmitted lons 299.5 Vacancies/Ion ION STATS Range Straggle

**Backscattered Ions** 

Radial

Longitudinal 1454 A 486 A 443 A 551 A Lateral Proj.

691 A

345 A

Type of Damage Calculation Quick: Kinchin-Pease

Stopping Power Version SRIM-2008

**Phonons** 

% ENERGY LOSS lons Recoils 7.97 63.07 Ionization 0.25 1.24 Vacancies 0.87 26.60

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#### SPUTTERING YIELD

	Atoms/lon	eV/Atom		
TOTAL				
Si	0.000000	0.00		

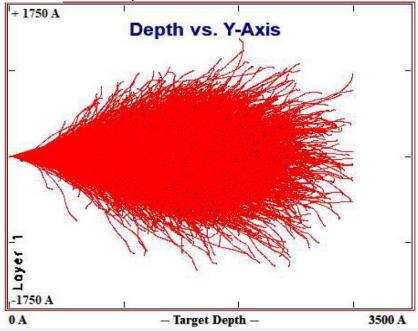
#### Target layers:

	Layer Name	Width (A)	Density	Si (28.086)	Solid/Gas	Stop Corr.
1	Layer 1	3000	2.321	1.00000	Solid	1
	Lattice Binding Energy	1		2		
	Surface Binding Energy			4.7		
	Displacement Energy			15		

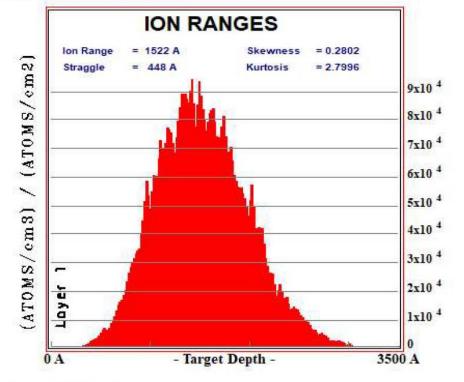
# Dependence of the skew of the profile on the ion mass: Indium in silicon implantation

lon Energy	dE/dx Elec.	dE/dx Nuclea		Longitudina Stragglin	al Lateral g Stragg	
200.00 ke 225.00 ke 250.00 ke 275.00 ke 300.00 ke 350.00 ke 375.00 ke 400.00 ke 450.00 ke	2V 1.197 2V 1.345 2V 1.568 2V 1.643 2V 1.706 2V 1.762 2V 1.815 2V 1.916	E+00 8.6 E+00 8.6 E+00 7.8 E+00 7.8 E+00 7.6 E+00 7.6 E+00 7.5 E+00 7.5 E+00 7.5 E+00 7.5	123E+00 055E+00 979E+00 899E+00 <b>315E+00</b> 730E+00 644E+00 658E+00 887E+00	966 A 1069 A 1173 A 1276 A 1379 A 1482 A 1586 A 1690 A 1794 A 2005 A 2218 A	233 A 254 A 275 A 296 A 316 A 337 A 357 A 376 A 396 A 435 A 474 A	189 A 206 A 224 A 241 A 257 A 274 A 291 A 307 A 323 A 356 A 388 A





#### Indium Silicon implant



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Ion Type = In

Ion Angle = 0

Backscattered lons **Transmitted Ions** 

ION STATS

Lateral Proj.

Radial

Vacancies/Ion

Type of Damage Calculation

Quick: Kinchin-Pease

lons

11.69

0.21

**Stopping Power Version** SRIM-2008

% ENERGY LOSS

Ionization

**Vacancies** 

**Phonons** 

Longitudinal 1522 A

Ion Energy = 325 keV

Calculation Parameters:

Range

4982.9

Straggle

448 A

317 A

222 A

Recoils

30.68

2.96

54.35

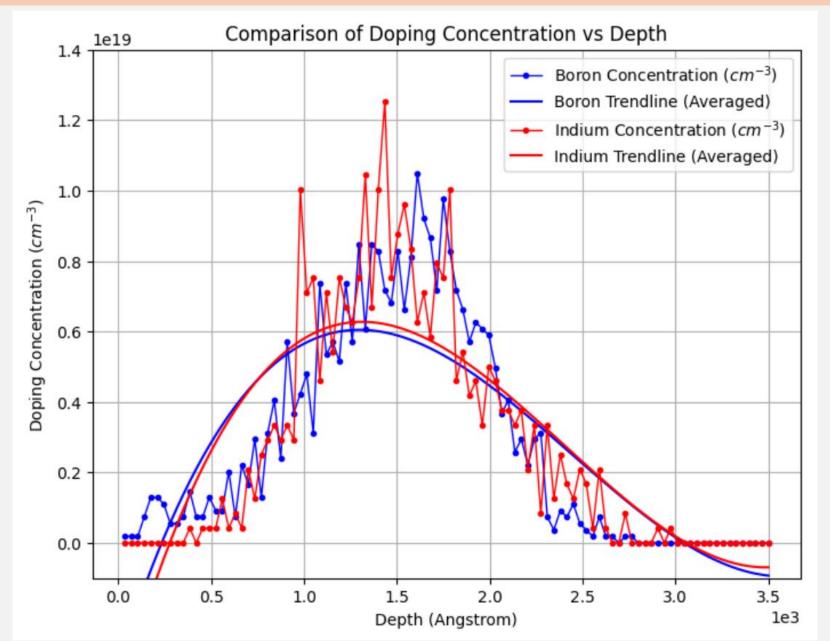
#### SPUTTERING YIELD

	Atoms/ion	eV/Atom	
TOTAL			
Si	0.000000	0.00	

# Target layers:

	Layer Name	Width (A)	Density	Si (28.086)	Solid/Gas	Stop Corr.
1	Layer 1	3000	2.321	1.00000	Solid	1
	Lattice Binding Energy			2		
	Surface Binding Energy			4.7		
	Displacement Energy			15		

Dependence of the skew of the profile on the ion mass: Comparison of doping concentration



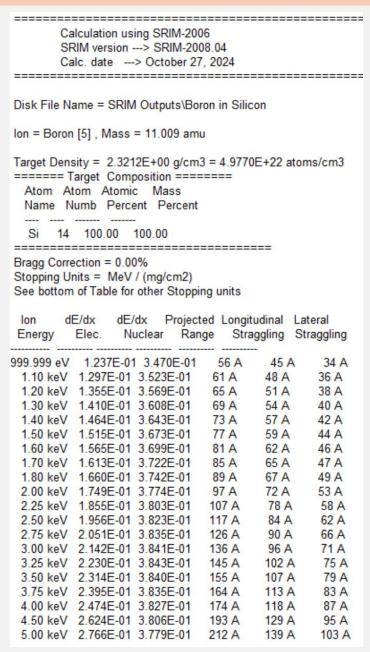
We can observe from the plot that the concentration variation of indium is slightly more shifted towards higher depth in the substrate

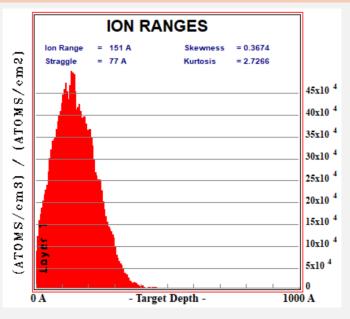
We can also observer the skewness factor from the previous slides where skewness factor for an Indium implantation is higher than that of Boron implant.

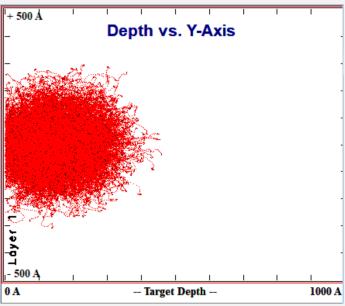
This is also reflected in their ion projectile profile whereas the plot of Boron implant is almost circular whereas the plot of Indium implant is ellipsoidal and skewed towards the depth axis

Thus, we can conclude that higher ion mass leads to a more skewed doping profile.

# Design of the thickness of poly-Si for gate application







If we assume that for no considerable effect on the threshold voltage the ion concentration in the Poly Si should become zero as we reach the channel then the minimum thickness of the Poly Si will be equal to the range which is 13.6 nm

But if we consider the recommendation of thickness of material to be equal to ~ range + 6\*straggle then our minimum thickness is

Min thickness = 
$$136 + 6*96 \text{ A}$$
  
=  $71.2 \text{ nm}$