EE669: VLSI Technology

Thermal Oxidation of Silicon

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SiO_2

Success of Si in electronic applications is attributed to the availability of the native oxide SiO_2, which:

- **Can be easily grown thermally on Si by heating in O_2 or H_2O**
- **Has an excellent interface with Si: the best in terms of electrical and mechanical properties. Low density of defects and stable with time => interface passivation.**
- **Diffusion of most of the dopants in SiO_2 is slower than in Silicon. Stopping power of SiO_2 is better than Silicon => excellent mask for diffusion and ion implantation**
- **Si can be etched selective to the oxide and vice versa => etch mask**
- **SiO_2 is resistant to most chemicals used in fabrication but can be easily etched using HF**
- **Many dielectrics can do one or more of the above, not all!**

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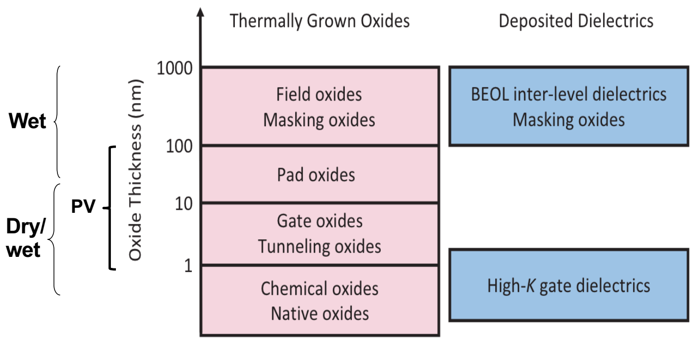
Applications of oxides in Silicon device technology



Plummer and Griffin, Integrated Circuit Fabrication: Science and Technology, 2023

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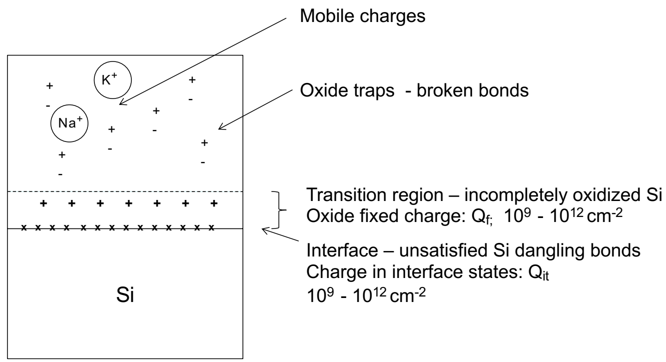
Charges and traps in thermal oxides



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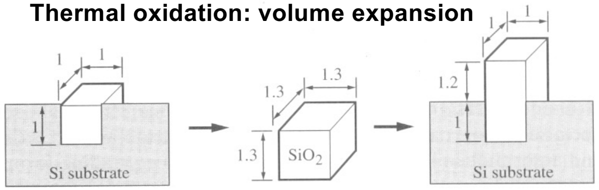
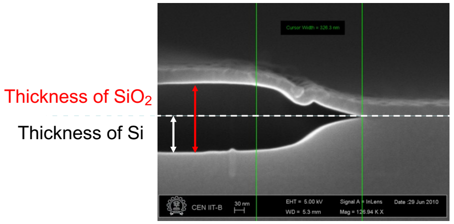
Thermal oxidation: volume expansion



J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001



CMOS team, CEN, IITB

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Exercise

At RT, how many silicon atoms are present in $2.2\ cm^3$ of SiO_2?

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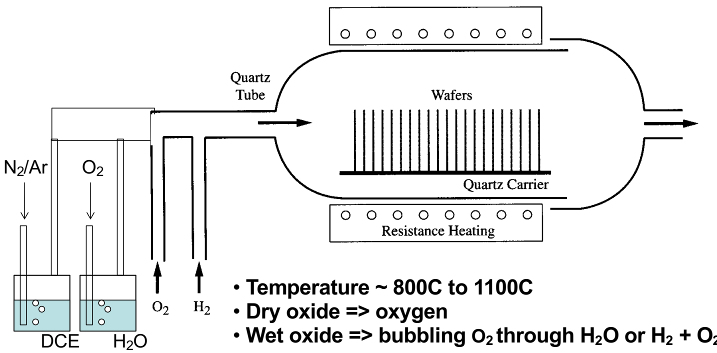
Thermal Oxidation: Typical Furnace



- Temperature ~ 800C to 1100C
- Dry oxide => oxygen
- Wet oxide => bubbling O_2 through H_2O or $H_2 + O_2$
- $C_2H_2Cl_2$ or HCl used for cleaning the tubes

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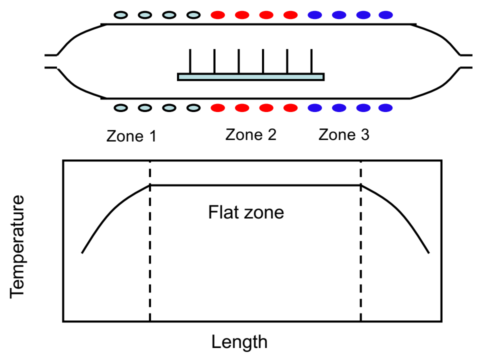
Atmospheric furnace for oxidation



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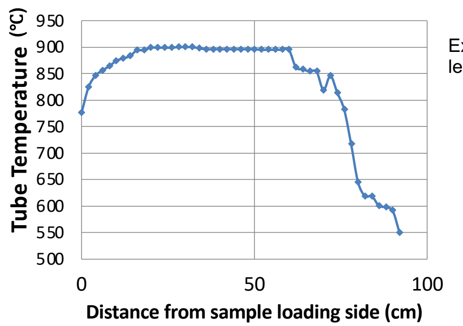
Temperature profile in a typical furnace for oxidation



Exercise: determine the length of the flatzone

Rajendra Sonawane, IITB-NF

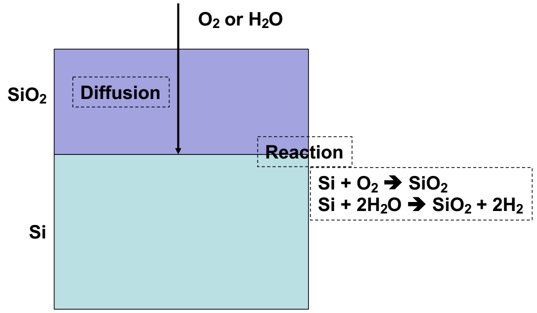
Atmospheric furnace for oxidation (3)

A typical furnace oxidation recipe:

Step	Name	Time	Temp	Gas
1.	load	11 min.	775 C	3% O2/N2
2.	stab	10 min.	775 C	3% O2/N2
3.	ramp up	10 C/min.	To 1000 C	3% O2/N2
4.	stab	20 min.	1000 C	3% O2/N2
5.	dryox	to XX nm	1000 C	O2
6.	purge	5 min.	1000 C	N2
7.	ramp down	4 C/min.	to 775 C	N2
8.	unload	16 min.	775 C	N2

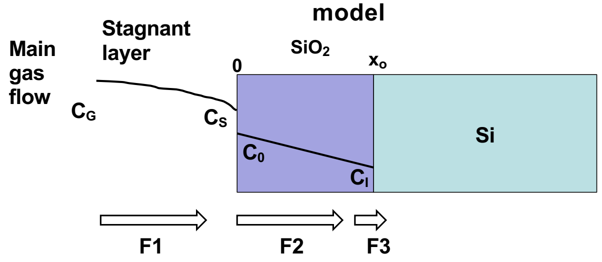
A significant amount of time is taken for ramp up, stabilization and ramp down => high and extra thermal budget.

Thermal oxidation – model



Do silicon diffuse to the surface of SiO_2 and react?

Thermal oxidation – Deal-Grove or linear parabolic model

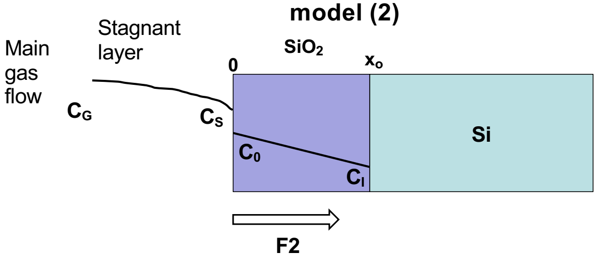


Transport from main gas flow to the surface through the stagnant layer. Not rate limiting in oxidation reactions.

Transport through the oxide, mainly by diffusion

Consumption of the oxidant species in chemical reaction

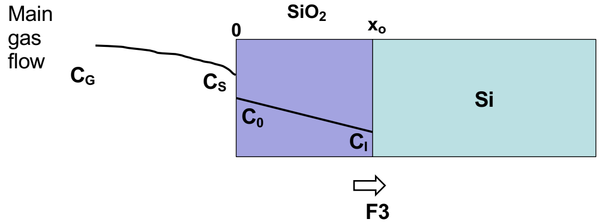
Thermal oxidation – Deal-Grove or linear parabolic model (2)



Fick's first law of diffusion

$$F2 = -D\frac{\partial C}{\partial x} = D\frac{C_o - C_I}{x_o}$$

Thermal oxidation – Deal-Grove or linear parabolic model (3)



$$F3 = k_S C_I$$

Thermal oxidation – Deal-Grove or linear parabolic model (4)

Under steady state, $F2 = F3 = F$

$$F = D\frac{C_O - C_I}{x_O} = k_S C_I$$

$$F = \frac{C_O k_S}{1 + \dfrac{k_S x_O}{D}}$$

If "N" is the number of oxidant consumed per unit volume of the film grown

$$N\frac{dx_o}{dt} = F = \frac{k_S C_0}{\left(1 + \frac{k_S x_o}{D}\right)}$$

$$N\int_{x_i}^{x_o}\left(1 + \frac{k_S x_o}{D}\right)dx_o = k_S C_0 \int_0^t dt$$

Exercise: Determine N for O_2 and H_2O

Thermal oxidation – Deal-Grove or linear-parabolic model (5)

$$\frac{x_O^2 - x_i^2}{B} + \frac{x_O - x_i}{B/A} = t$$

where $B = 2\dfrac{C_O}{N}D$

$$\frac{B}{A} = \frac{C_O}{N}k_S$$

The growth equation can be rewritten as:

$$\frac{x_O^2}{B} + \frac{x_O}{B/A} = t + \tau$$

$$\tau = \frac{x_i^2 + Ax_i}{B}$$

Thermal oxidation – Deal-Grove or linear parabolic model (6)

$B = C_1 \exp(-E_1/kT)$

$B/A = C_2 \exp(-E_2/kT)$

Values for (111) surface are given below. C_2 values for (100) is obtained by dividing the given values by 1.68

Ambient	B	B/A
Dry O_2	$C_1 = 2.1 \times 10^{-9}$ cm^2 s^{-1}	$C_2 = 0.17$ cm s^{-1}
	$E_1 = 1.23$ eV	$E_2 = 2.0$ eV
H_2O	$C_1 = 1.0 \times 10^{-9}$ cm^2 s^{-1}	$C_2 = 4.52$ cm s^{-1}
	$E_1 = 0.78$ eV	$E_2 = 2.05$ eV

In case of a mixture of H_2O and O_2, the values would be somewhat different.

J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001

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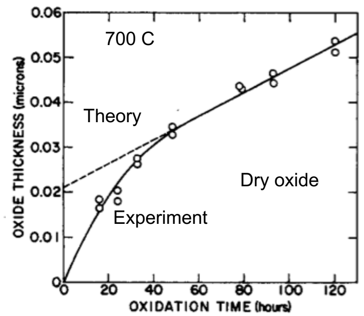
Thin oxide growth – departure from D & G model



Deal and Grove, Journal of Applied Physics, 1965, pp. 3770.

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Models for thin oxide growth

1. Drift component in addition to the diffusion component
   - drift in the field set up by the dissociation of O_2 into O_2^- and 2h
   - Holes would move faster than O_2^-, resulting in a field that drives O_2 faster
   - The field acts over the extrinsic Debye length

$$L_D = \sqrt{\frac{kT\varepsilon}{2q^2C}}$$

2. Massoud model

$$\frac{dx_o}{dt} = \frac{B}{2x_o + A} + C_M e^{(-x_o/L)}$$

where $$C_M = C_M^0 e^{(-E_A/kT)}$$

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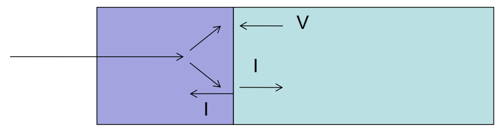
Point defect generation during oxidation

- Non local phenomena are seen during oxidation, the prominent ones being oxidation enhanced diffusion and oxidation retarded diffusion far from the oxidizing surface

- The growth result in volume expansion => more room required to accommodate the growing oxide.
  - Result in stress
  - One way to relax the stress is by creation of point defects
  - SiO_2 forms by absorption of vacancies and creation of interstitials

$$(1 + 2\gamma)\, Si + 2O_I + 2\beta V \Leftrightarrow SiO_2 + 2\gamma I + \text{stress}$$



J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001

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Point defect generation during oxidation

- Higher concentration of vacancies can enhance oxidation reaction
- Thin oxide growth can be significantly enhanced or retarded based on the availability of vacancies
- Other substrate conditions that favor creation of vacancies would enhance or differentiate thin oxide growth rate

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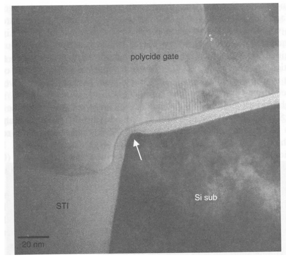
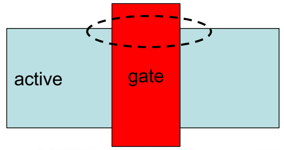
Growth on 2D non planar surfaces (integration)

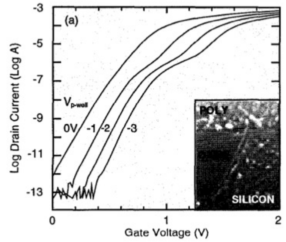
Example: STI



STI corner

C.-H. Tung, G. T. T. Sheng and C.-Y. Lu, ULSI Semiconductor Technology Atlas, Wiley Interscience, 2003

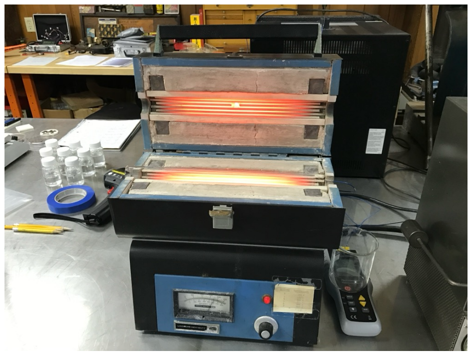




Perera et al., IEDM 1995, pp. 679.

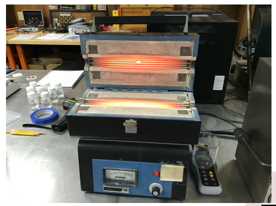
Enhanced visco-elastic flow of SiO_2 at high temperature relieve stress generated during oxidation and reduce corner thinning in STI

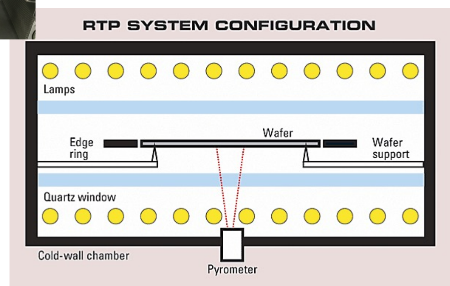
Tube furnace



Sam Zeelof, sam.zeelof.xyz
"It's not enough to have a dream, you have to have a garage."

How to reduce the thermal mass?





CeNSE, University of Kentucky

Rapid Thermal Oxidation

Ultra thin oxides for ULSI gate applications on large wafers

Name	Time	Temp	Gas
1. Load&stab	190 s	550 C	---
2. R/U&stab	20 C/s, max 30s	to 620C	N2
3. R/U&stab	75 C/s, max 30s	850C	N2
4. R/U&stab	50 C/s, max 30s	900C	N2
5. R/U&stab	25 C/s, max 30s	1000C	N2
6. Oxidation	XX sec	1000C	O2/N2
7. R/D	50 C/s	550C	N2

Rapid thermal process chamber

Applied Materials Inc.

Rapid Thermal Oxidation

Rapid thermal process

Name	Time	Temp	Gas
1. Load&stab	190 s	550 C	---
2. R/U&stab	20 C/s, max 30s	to 620C	N2
3. R/U&stab	75 C/s, max 30s	850C	N2
4. R/U&stab	50 C/s, max 30s	900C	N2
5. R/U&stab	25 C/s, max 30s	1000C	N2
6. Oxidation	XX sec	1000C	O2/N2
7. R/D	50 C/s	550C	N2

furnace

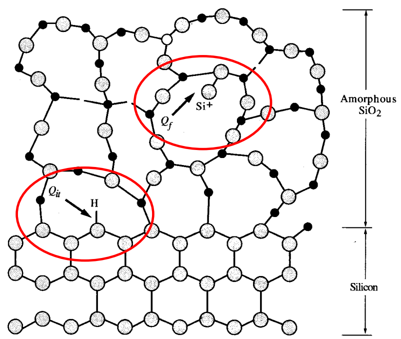
Step	Name	Time	Temp	Gas
1.	load	11 min.	775 C	3% O2/N2
2.	stab	10 min.	775 C	3% O2/N2
3.	ramp up	10 C/min.	To 1000 C	3% O2/N2
4.	stab	20 min.	1000 C	3% O2/N2
5.	dryox	to XX nm	1000 C	O2
6.	purge	5 min.	1000 C	N2
7.	ramp down	4 C/min.	to 775 C	N2
8.	unload	16 min. 775 C	N2	

Passivation of Si – SiO_2 interface

- Oxide fixed charges
  - Post growth anneal in Ar ambient at ~ 1000C is known to reduce the fixed charge density
  - Probably due to rearrangement of microscopic structure at the interface that reduce missing bonds
- Interface state density can be reduced by annealing the device at 300 – 500 C in H_2 ambient for ~ 30 min
  - H_2 ⇔ 2H
  - ≡Si• + H ⇔ ≡SiH
  - The reaction is reversible and hence the temperature has to be limited
  - Forming gas, 90% N_2 + 10% H_2, usually used due to safety concerns

J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001

Si - SiO_2 interface passivation



J. D. Plummer, M. D. Deal, P. G. Griffin, Silicon VLSI Technology, Pearson Education, 2001

Summary

- Applications of oxide in VLSI and deposition techniques
- Structure and defects
- Overview of oxidation furnace and process
- Deal – Grove model for oxidation
- Deviations from Deal – Grove model
    - Thin oxide regime
    - Point defects and doping effects
    - Dependence on pressure
    - Surface orientation dependence
    - Mixed ambients for oxidation
    - 2D and 3D effects → Case study
- Rapid Thermal Oxidation

Simulation exercise