



## **Lithography Masks**



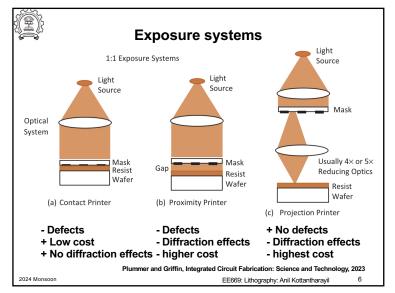
- Substrate material is transparent to light: glass, transparency sheets
- The opaque layer: chrome, black ink
- · Maskless lithography is possible for low throughput applications

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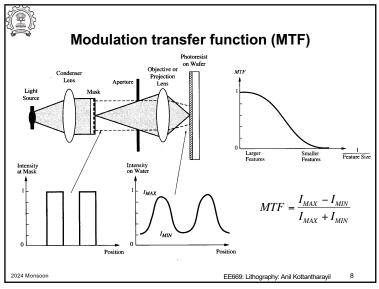
EE669: Lithography: Anil Kottantharayil

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General Technology Trends									
Tr. on the	2007	2000	2000	2010	2011	2012	2012	2014	2015
Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
DRAM ½ pitch (nm) (contacted) DRAM and Flash	65	57	50	45	40	36	32	28	25
DRAM ½ pitch (nm)	65	57	50	45	40	36	32	28	25
Flash ½ pitch (nm) (un-contacted poly)	54	45	40	36	32	28	25	23	20
Contact in resist (nm)	72	62	55	50	44	39	35	31	28
Contact after etch (nm)	65	57	50	45	40	36	32	28	25
Overlay [A] (3 sigma) (nm)	13	11.3	10.0	9.0	8.0	7.1	6.4	5.7	5.1
CD control (3 sigma) (nm) [B]	5.6	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1
MPU									
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	68	59	52	45	40	36	32	28	25
MPU gate in resist (nm)	42	38	34	30	27	24	21	19	17
MPU physical gate length (nm) *	25	23	20	18	16	14	13	11	10
Contact in resist (nm)	84	73	64	56	50	44	39	35	31
Contact after etch (nm)	77	67	58	51	45	40	36	32	28
Gate CD control (3 sigma) (nm) [B] **	2.6	2.3	2.1	1.9	1.7	1.5	1.3	1.2	1.0
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