EE 724: HW 2

Practice Problems (no need to submit – just ensure that you can solve these)

Griffiths: Practice Problems: Example 4.1, Problem 4.1-4, Example 4.4

Griffiths, Reproduce Examples 3.3-5. Solve 3.12-15

Problems to submit After each sub-problem- write down 1 sentence of principle verified or applied.

1. In between two concentric metal spherical shells of radius r_i=5nm and r_o=15nm there are 3 cases
    a. There lies a dielectric with dielectric constant of $\varepsilon_1 = 10*\varepsilon_o$. A potential difference of 5V is applied to the outer cylinder.
    b. There are 2 concentric dielectrics of dielectric constant $\varepsilon_1 = 10*\varepsilon_o$ (r<10 nm) and $\varepsilon_2 = 30*\varepsilon_o$ (r>10 nm). A potential difference of 5V is applied to the outer cylinder.

    For each case, analytically solve and draw the charge density, Electric Field and Potential profile vs radius. Plot with MATLAB. Solve for capacitance.

    Show that b & c parts can be easily solved alternatively by a capacitive network.

    Note: Similar electrostatics maybe seen in metal nanoparticles surrounded by dielectrics. Electrodes are used in single electron transistors (SETs).

    c. Given a case (a), if 1 electron is transferred from from outer to inner shell, how much energy does the next electron transfer need? This increase in energy for each additional electron is known as coulomb blockade to injection. How does it depend on radius of the inner and outer shells? Plot using MATLAB, energy vs. inner radius. Annotate the radius at which energy exceeds thermal energy of 25mV at 300K. At these radii, the coulomb blockade can be observed at room temperature in nano-scale SETs.

2. ***<Practice problem – no need to submit>*** In between two concentric metal cylinders of radius r_i=5nm and r_o=15nm there are 3 cases
    a. There lies a dielectric with dielectric constant of $\varepsilon_1 = 10*\varepsilon_o$. A potential difference of 5V is applied to the outer cylinder.
    b. There are 2 concentric dielectrics of dielectric constant $\varepsilon_1 = 10*\varepsilon_o$ (r<10 nm) and $\varepsilon_2 = 30*\varepsilon_o$ (r>10 nm). A potential difference of 5V is applied to the outer cylinder.
    c. There is a fixed charge of density $\sigma=10^{12}/cm^2$ at between r_q=11nm. A potential difference of 0V is applied to the outer cylinder. Also solve for 5V potential difference.

For each case, analytically solve and draw the charge density, Electric Field and Potential profile vs radius. Plot with MATLAB. Solve for capacitance.

Show that b & c parts can be easily solved alternatively by a capacitive network.

Qualitatively verify using Matlab PDE solver.

Note: Such electrostatics is seen in nanowire FETs where the nanowire channel is surrounded by a concentric gate dielectric and electrode. When the device is on, the channel has many conductors and can be approximated as a metal.

3. ***<Practice problem – no need to submit>*** Two electrodes start at origin and extend to +x and +y to infinity (i.e. perpendicular to each other) with a bias of 5V across them.
   a) For the 1st quadrant (Note: this is like the Gate/Source or Gate Drain capacitance that is a parasitic capacitance).
   b) For the rest of the quadrants
   c) If each quadrant has dielectrics with different dielectric constant (as opposed to same dielectric constant in a & b)

   For each case, analytically solve and draw the charge density, Electric Field and Potential profile vs radius. Plot with MATLAB.

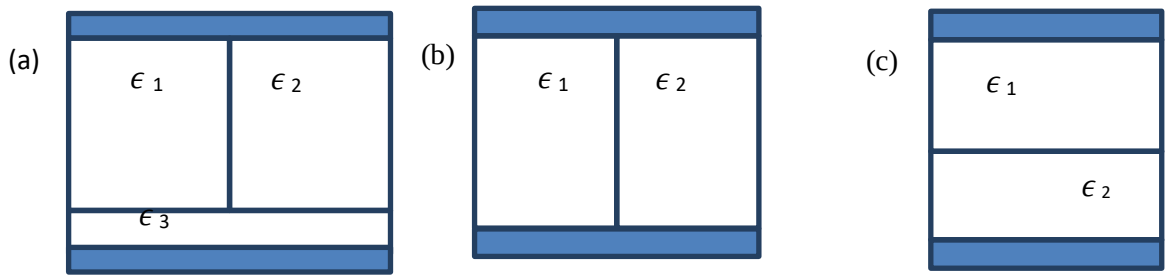
   Solve for the total capacitance.

   Can (c) be solved by capacitor network easily?

   Qualitatively verify using Matlab PDE solver.

   For 3 (a), identify the outer radius by which the charge reduces to 10% of the inner radius. Note that this outer radius captures 90% of the capacitance; So, the plates do not need to be infinite for this approximation to be valid.

4. In which parallel plate capacitor shown below, capacitor network may not be used. Confirm with MATLAB PDETOOL simulations.
   In each of the examples, plot (a) equipotential surfaces (b) iso-electric field lines. Comment on how we can derive or draw one if we know the other.



5. For a finFET of gate length 15nm node and approximate it as infinitely tall fin-height.

a) Derive the expression for V(x,y) at V_G=5V and (i) V_D=V_S=0V; (ii) V_D=-5V, everything else is same;

Plot V(x,y) is matlab using "meshgrid comment and 3D plots". Compare the shape with the PDEtool box solution.

b) Find out analytically $\frac{dV_b}{dV_G}$ at V_G=5V and low V_{DS} which is a measure of gate control of effective barrier position (i.e. V_b). Plot $\frac{dV_b}{dV_G}$ vs. finwidth and find the finwidth limit for 90% effectiveness in barrier control by gate.

c) Find out analytically $\frac{dV_b}{dV_D}$ at V_G=5V and high V_{DS} which is a measure of drain control. Assume that barrier is minimum at the center and its position is voltage independent (an approximation whose validity you can check based on part d). Plot $\frac{dV_b}{dV_D}$ vs. finwidth and find the finwidth limit for 90% effectiveness in barrier control by gate.

d) How does barrier position change as a function as VDS becomes more negative? Write a algorithm and implement it in Matlab to plot V_b vs V_{DS} and x(barrier), y(barrier) vs V_{DS}. Check experimentally based on PDEtool box quantitatively (i.e. plot expt vs calculated).

e) If there is fixed charge (e.g. ionic cores during depletion), how does it affect the above analysis?

f) If there is finite gate oxide thickness (t_{ox}), how does it affect the above analysis for Vbarrier calculations?

g) For V at center, can a capacitive divider model be created? What is the error compared to 1D models for capacitors compared to capacitances derived from Laplace solutions.

6. ***<Practice problem – no need to submit>*** For a nanowire FET of gate length 15nm with a *square* cross-section of finside "a" nm. Repeat part (b) and (c) to show which device has better gate control and poorer drain control? At what dimension (finwidth vs. finlength) do the devices perform similarly i.e. which device requires more scaled features for same performance.

7. Please explain why even without free charge, potential V(x,y) has a saddle point behavior in 2D or 3D?

8. A TCAD exercise on FinFETs will be introduced later.