EE 724: Electrostatics

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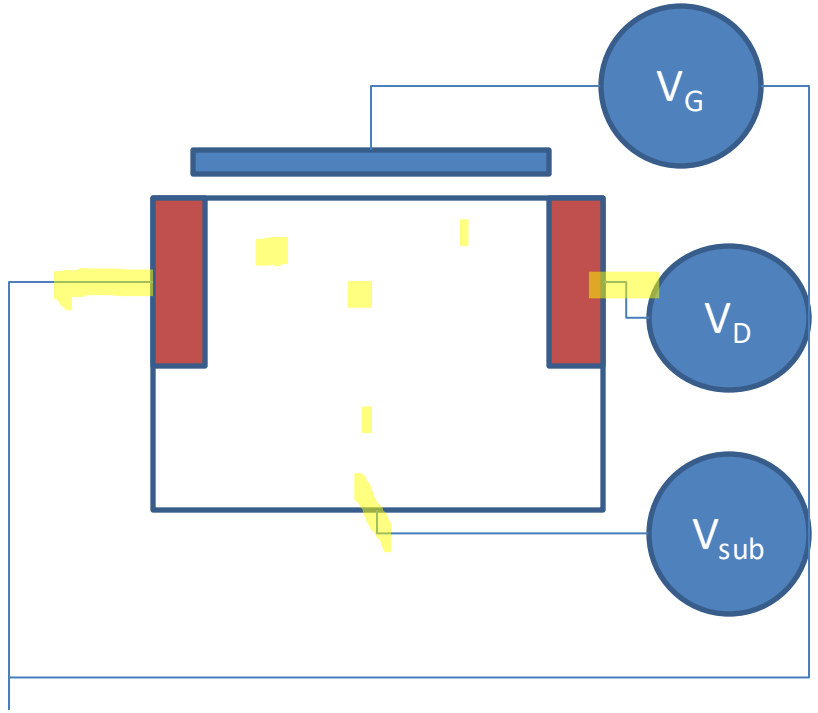
Based on Griffiths “Electrodynamics” Ch 2-4.

Assumptions

- This section assumes that there is metal and insulator.
- Semiconductors are not yet introduced.

Why electrostatics?

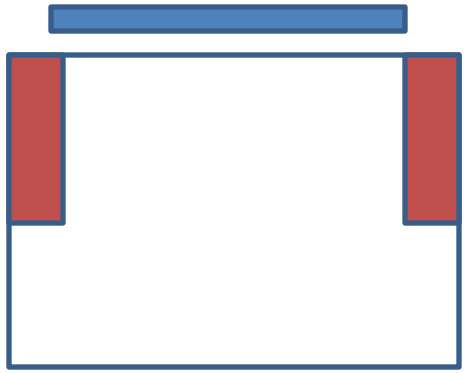
- Electrostatics represents the force (motivation) for current flow
- Force is “local”



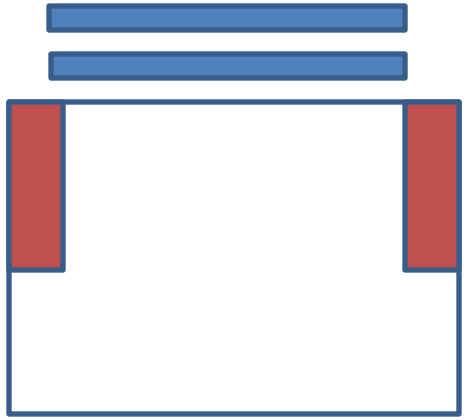
- Electrostatics is only set by “global” interfaces = contacts

Need to find local potential/electric field – given external V-supplies

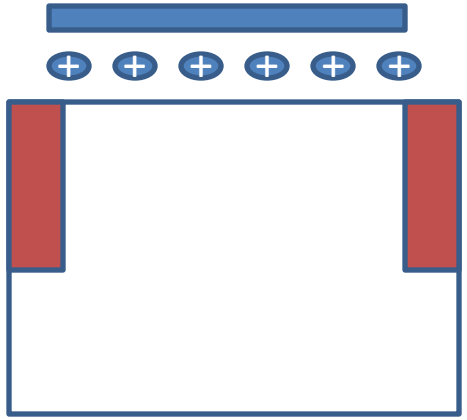
Various MOSFET Devices



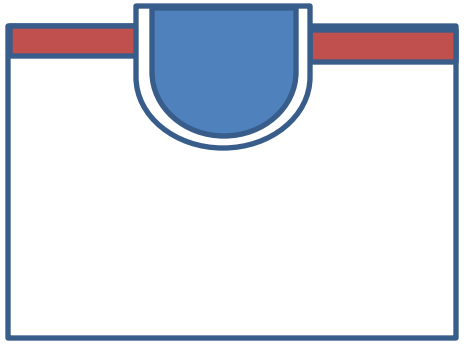
Planar



FG Flash

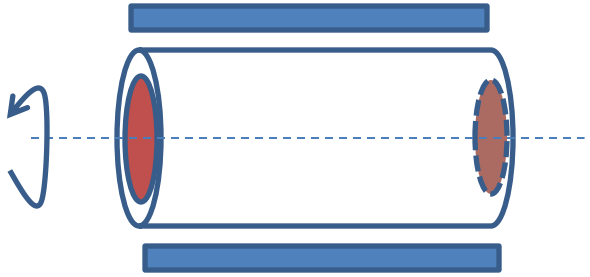


Charge Trap Flash

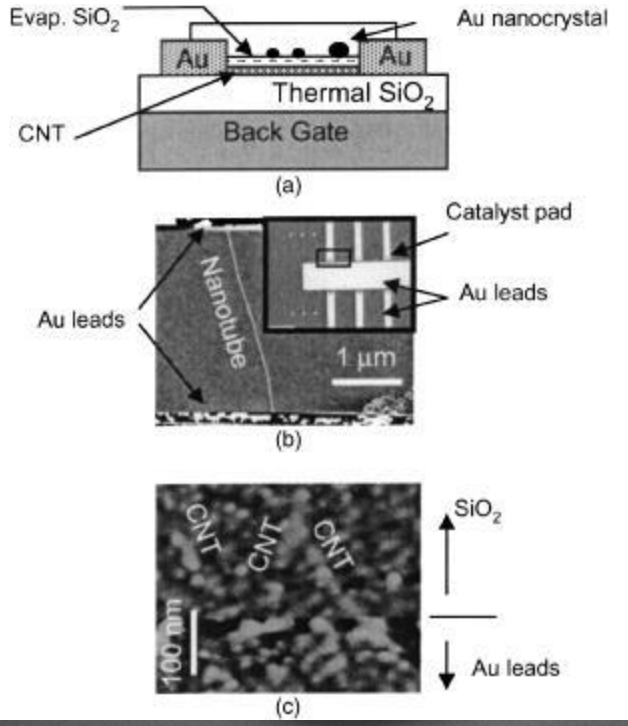


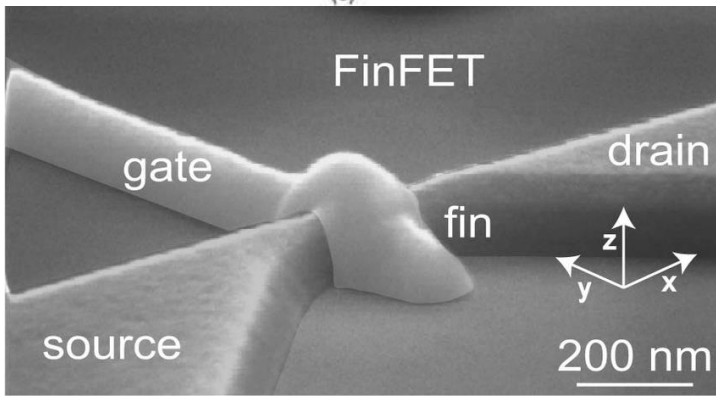
DRAM Access Xtor

SOI FET



FinFET / Nanowire





Common materials are :
Metals, Insulators, Semiconductors arranged in <u>different</u> structures

Electrostatics - Plan

What is exciting about nanoscale transistors ➔ things change at small scales… what is the *reference* of small? Do all things change with scale?

<u>No Length Scale</u>

1. Conductor & Vacuum (no length-scale)
2. Dielectrics (polarization-no length-scale)

Example

➔ Gate Stack

➔FinFETs

<u>Fundamental Length scales</u>

3. Bound charges (depletion length)
4. Free carrier screening (Debye length)

Examples

➔Depletion approximation in MOSCAP

➔Inversion in MOSCAP

Electrostatics: Charge in Space

- Electrostatic Field = action at a distance

<u>Properties of Field</u>

- It flows i.e. field line are conserved
- Gauss Law define source/sink of Electric field: Field lines start in +ve charge and end in –ve charge;
- Stoke Law shows that field line do not cross itself: Field lines repel each other
  - Compare for magnetic field

Gauss Law:

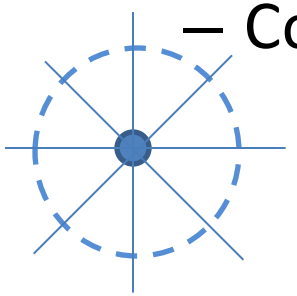
$$\oint_S \mathbf{E} \cdot d\mathbf{a} = \frac{1}{\epsilon_0} Q_{\text{enc}},$$

$$\nabla \cdot \mathbf{E} = \frac{1}{\epsilon_0} \rho.$$

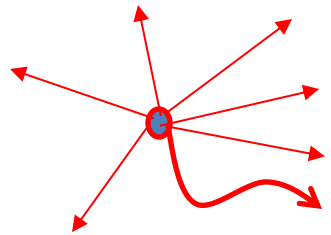
Stoke's Law:

$$\oint \mathbf{E} \cdot d\mathbf{l} = 0,$$

$$\nabla \times \mathbf{E} = 0.$$



Èxample: What is the error?
What laws does it violate?
Modify the image for a Gauss Law violation

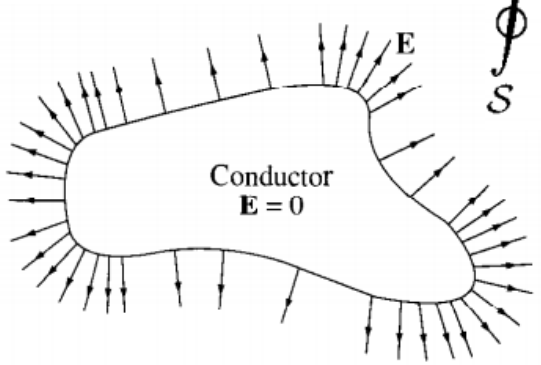


$$\boxed{\nabla \cdot \mathbf{B} = 0.}$$

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{J}.$$

E'Statics Media: Metal vs. Dielectrics

- Charge inside a medium
  - Free charge (Metal, semiconductor)
  - Bound charge (doping, polarization)
- Metal surface
  - Electrons are free
  - Surface is equipotential.
  - Field line are always normal to metal surface. Why?
    - If not, then parallel component of E field (i.e. not equipotential) will cause electron flow until parallel component is zero.
- Dielectric interfaces
  - D_{normal} is conserved. What is the proof? $\mathrm{D} = \epsilon_o E + P = \epsilon E$ and
    - See Gauss Law using D
  - $E_{parallel}$ is conserved. What is the proof?
    - See Stokes Law



$$\oint_S \mathbf{E} \cdot d\mathbf{a} = \frac{1}{\epsilon_0} Q_{\text{enc}},$$

$$\oint \mathbf{E} \cdot d\mathbf{l} = 0,$$

Dielectric Polarization

Dielectric are locally polarized by electric field $\mathbf{p} = \alpha \mathbf{E}.$ $\mathbf{P} = \epsilon_0 \chi_e \mathbf{E}.$

Experimentally determined polarizability

H	He	Li	Be	C	Ne	Na	Ar	K	Cs
0.667	0.205	24.3	5.60	1.76	0.396	24.1	1.64	43.4	59.6

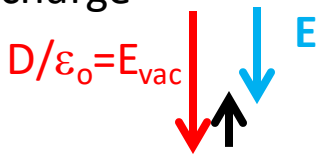
$$\mathbf{D} = \epsilon_0 \mathbf{E} + \mathbf{P} = \epsilon_0 \mathbf{E} + \epsilon_0 \chi_e \mathbf{E} = \epsilon_0 (1 + \chi_e) \mathbf{E},$$

Electric field depends upon all charge

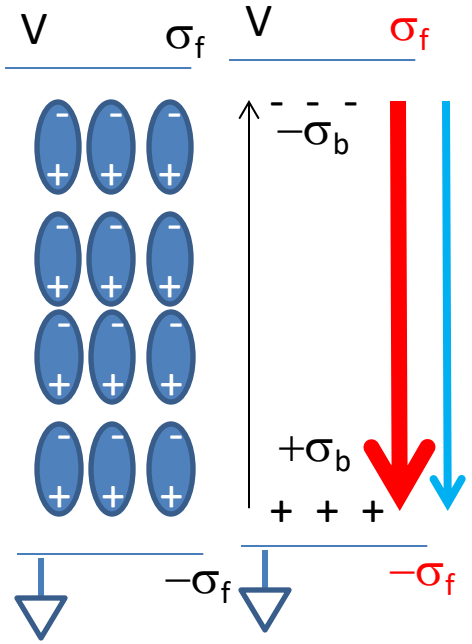
$$\epsilon_0 \nabla \cdot \mathbf{E} = \rho = \rho_b + \rho_f = -\nabla \cdot \mathbf{P} + \rho_f$$

Electric Displacement depends only on free charge

$$\nabla \cdot \mathbf{D} = \rho_f,$$



P/ε$_o$=E$_{vac}$$X$



Q: What is the direction of atomic polarization

Q: Draw charge & field lines inclusive of dipoles to show that E-field reduces in dielectric

Q: Is the reduced field uniform?

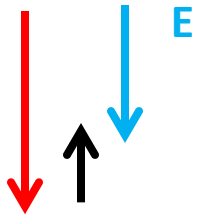
Field is uniform beyond a few atomic scale; but non-uniform at atomic scale

Microscopic vs. effective picture

Why is picture 2 more correct?

$D/\varepsilon_o = E_{vac}$

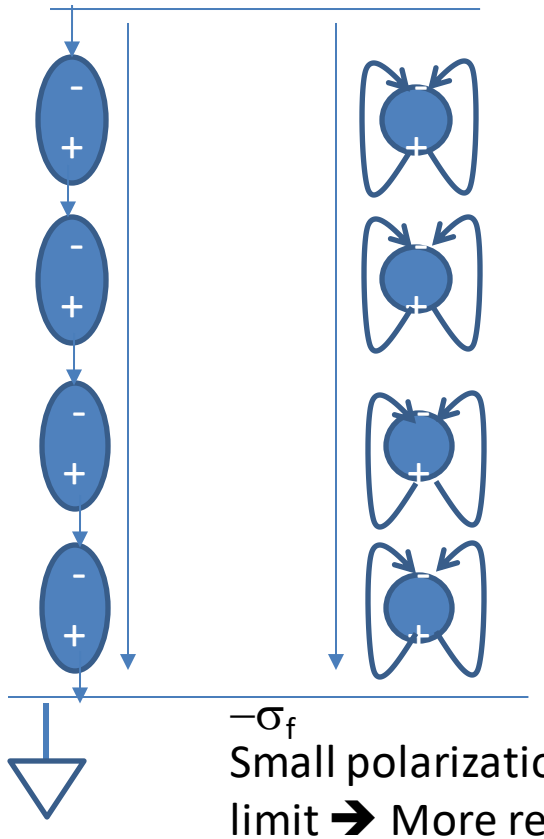
$P/\varepsilon_o = E_{vac} X$



Large polarization limit ➔ Not realistic

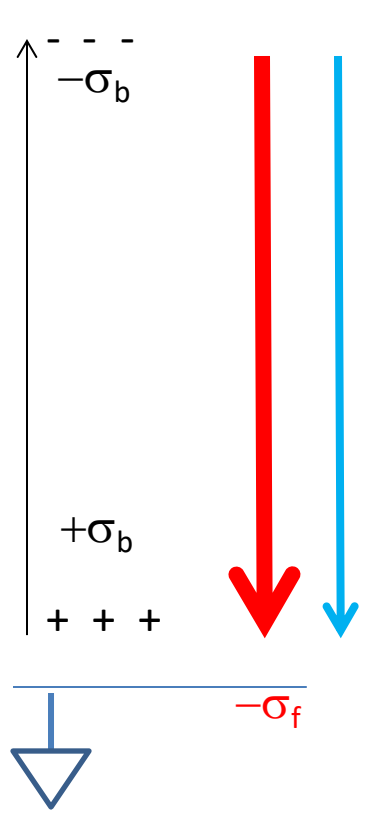
Picture 1:
No field inside the atom

Picture 2:
Polarization field opposes Applied Field



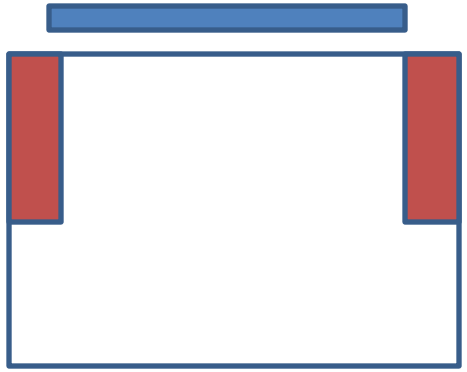
Small polarization limit ➔ More realistic

Microscopic

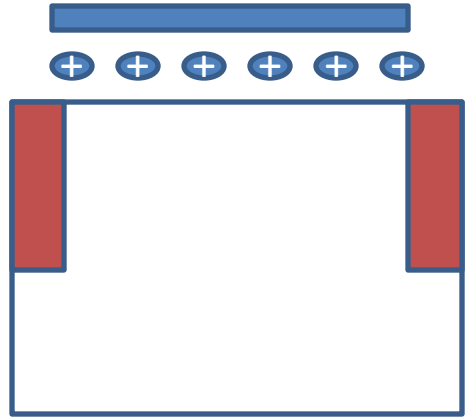


effective

Simple capacitors in Nanoelectronics



Planar



Charge Trap Flash

We will simplify to assume that silicon is a metal.
We will later correct for silicon as a semiconductor

$\vec{\nabla}V = -E; \vec{\nabla}.\vec{E} = \rho/\epsilon$

1D Capacitor

1. Microscopic soln

In a capacitor, if a potential V is applied across it;

Q: Show that the field outside is zero

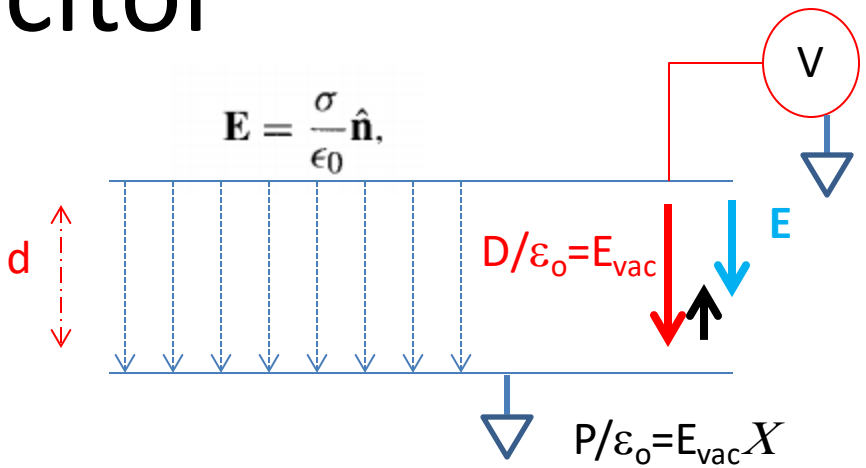
C=Q/V depends upon surface charge on conductor;

1. Draw charge, electric field, potential due to
   - Free charge
   - Polarization charge
2. Use superposition to show final effect

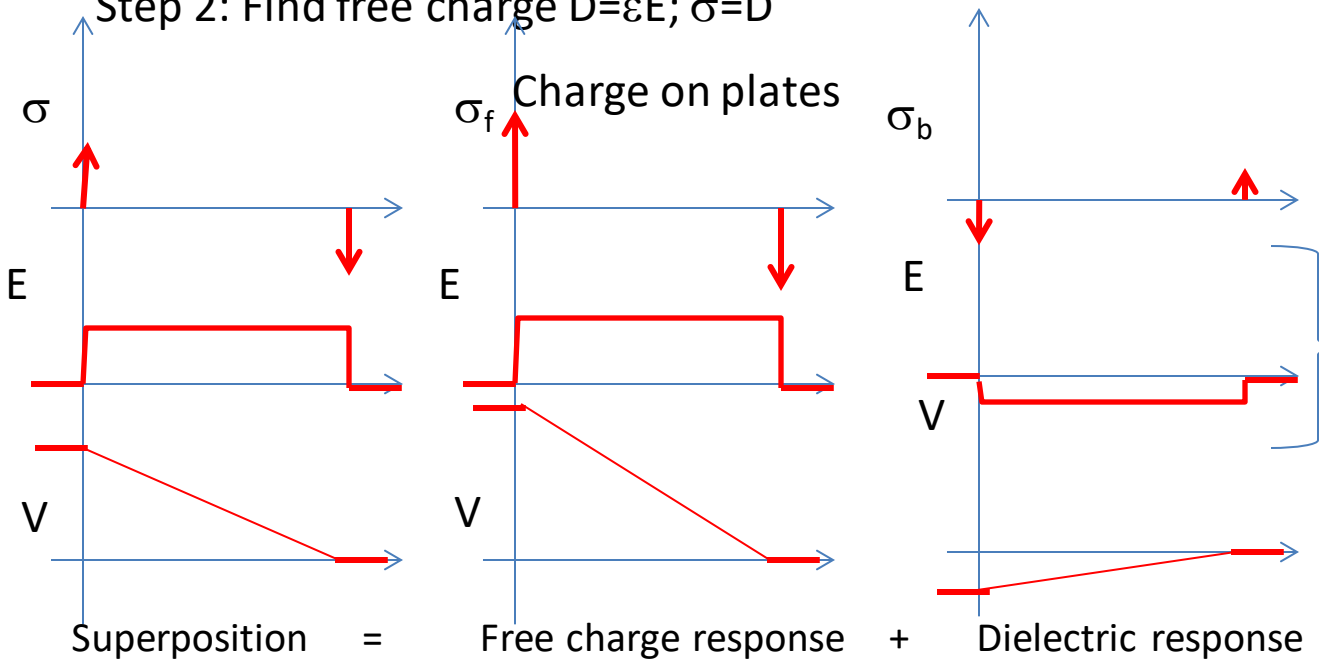
Solution:

Step 1: Find E=V/d

Step 2: Find free charge D=εE; σ=D



2. Graphical soln



Two kinds of problems are possible: (i) Given charge find voltage

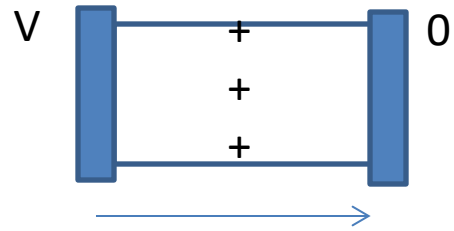
(ii) Given V, find charge

In both cases, connection is through E field relations as E, E_{vac}, P are relation is known

3. Analytical Soln

$C=\frac{\epsilon A}{d}; Q = CV$

Exercise

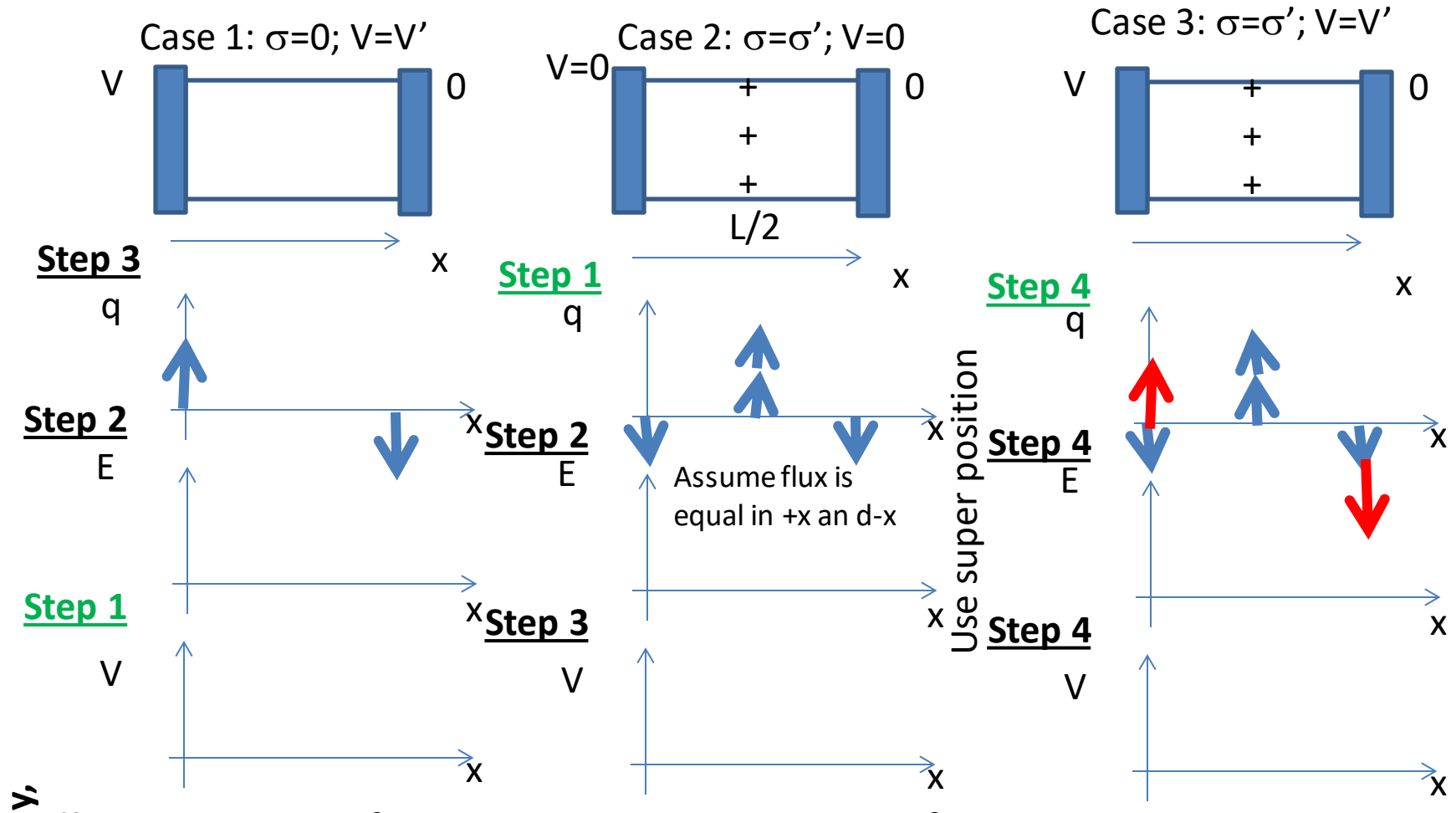


1. In a MIM capacitor; if a bias V is applied then what is charge and electric field?
2. Removing the bias, if there is a fixed charge sheet σ (/cm^2), added at x=d/2; calculate max(V). What is the V(x);
3. How would max(V) change with x=d/3?

(Strategy: can you divide this into two capacitors? Justify)

1. Calculate and draw potential profile V(x) if both fixed charge and bias is applied simultaneously.

2 approaches: Gauss Law/Poisson's Eqn. Vs Circuit

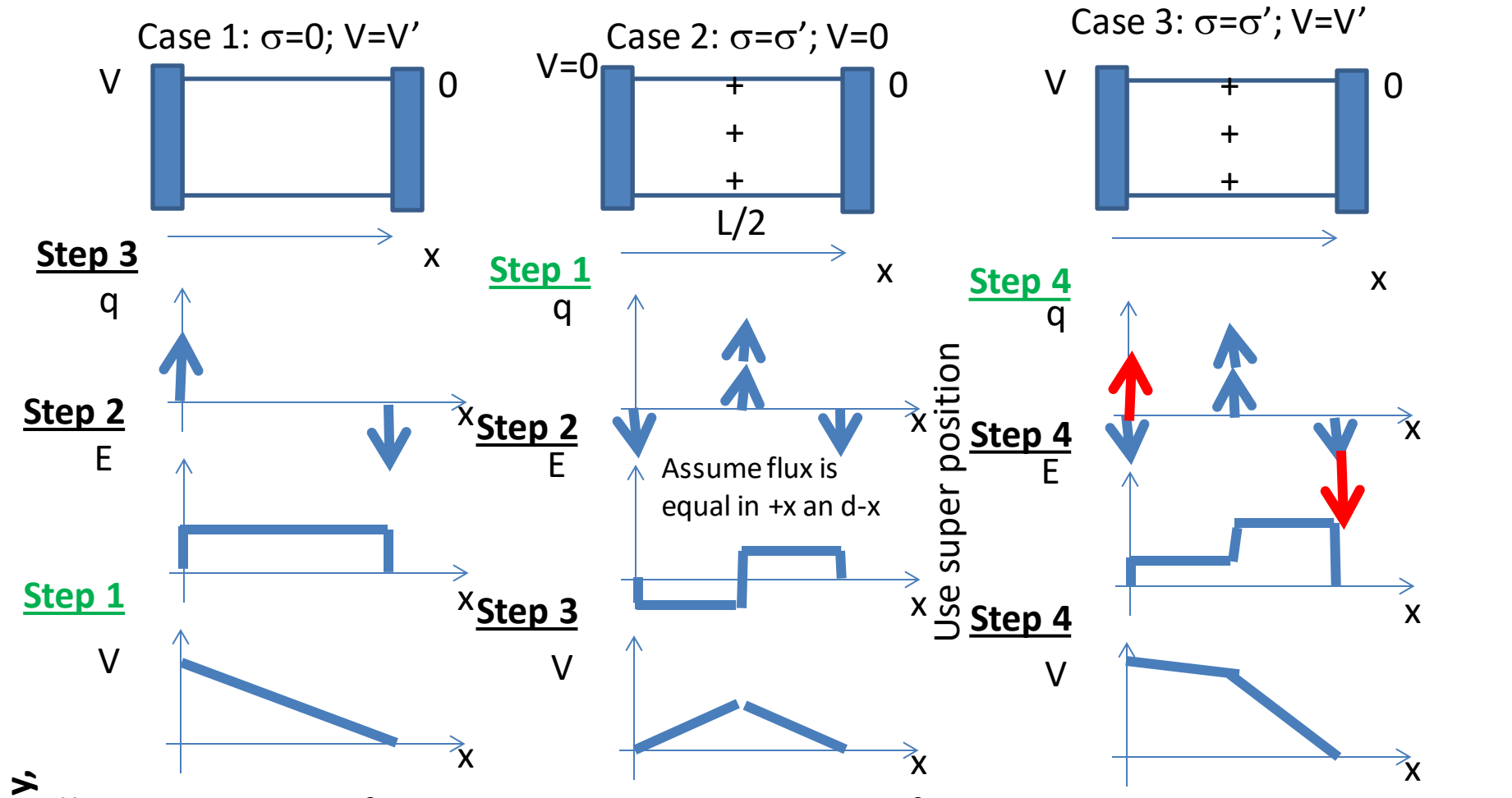


Alternatively, use circuits;

Step 1: Extract C from structure
Step 2: relate V, Q i.e Q=CV

Step 1: Extract C from structure
(note difference in circuit)
Step 2: relate Q, V i.e Q=CV

2 approaches: Gauss Law/Poisson's Eqn. Vs Circuit



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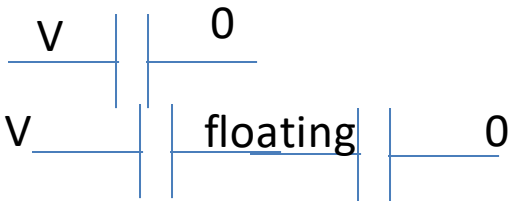

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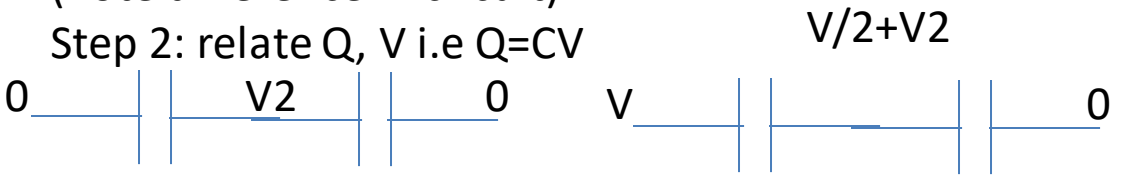
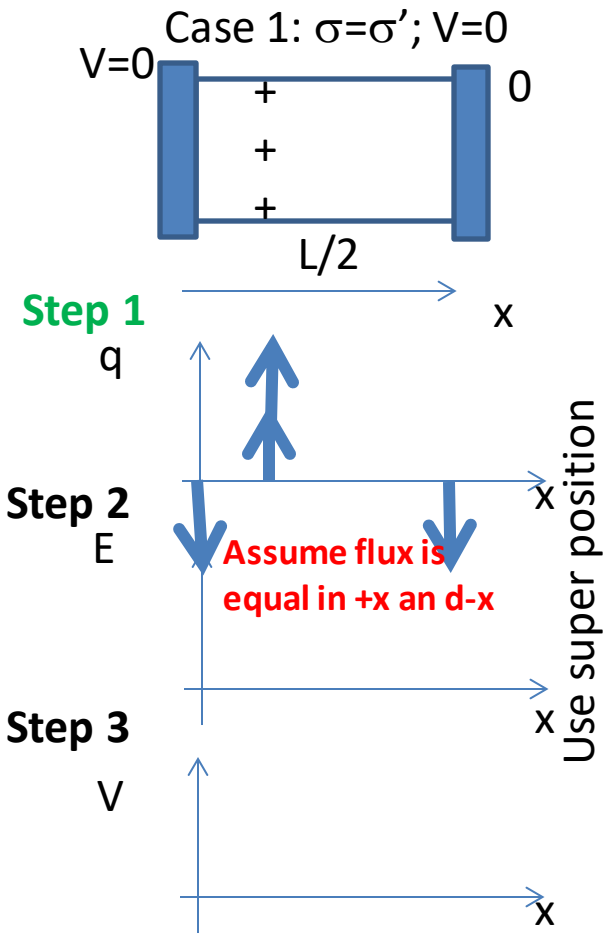
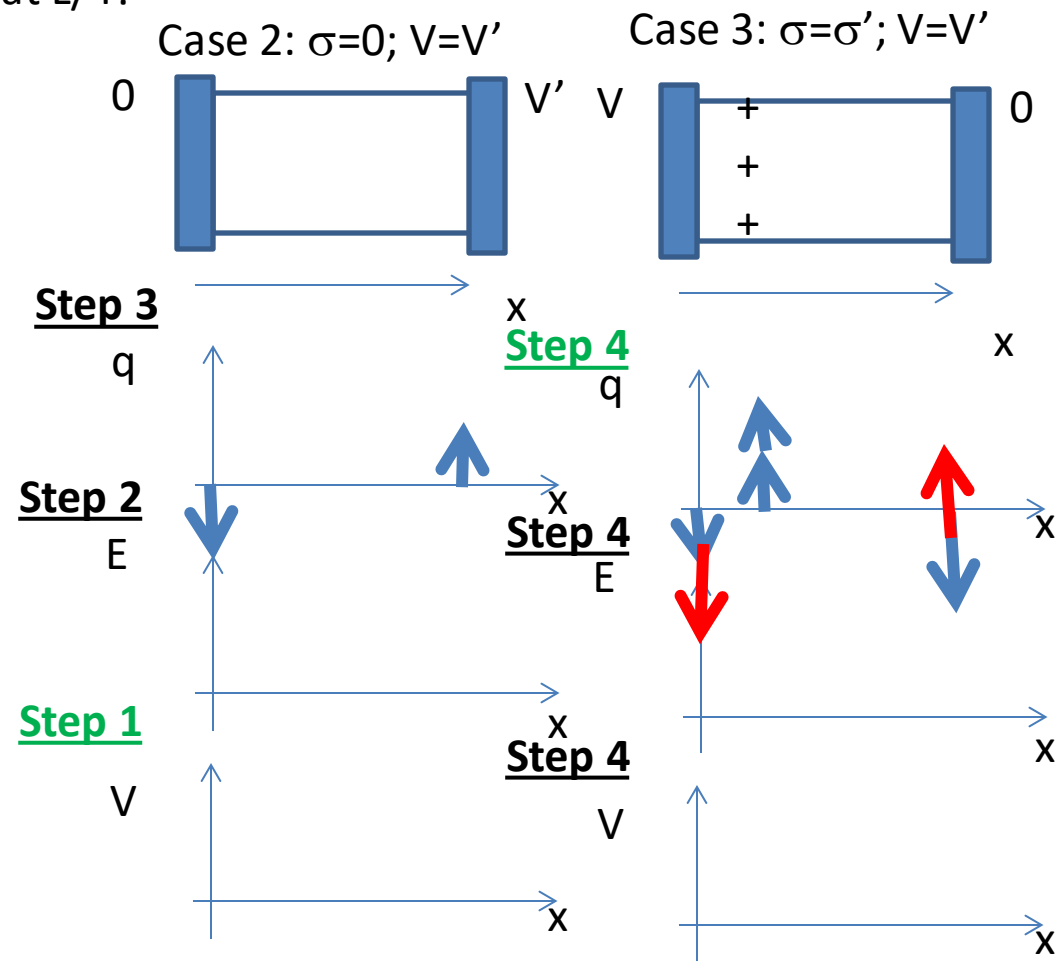


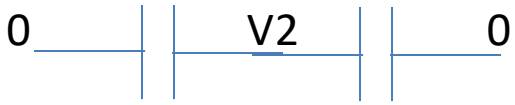
Another example

What is σ is not at center i.e. say at L/2?





Alternatively; capacitor circuit is used



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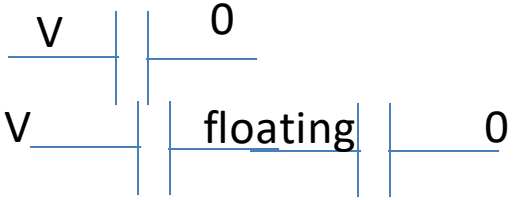
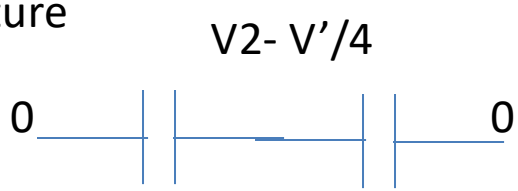
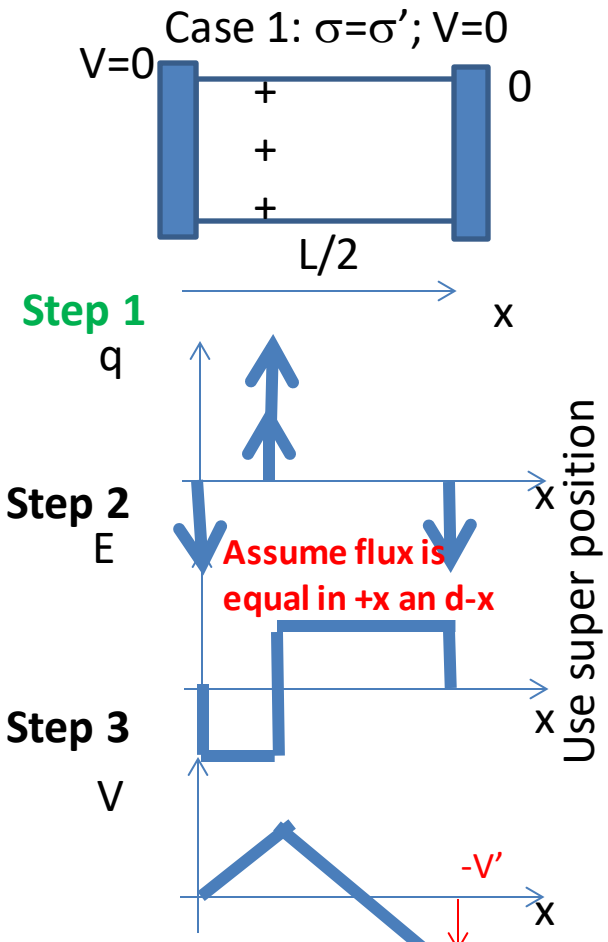
Step 2: relate V, Q i.e Q=CV

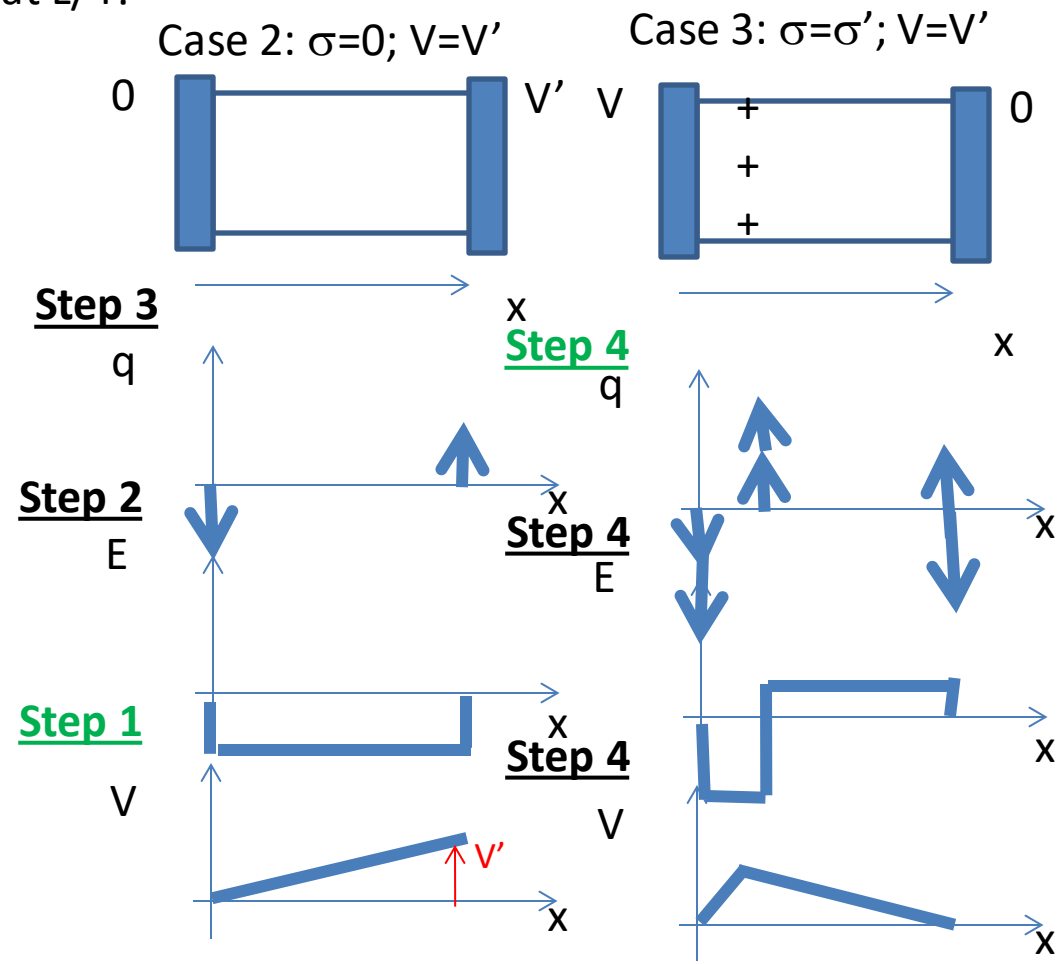




Another example

What is σ is not at center i.e. say at L/4?





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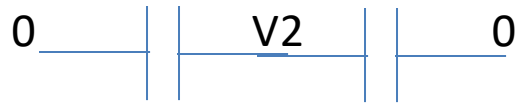
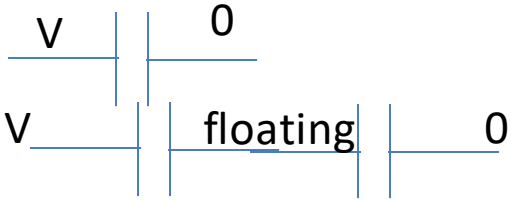
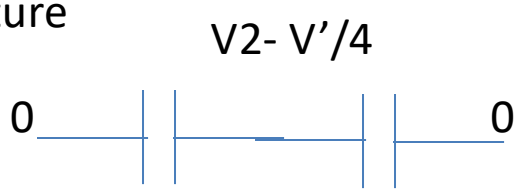


Capacitor solution works easily but Poisson shows that V=V'≠0;

Step 1: Extract C from structure

Step 2: relate V, Q i.e Q=CV

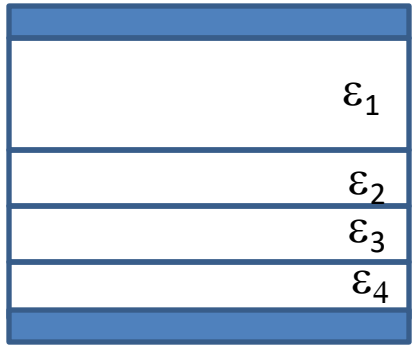




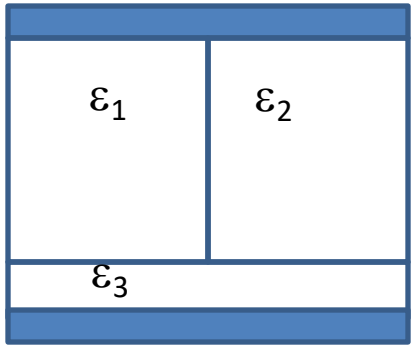
Assume flux is equal in +x an d-x: WRONG

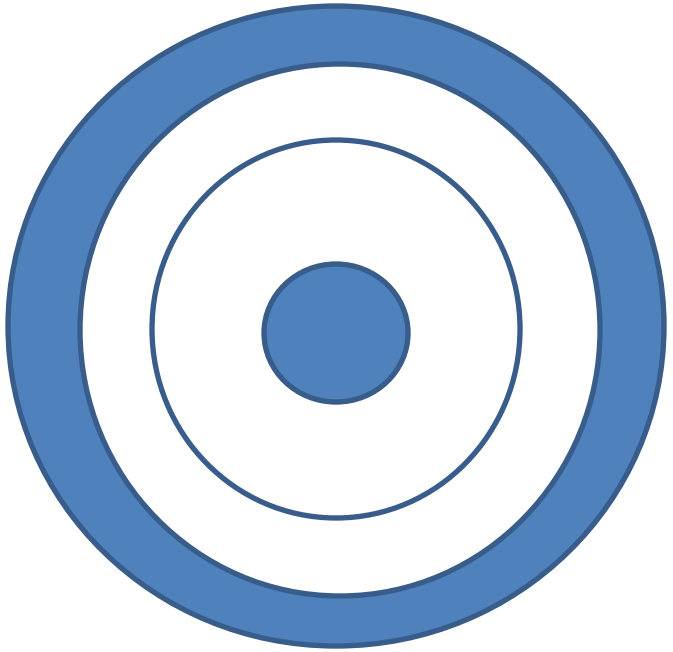
Circuit approach: Ease & limits

Case 1

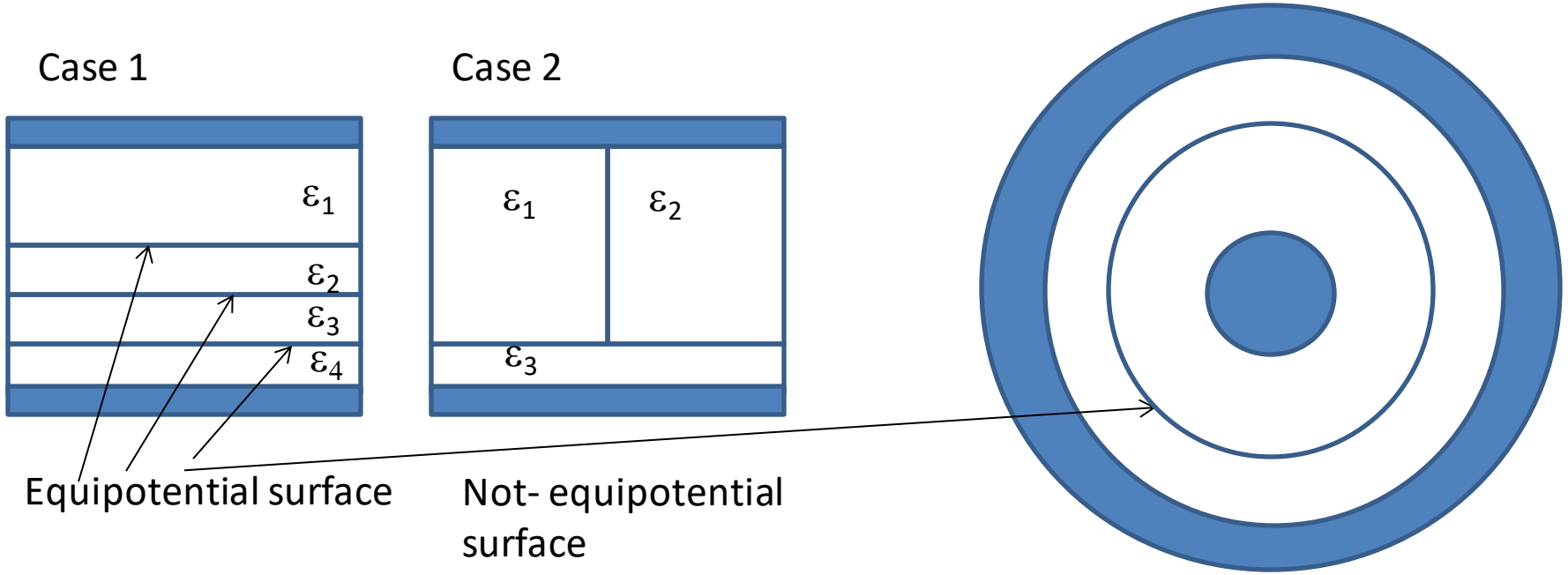


Case 2





Circuit approach: Ease & limits



Case 1: 4 dielectric stack can be simplified by describing as 4 capacitors in series.
Why is it possible?
Adding" floating" parallel metal plates at interface does change the situation.
Essentially as long as we can find an equipotential surface, we can add a metal plate there; This can be true for any structure and dependent on symmetry

Case 2: this cannot be reduced to capacitors circuit easily.

Can you make parallel circuits in case 1? Why do parallel elements work in case 1 but not in case 2?

Points to remember

- There are different ways to model of the same problem
  - Circuit model vs. detailed physics (PDE) based model
- Each model has various representations
  - Physical picture (e.g. force on strain gauges placed to measure E-field)
  - Mathematical formulations
  - Graph
- It is important to be able to work with as many methods and critically understand each others limitations and strengths