EE 724: Electrostatics L5

Udayan Ganguly

Jan 21, 2019

IIT Bombay

Based on Griffiths “Electrodynamics” Ch 3.3

Status/Next steps

- Laplace can be solved
- How is it applied to FinFET analysis?
- Is it valid? Or under what conditions will it not be valid? E.g. ON or Off state?
- What would be the methodology to verify?

FinFET performance

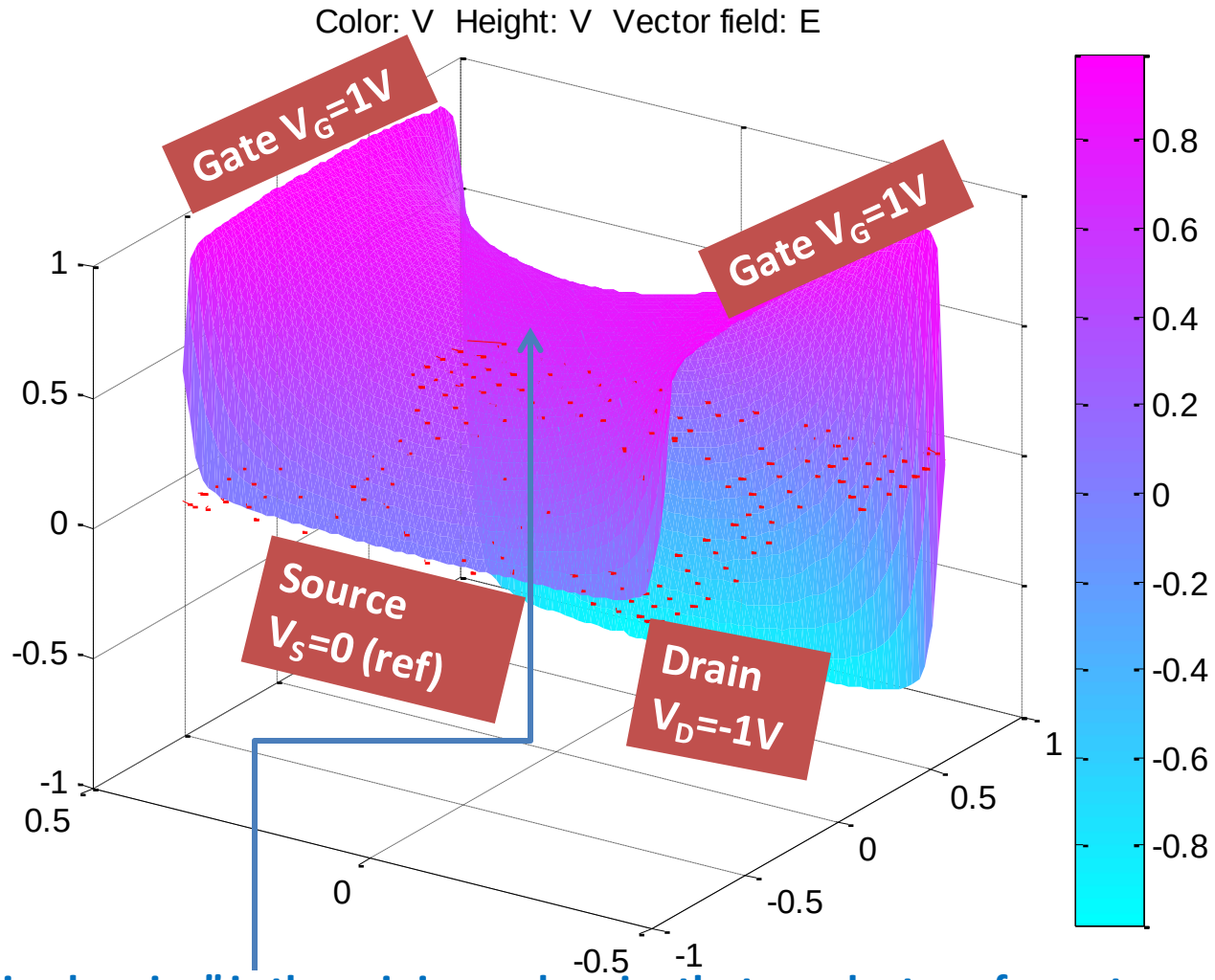
- Specification
- Current: We assume this depends upon the leakiest path I.e. minimum barrier that an electron faces from Source to Drain
  - On-current : Laplace is not valid. Why?
  - Off-current: Laplace is valid. Why?
  - What extent is acceptable? Maybe <10% correction to "leakiness" or conductivity i.e. $n(x, y)$ in the leaky path.

- Subthreshold slope = $\frac{dV_{barrier}}{dV_{gs}}$ @ Vds=0.01V and & Vgs is such that channel is off **<70mV/decade**
- Drain-induced barrier lowering = $\frac{dV_{barrier}}{dV_{ds}}$ @ Vds=0.8V & Vgs is such that channel is off **<20mV/V**

Solve for Electrostatics

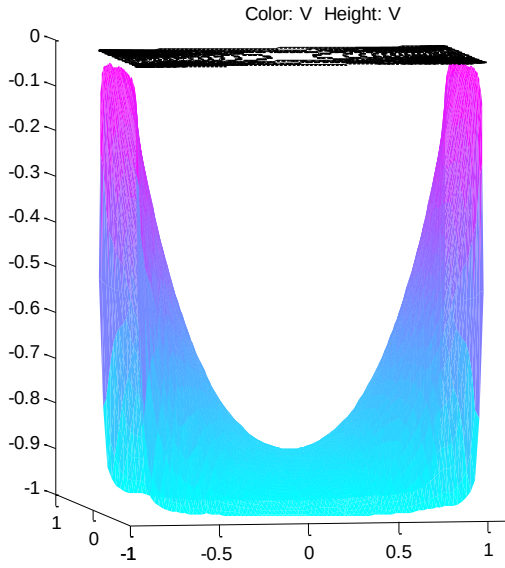
- Where is $V_{barrier}$ in terms of x,y coordinates?
- Are they in the same place for SS and DIBL?

Potential vs. position



"effective barrier" is the minimum barrier that an electron faces to cross over from Source to Drain

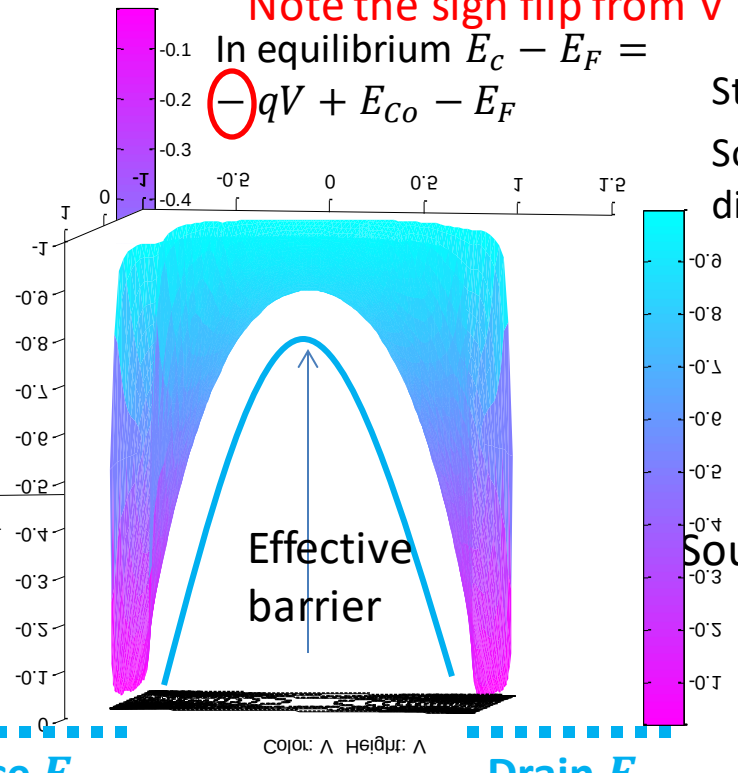
Converting V(x,y) to charge



Step 1; Potential V(x,y)

Note the sign flip from V → E

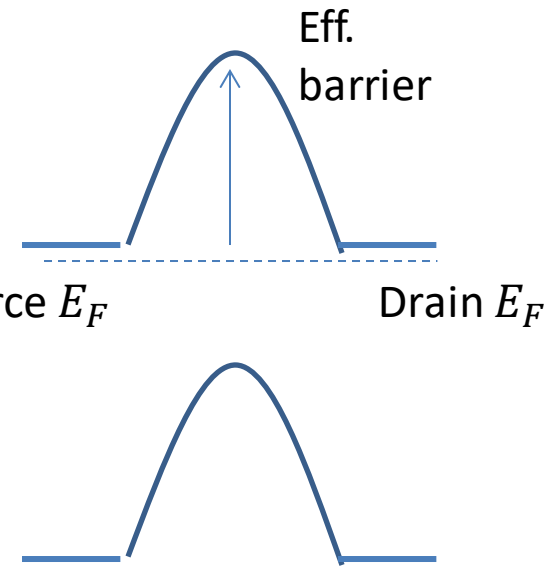
In equilibrium $E_c - E_F = -qV + E_{Co} - E_F$



Step 2: E_c(x,y) in eV by flipping the V sign

Step 3: Find $n(x,y) = N_c \exp(-\frac{E_c - E_F}{kT})$

So from potential we can create a band diagram; Note the error



- **How much does "local" potential need to change to change carrier concentration in "effective" barrier by 10x?**
- **Approx. 60mV at 300K. (show this).**
- **Controlling the conductivity of the MOSFET simplifies to controlling the conductivity of the most leaky path as an approximation. (argue that this is true or false based on a resistor network)**

How to calculate SS and DIBL

We only consider the modulation of effective barrier as a simplification

- For SS
- $V(x,y) = \sum_{n=0}^{inf} C_n cos(k_n y)\cosh(k_n x)$
- By symmetry at center (y=0 and x=0) should be $V_{barrier}$ (you may test this using PDEtool)
- How to get SS in mV/decade?

- For DIBL, potential applied at source and drain needs to be solved
- $V(x,y) = \sum_{n=0}^{inf} C_n cos(k_n y)\sinh(k_n x)$
- By symmetry at center should be Vbarrier
- How to get DIBL in mV/V?

$$V(x,y) = \sum_{n=0}^{inf} (-1)^n \frac{2Vo}{ak_n} cos(k_n y) \frac{\sinh(k_n x)}{\sinh(k_n b)}$$

TPS

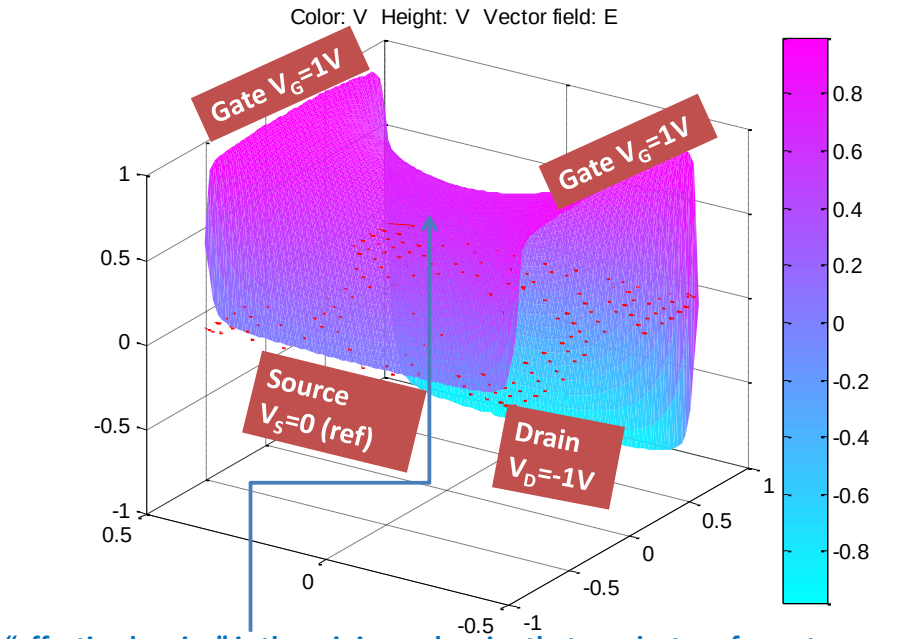
Potential V(x) in a 1D capacitor is linear with x (nature) and depends on x/d (parameter)

Where d = thickness of insulator

Now that you know how to solve for FinFET electrostatics,

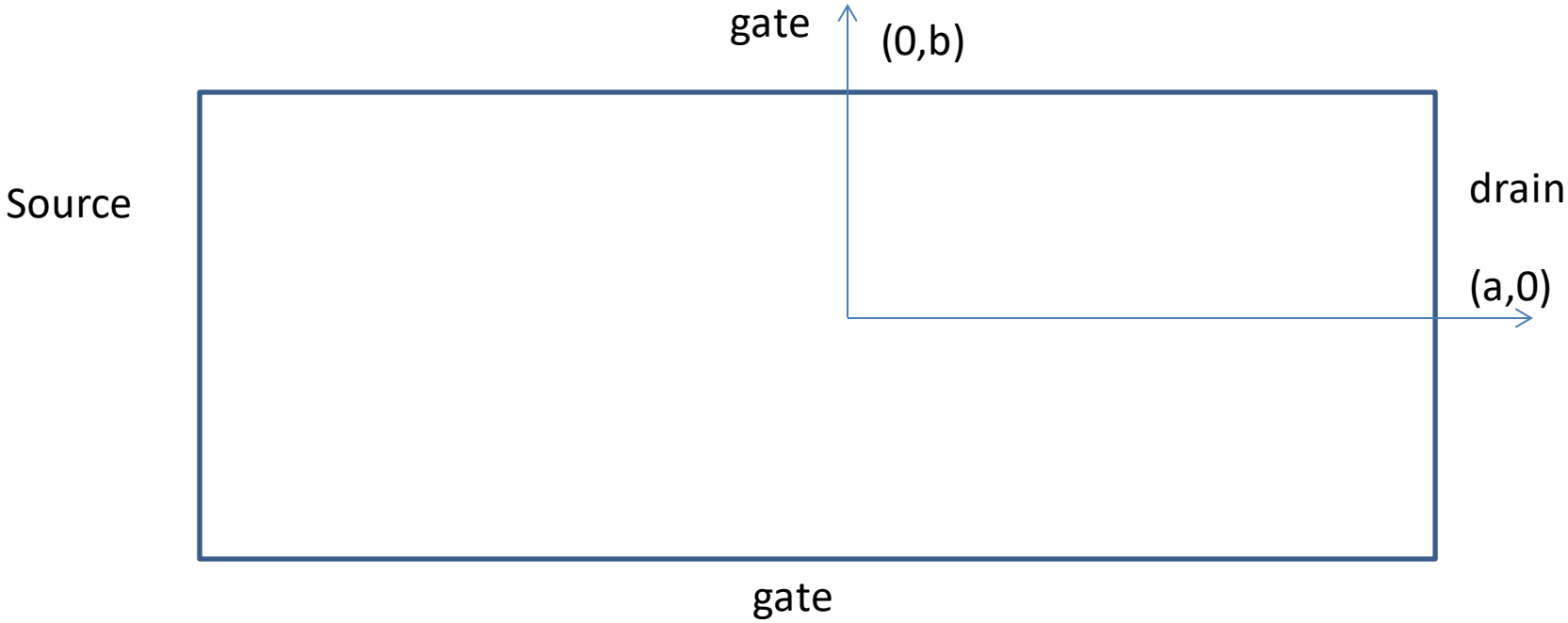
(1) how (nature and parameters) the gate potential change (ΔV_g) affect barrier (ΔV_b)?

(2) how (nature and parameters) the drain potential (ΔV_d) affect barrier (ΔV_b)?



"effective barrier" is the minimum barrier that an electron faces to cross over from Source to Drain

Implications



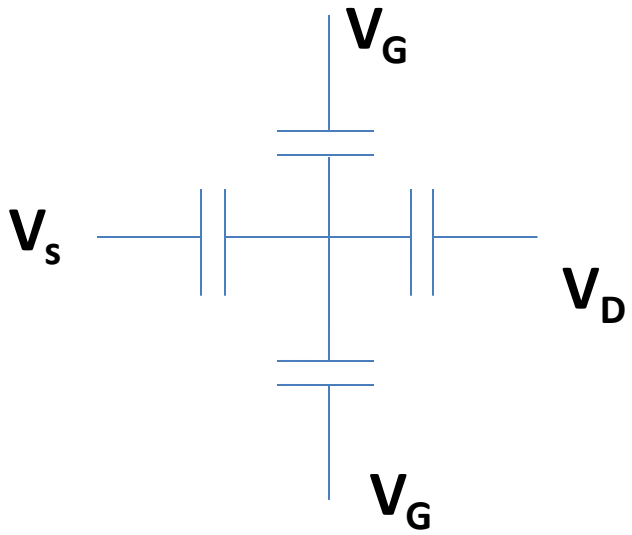
Decay in the y direction depends exponentially upon length-scale a

Decay in the x direction depends exponentially upon length-scale b

Barrier Height vs Applied bias

How (linearly / non – linearly) V(x,y) depends upon (i) VG and (ii) x,y?

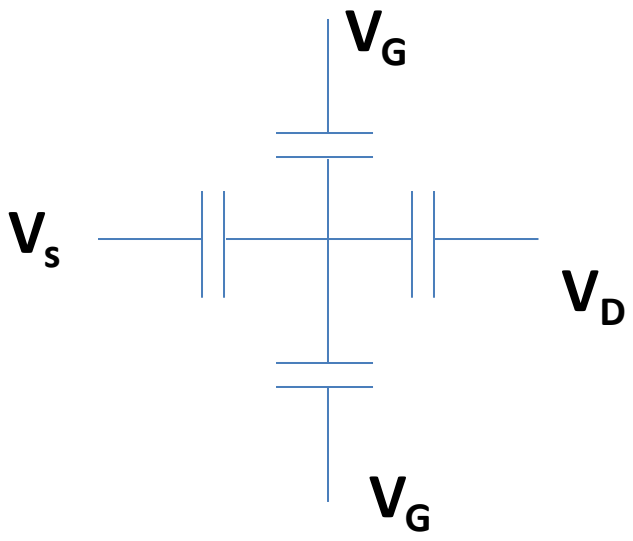
- $V(x,y) = Vo \sum_{n=0}^{inf} (-1)^n \frac{2}{ak_n} cos(k_n y) \frac{\sinh(k_n x)}{\sinh(k_n b)}$
- Knowing position of the barrier (x,y) we plug in
- There dependence is
  - Linear with Vo ➔ guarantees superposition
  - Complex (sinh, cos) dependence on geometry (Ko, b,a,x,y)
- $V_b = V(x,y) = VoA$
  - Where $A(k_n, a, b, x, y)$ depends only of geometry if x,y is known (position of barrier).
  - Position of barrier is bias dependent but given x,y is known the ratio $A = V_b/Vo$ is known for the at the x,y
  - we can find capacitances $A = \frac{C_D}{\sum C_i}$
- The circuit model can work for any capacitor form 1D, 2D etc but the exact value of the capacitor must be derived for different cases… we just saw how 2D Laplace based capacitor was derived.



How to add a circuit model?

Can we express the V(x,y) using a capacitive divider from each potential plate / note?

Why is it valid? Does the 1D capacitor model work? What are the capacitors?



1. Express $\frac{V(x,y)}{V_D} = K_1$ which is a geometric constant.
2. What is equivalent of K_1 in terms of capacitors?

From capacitive network $\mathrm{Q_D} = \left(\mathrm{V_D} - V(x,y)\right) C_D$

3. We can create such equations for each terminal and we know that $\sum Q_i = 0$ i.e. sum of charge due to all terminals at V (why? Because the terminal is floating in circuit AND Laplace is valid.)
4. For a case where $V_D = V$ and $V_S = V_G = 0$

$$V(x,y) = \frac{C_D V_D}{\sum C_i}$$

5. For 4 terminal we get 4 such equation for 4 unknown capacitors C_i. This can be solved.

Exercise: Please solve this

Points to remember

- Fundamental length-scale of **screening is geometric or structural** in the case of dielectrics;
  - Shape is everything
  - **Scaling (FinFETs) valid as long as shape is conserved**
- We will see that length-scales of **screening becomes more materials dependent** in semiconductors due to dopant ions (depletion) and free charges