

EE724 Tutorial

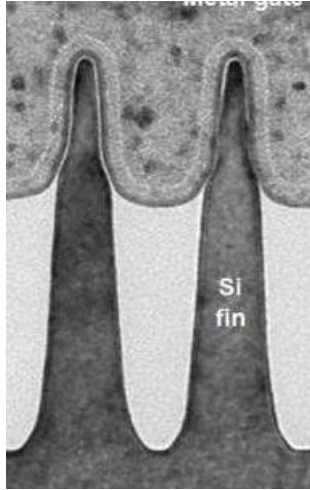
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Electrical Engineering (EE7), IIT Bombay

Group details

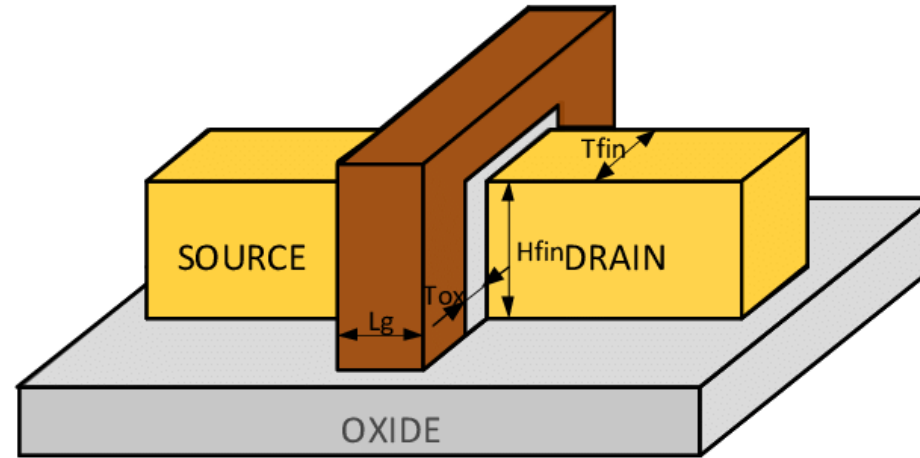
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10	Debankita	23d0527	Kavin Dave	23d0528	Rahul Awale	22d2018	EE724_10

- Introduction FinFET
- TCAD?
 - Why and how to use
 - 3D and 2D FinFET analysis
- FinFET designing for performance improvement
- Takeaways

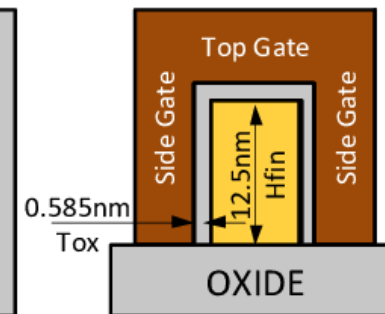
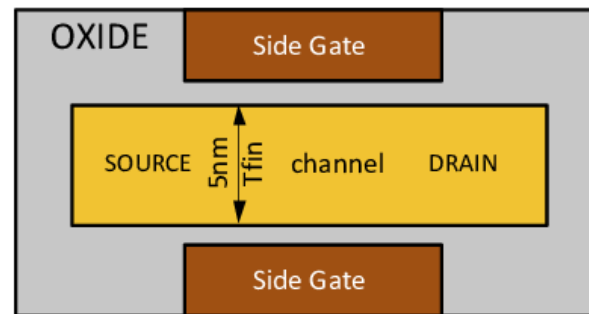
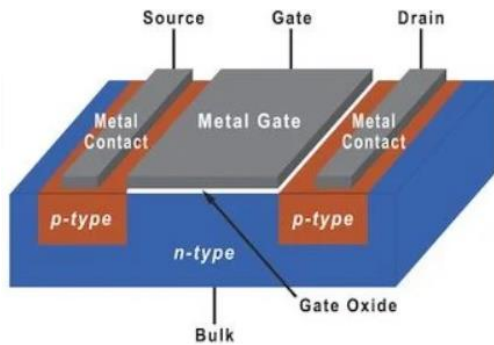
FinFET TEM



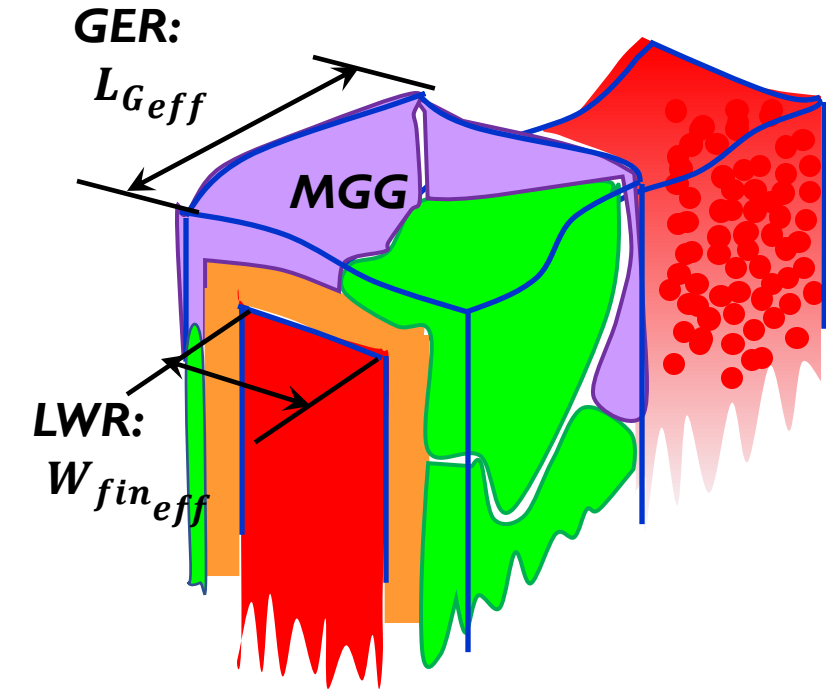
FinFET schematic and cross-section



10nm
 L_g



FinFET with variability



How do you simulate?

LER: Line Edge Roughness
LWR: Line Width Roughness
GER: Gate Edge Roughness
MGG: Metal Gate Granularity

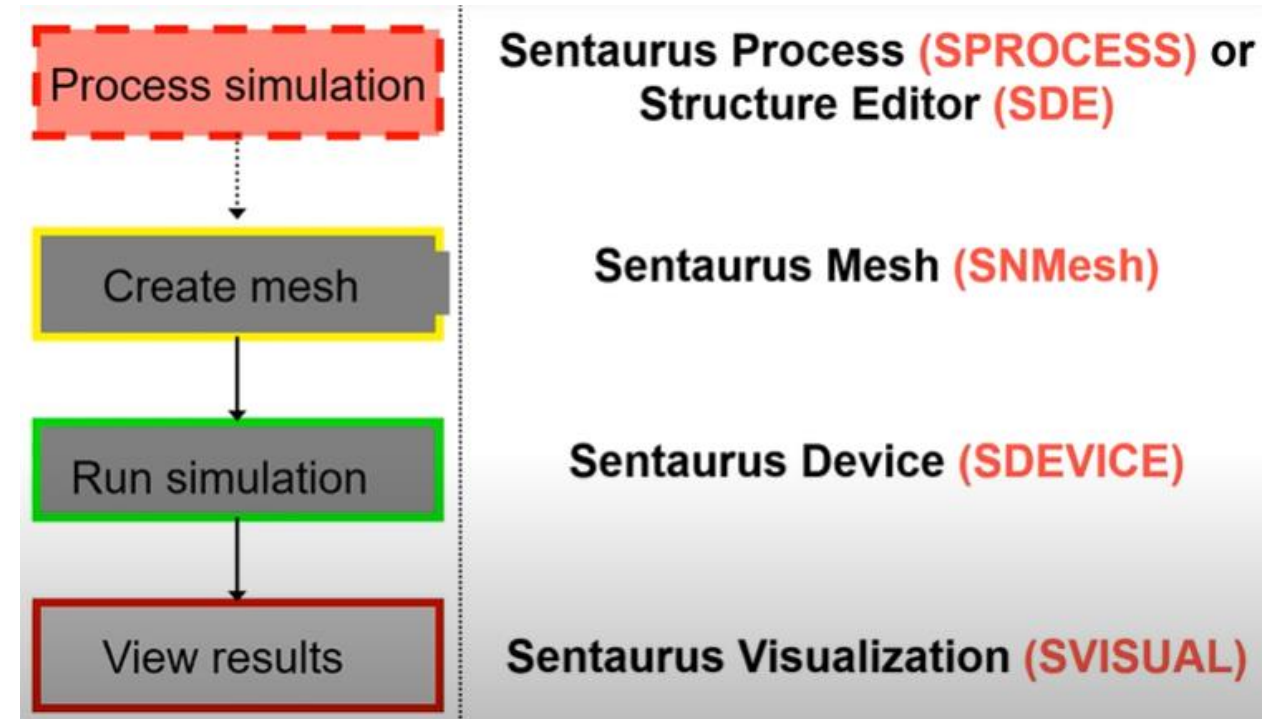
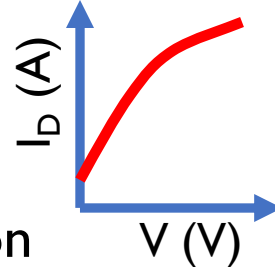
Planar MOSFET

Simulate real-world device → TCAD

TCAD: Why, What, How

- TCAD: Enables R&D for upcoming technology
- Solves fundamental, physical, and partial differential equations (Drift-Diffusion, Poisson, etc.) for discretized geometries

- Define equation: Physics to solve
 - Boundary condition: Electrode potential
 - Solve equation at each mesh point
- Files
 - .tdr – Structural information
 - .plt – Device characteristic information



How to start TCAD

- Download and install MobaXterm
- Start new session
 - Write command: `ssh -XY username@10.107.106.22`
 - Press enter
 - Usernames: Find in the sheet
 - Password: Same as username

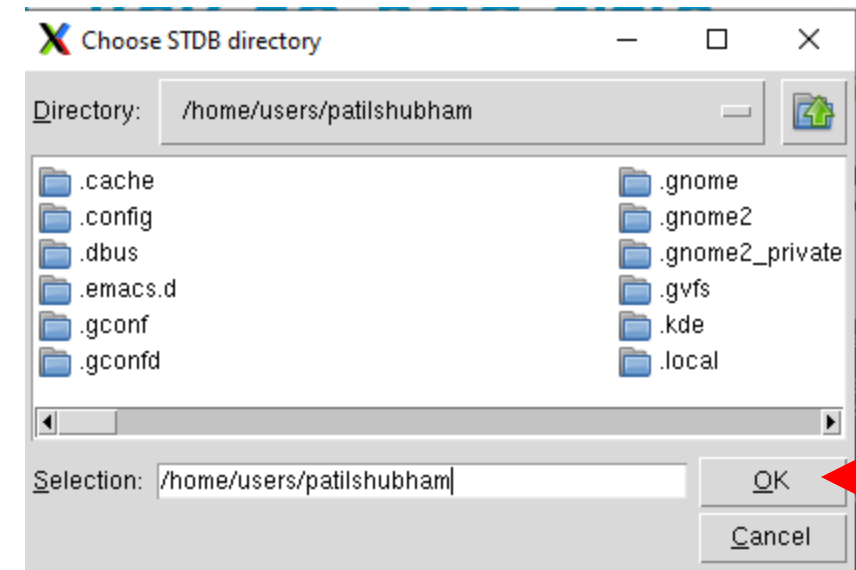
```
23/01/2024 12:33.30 /home/mobaxterm ssh -XY patilshubham@10.107.106.22
Last login: Tue Jan 23 10:24:36 2024 from 10.107.102.112
-bash: /usr/local/softwares/synopsys/SentaurusL2016/sentaurus/L_2016.03/bin:/usr/synopsys/T
rus_vL_2016.03/bin:/usr/local/Softwares/Qtplot/qtplot-0.9.8.7:/usr/local/Softwares/ICCAP
cal/Softwares/Sentaurus/Sentaurus_vG_2012.06/bin:/usr/lib64/qt-3.3/bin:/usr/local/bin:/bin:
[patilshubham@mcl22 ~]$
```

- Write: **swb** & Press enter
- Set working directory

```
23/01/2024 15:11:42 /home/mobaxterm ssh -XY patilshubham@10.107.106.18
Last login: Tue Jan 23 10:39:33 2024 from 10.107.102.112
-bash: /usr/local/softwares/synopsys/SentaurusL2016/sentaurus/L_2016.03/bin:/usr/synopsys/TCAD2018/sentaurus/0
rus_vL_2016.03/bin:/usr/lib64/qt-3.3/bin:/usr/local/bin:/usr/bin:/usr/local/sbin:/usr/sbin: No such file or d
[patilshubham@mcl18 ~]$ swb &
[1] 9335
[patilshubham@mcl18 ~]$
*****
***          Sentaurus Workbench          ***
***          Version T-2022.03            ***
***          (0.7486838, x86_64, Linux)    ***
***          Copyright (c) 1994-2022 Synopsys, Inc. ***
***
*** This software and the associated documentation are confidential ***
*** and proprietary to Synopsys, Inc. Your use or disclosure of this ***
*** software is subject to the terms and conditions of a written ***
*** license agreement between you, or your company, and Synopsys, Inc. ***
*****

STDB environment variable is not set or points to an invalid directory.
Set STDB to a valid directory, where your projects reside.

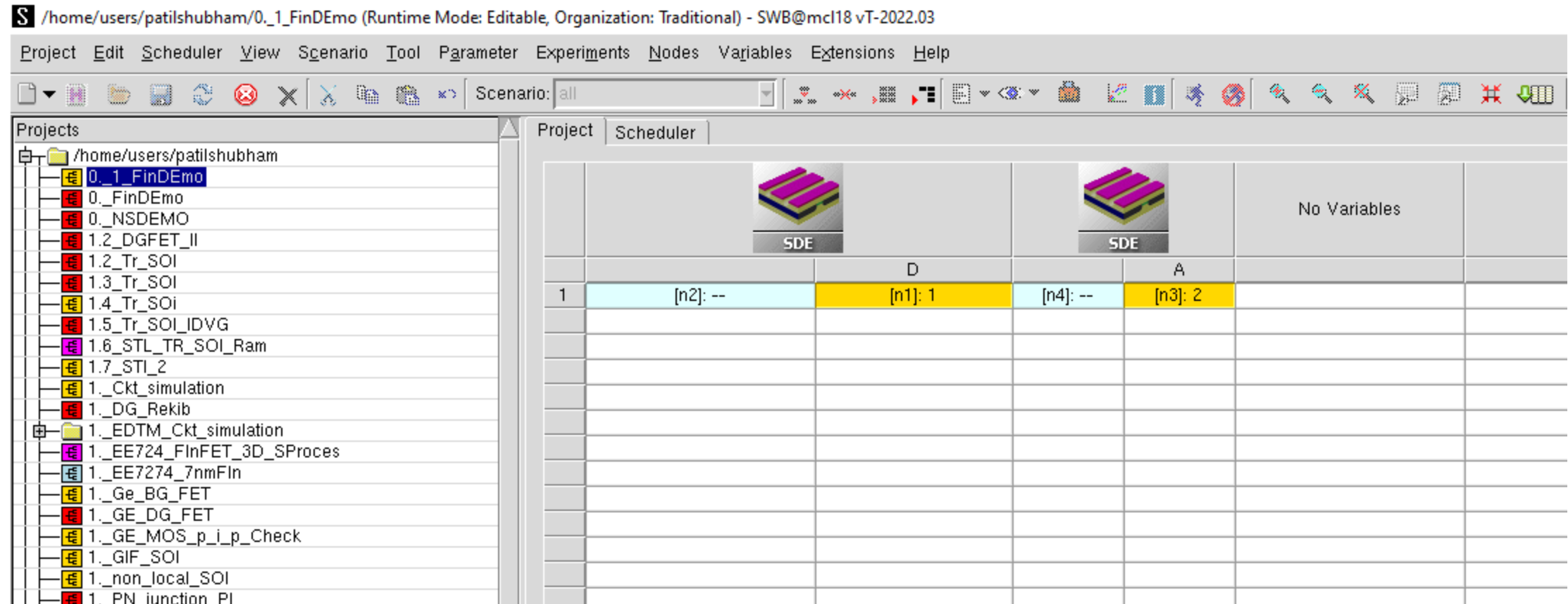
ixterm.mobatek.net
```



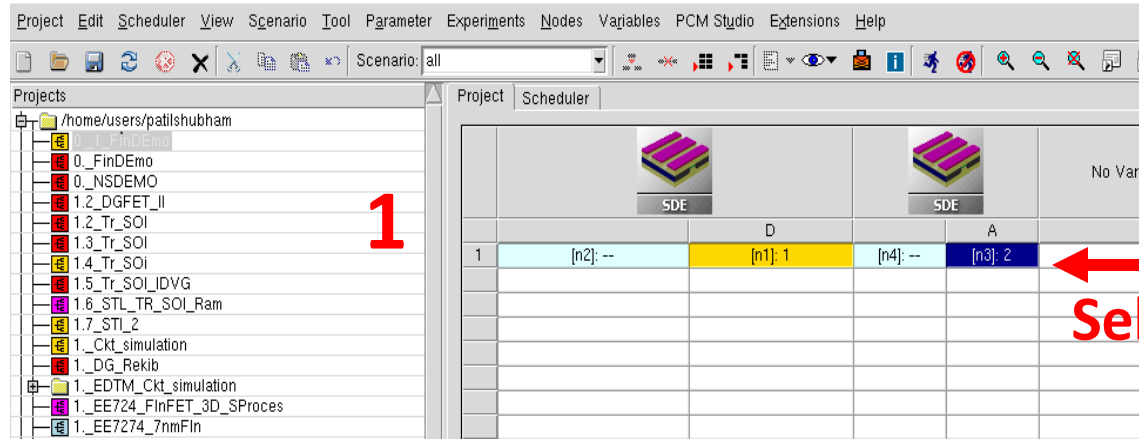
Your projects

TCAD examples

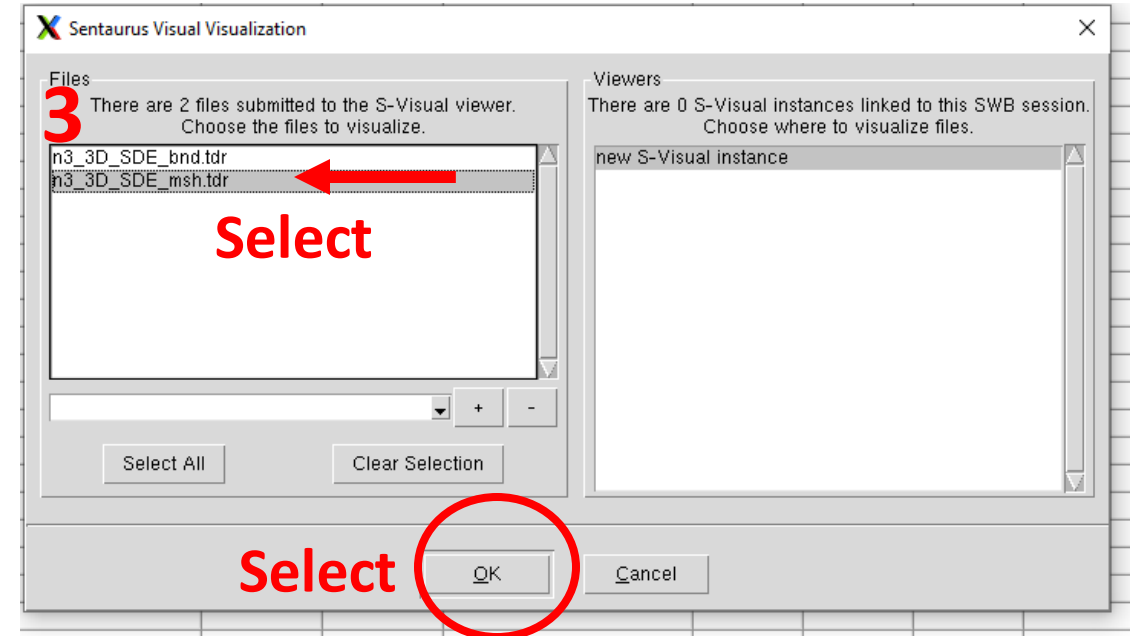
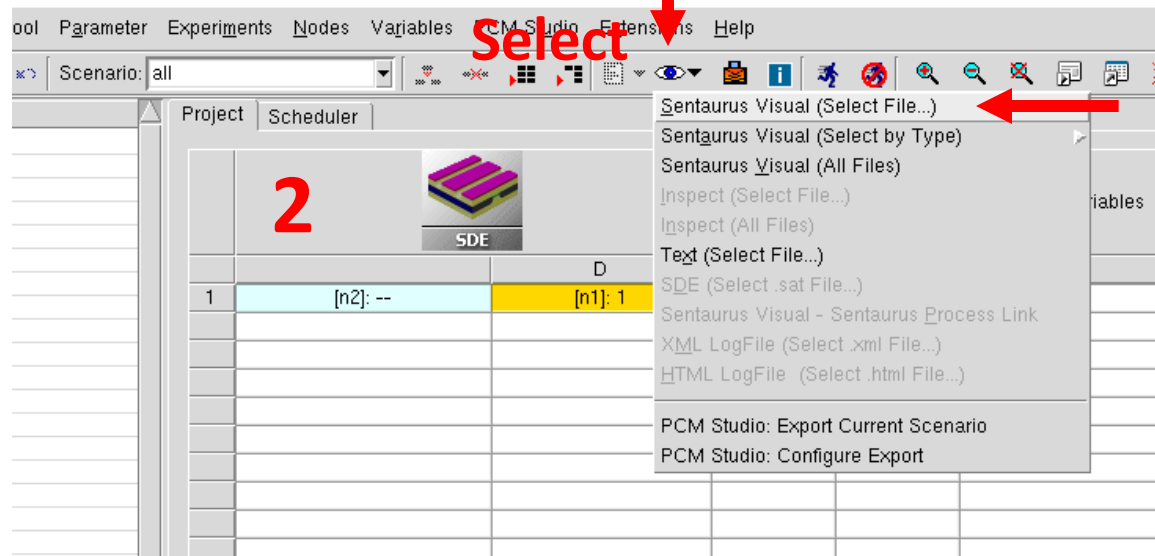
- In home, you will find the **0._I_FinDEmo** project. Double click to open

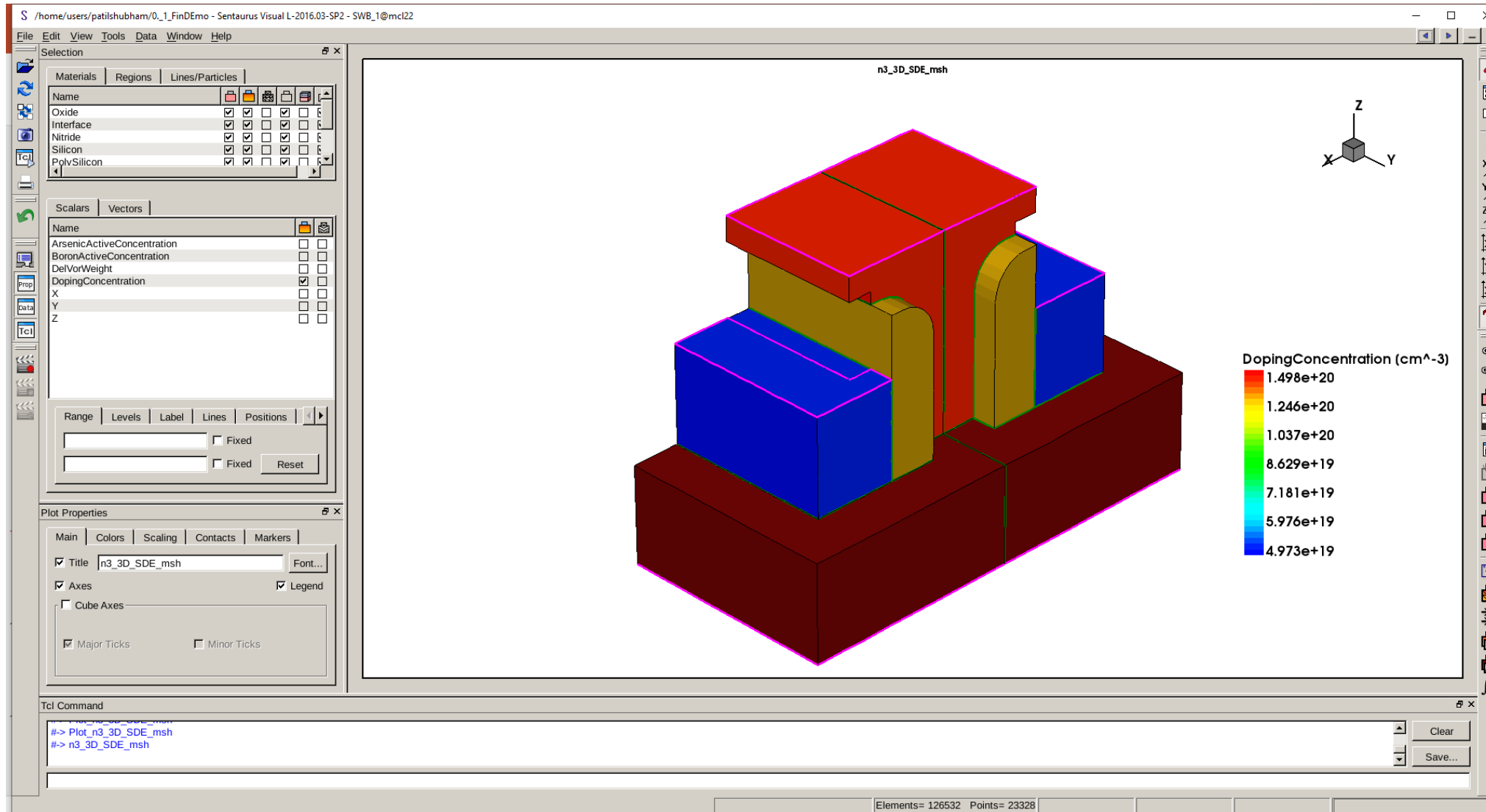


/home/users/patilshubham/0_1_FinDEmo (Runtime Mode : Editable) - SWB@mcl22 vL-2016.03-SP2



time Mode : Editable) - SWB@mcl22 vL-2016.03-SP2





Rotation
for view

Cutline

FinFET: Fabrication steps

Materials Regions Lines/Particles

Name						
Silicon	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
PolySi	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Oxide	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Insulator1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Nitride	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>

Scalars Vectors

Name		
X	<input type="checkbox"/>	<input type="checkbox"/>
Y	<input type="checkbox"/>	<input type="checkbox"/>
Z	<input type="checkbox"/>	<input type="checkbox"/>

Range Levels Label Lines Positions

☐ Fixed

☐ Fixed

Plot Properties

Main Colors Scaling Contacts Markers

☒ Title

☒ Axes ☒ Legend


☐ Cube Axes

☒ Major Ticks ☐ Minor Ticks

Tcl Command

```
set_material_prop PolySi -plot Plot_n1_finfet_procem_bnd -geom n1_finfet_procem_bnd -show_bulk  
#-> 0
```

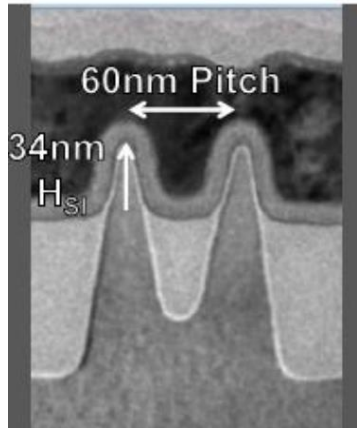
n1_finfet_procem_bnd



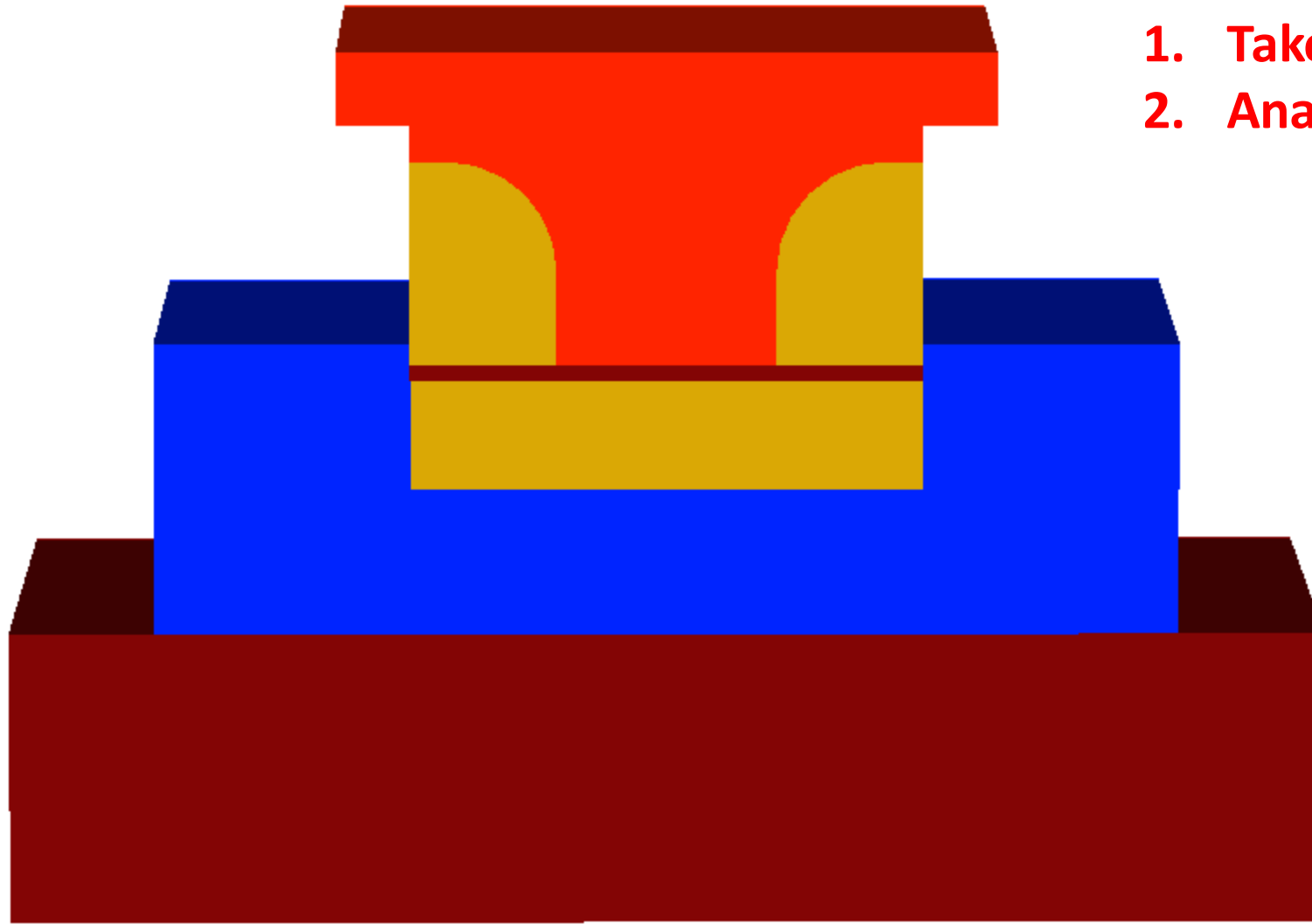
Elements= 824 Points= 195

27°C Smoke

17:52 23-01-2024

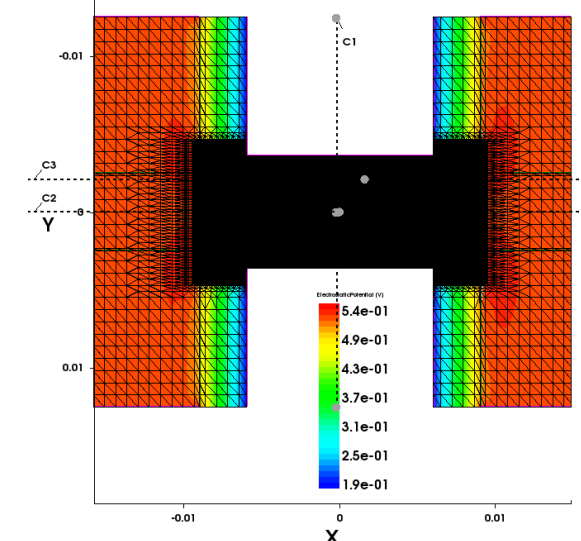
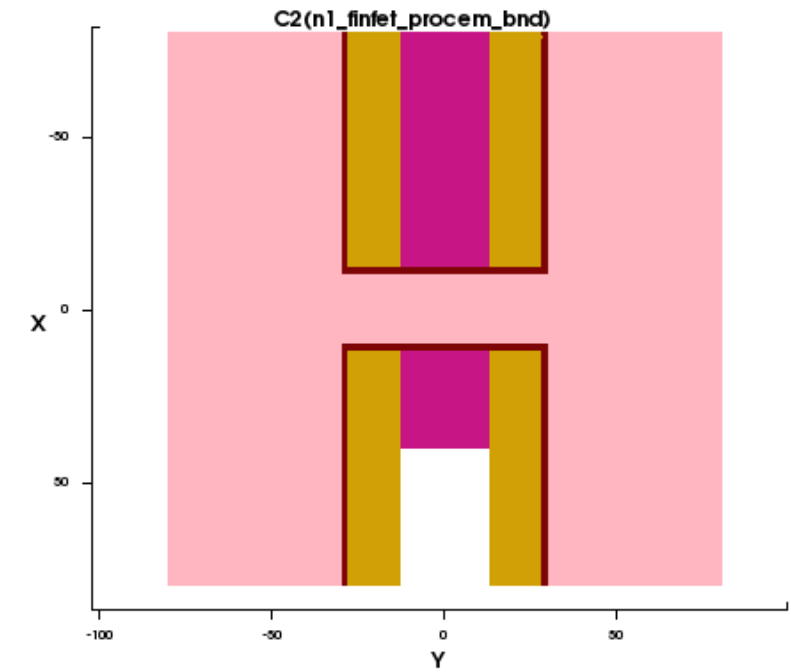
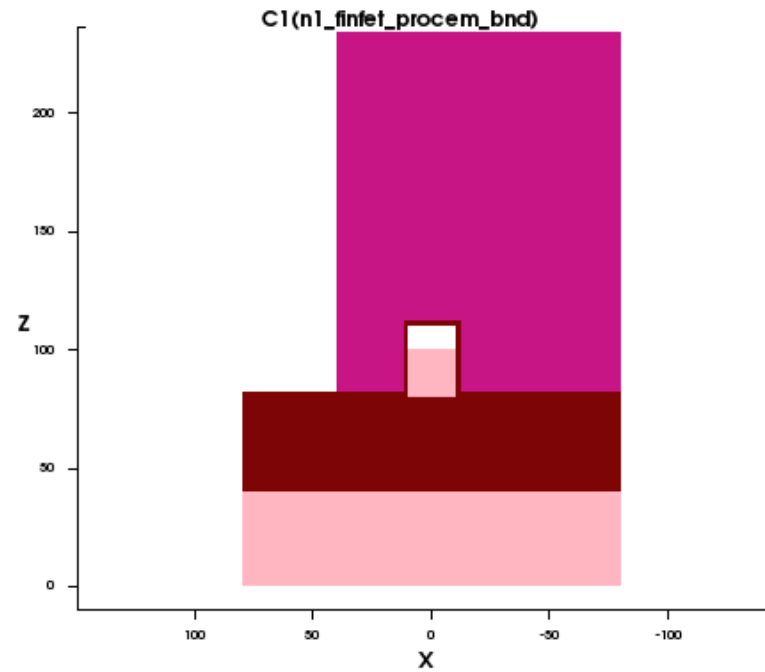
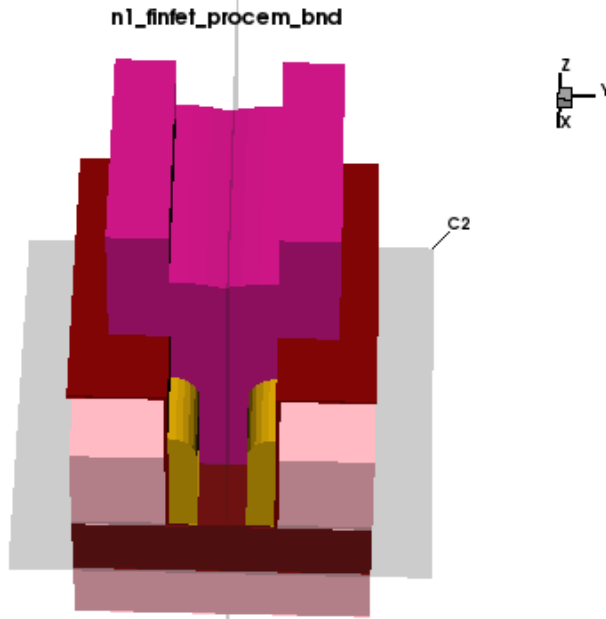


1. Take cutlines
2. Analyse structure

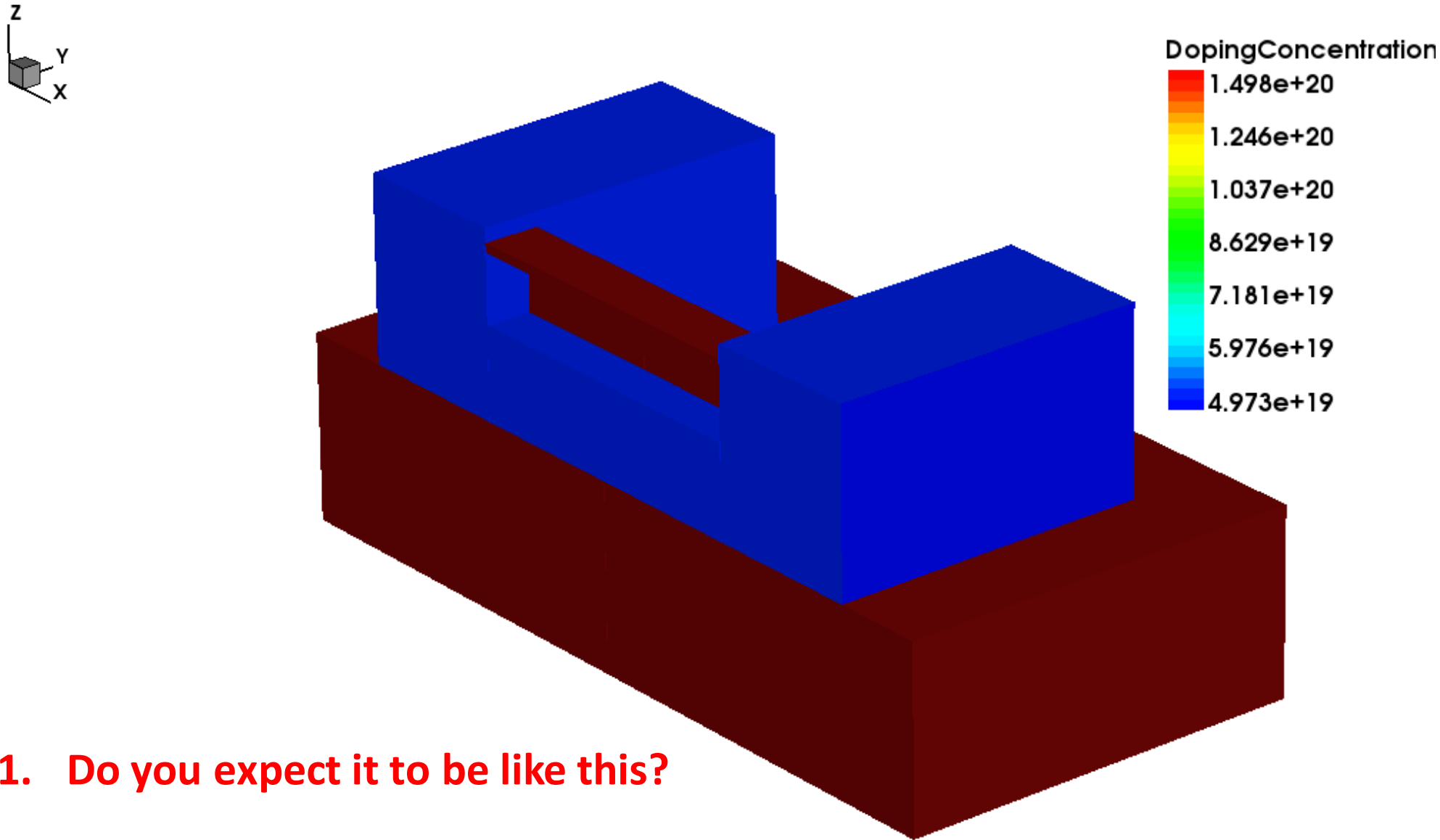


FinFET structure

3D → 2D FinFET

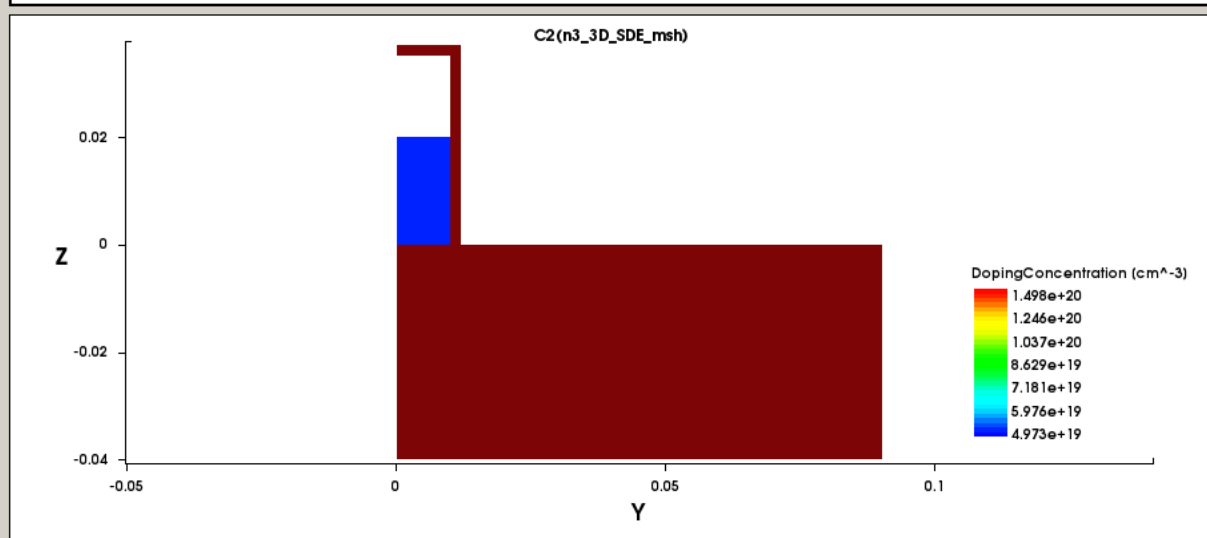
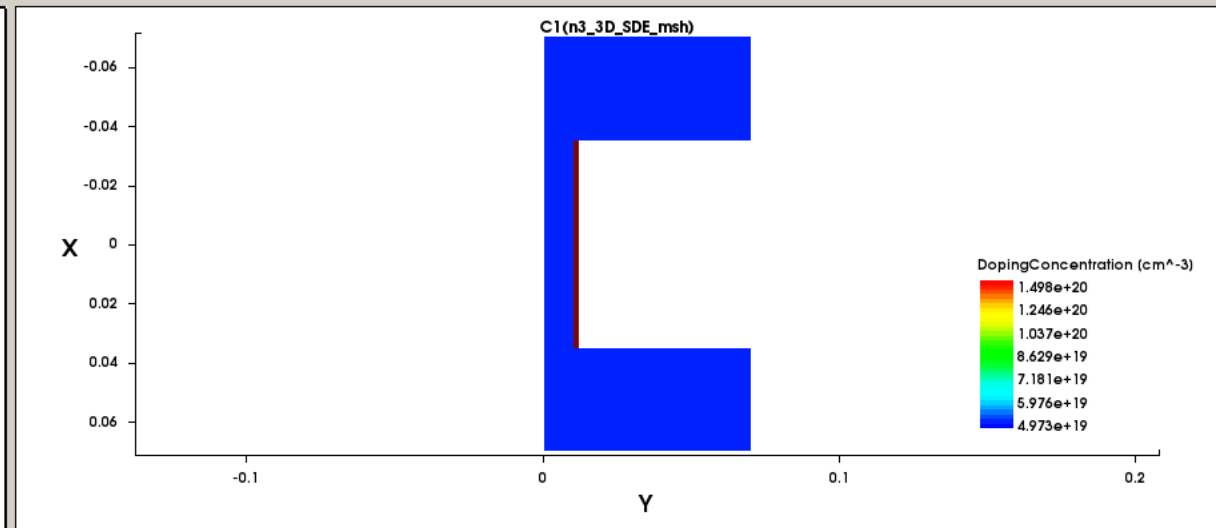
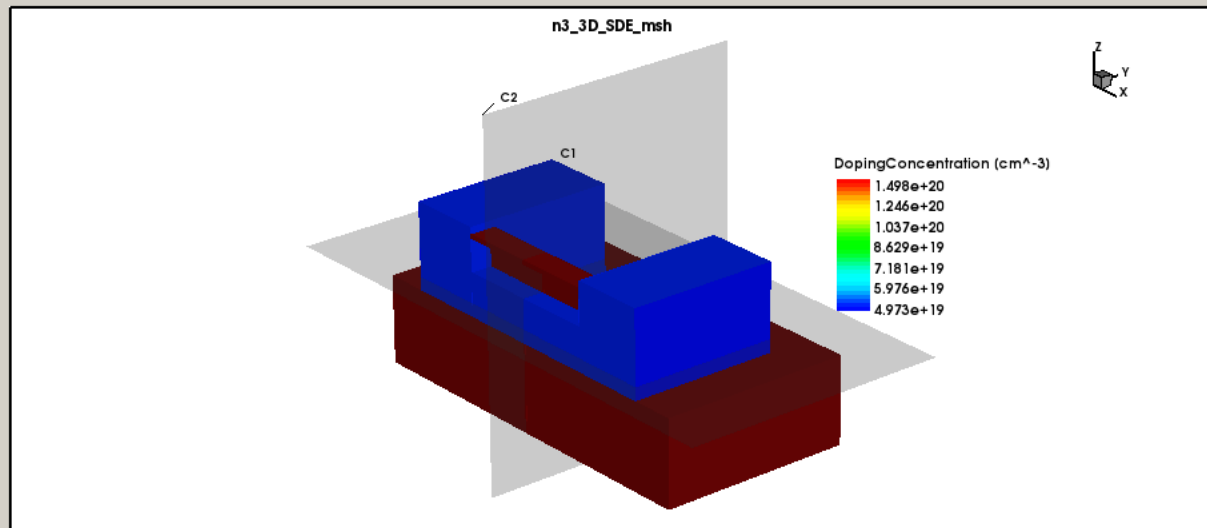


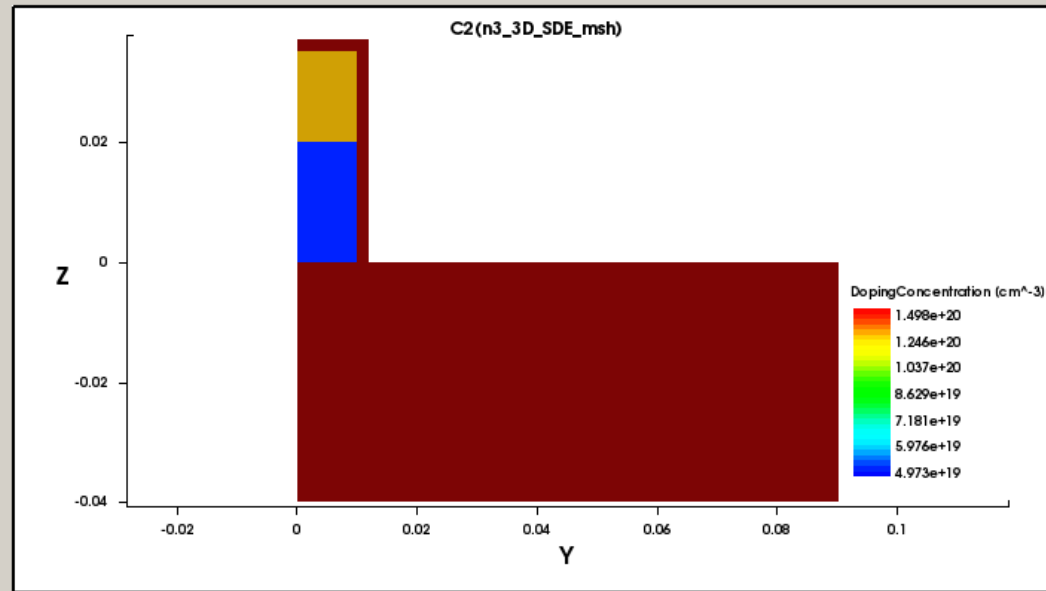
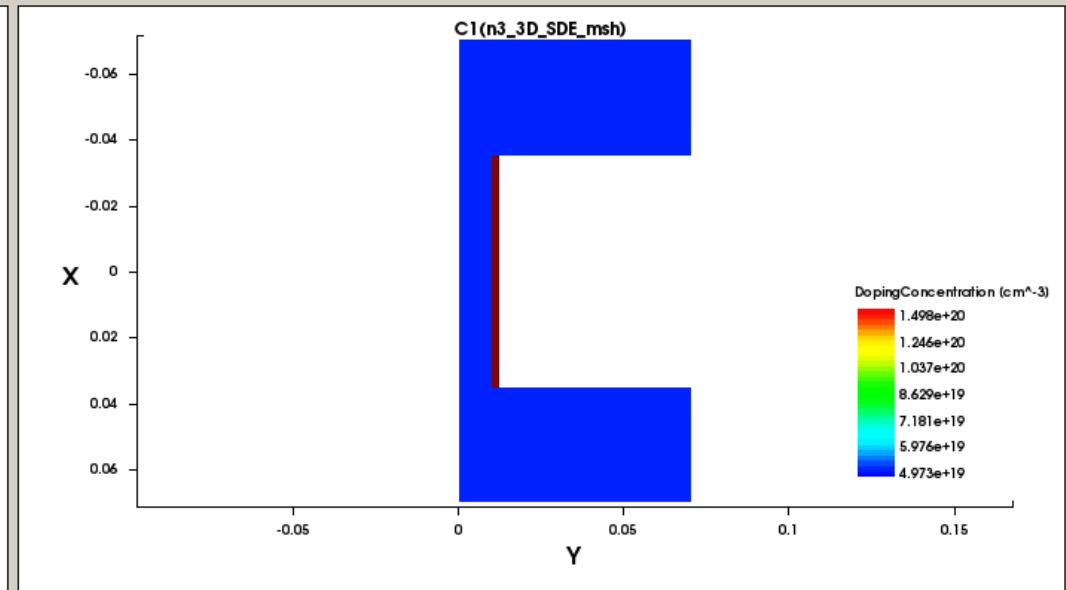
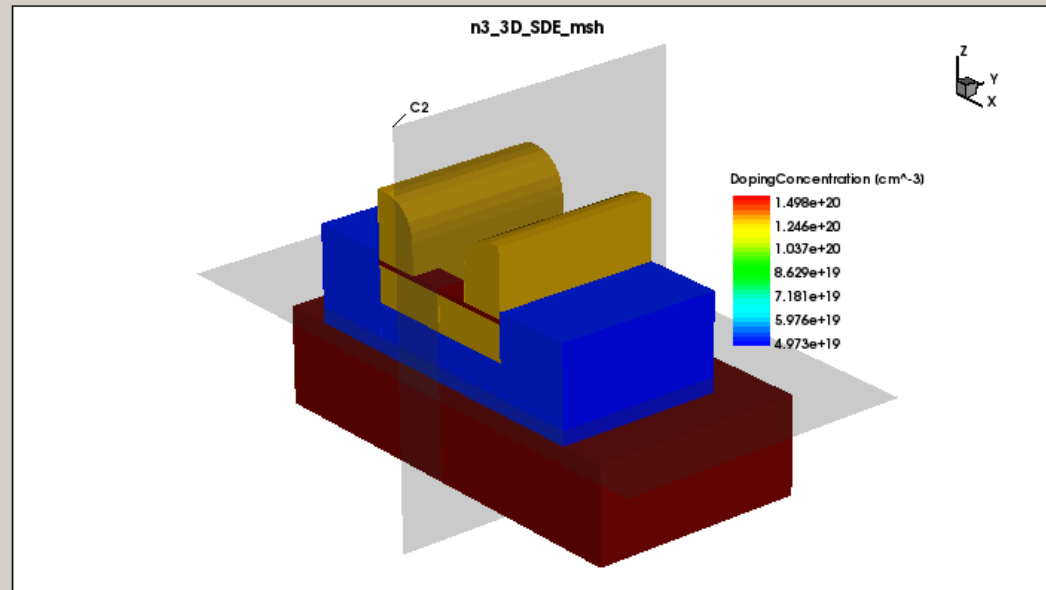
FinFET: Is something weird?



1. Do you expect it to be like this?

FinFET: 2D view



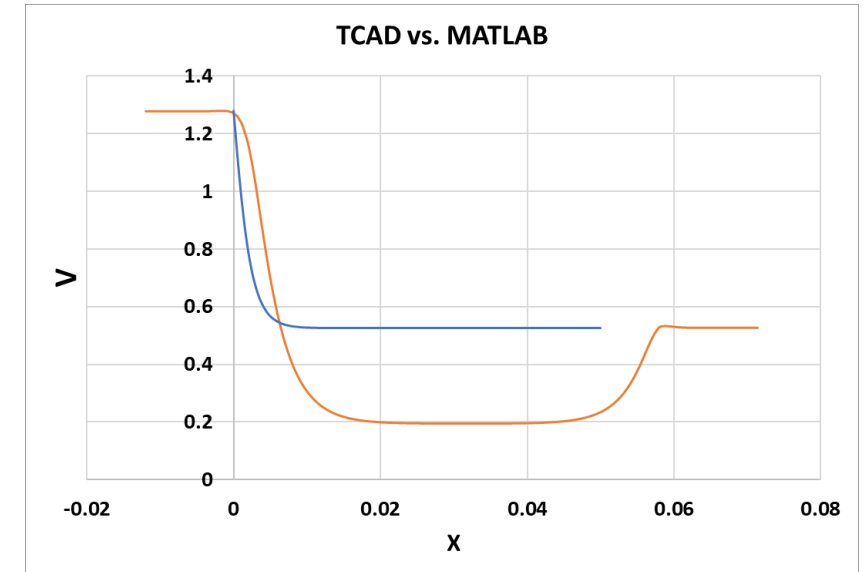
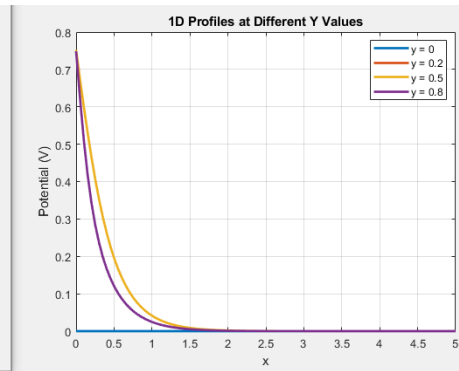
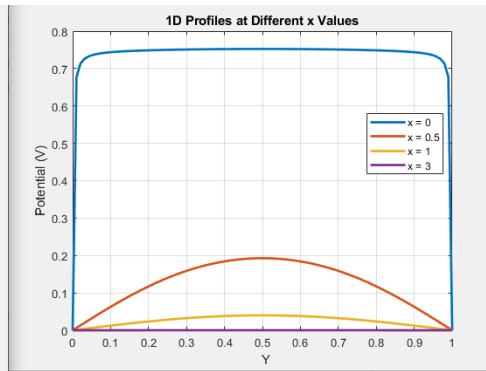
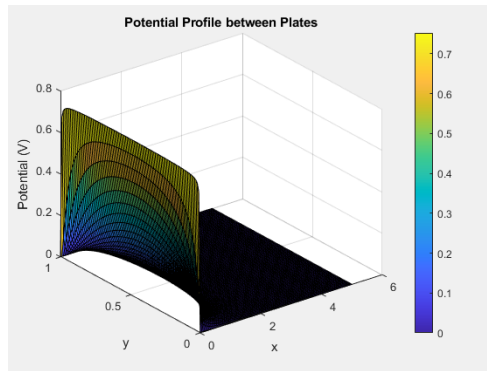
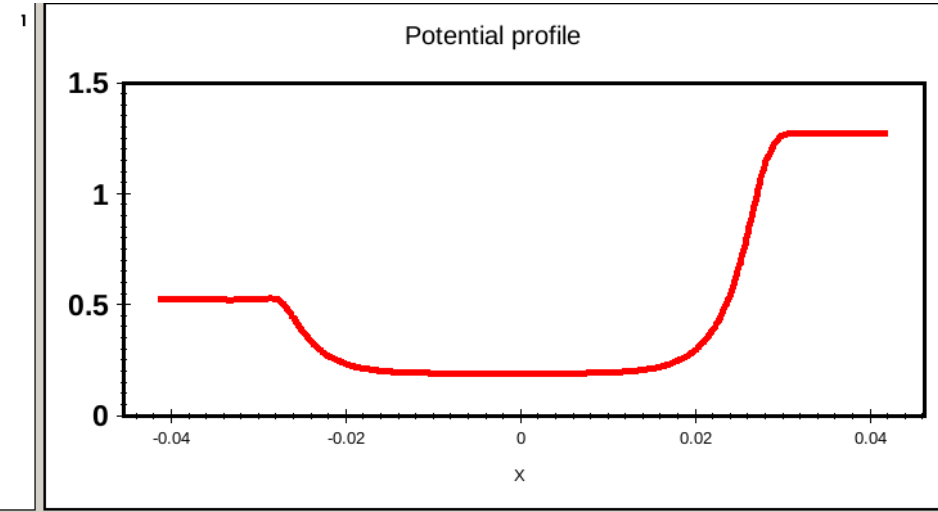
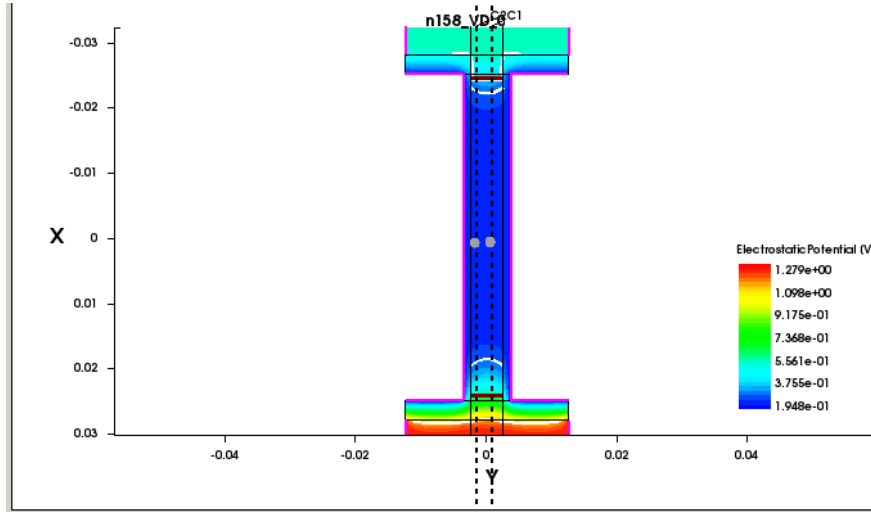


1. Is it something you expected?
2. If yes, why?
3. If no, what changes are needed?

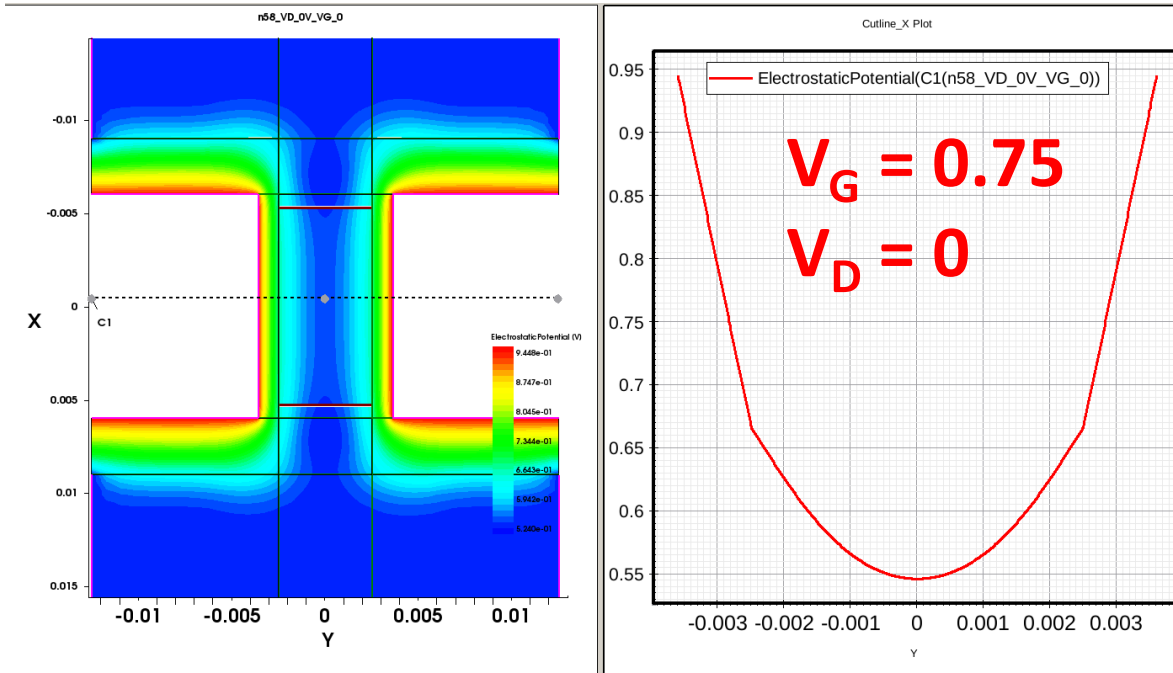
- Think:
 - What are the two types of boundary conditions?
 - In the half-fin model, what are the boundary condition
- Pair:
 - Why are the advantage/disadvantage of the half fin model?
 - Simulation cheaper
 - Spatial design variations can't be captured
 - Design with maybe different doping profiles, and workfunction
 - For a case where S/D is at zero bias, can a smaller simulation space suffice e.g. quarter fin model?
 - No, can't replicate

2D FinFET: Potential profile comparison vs. MATLAB

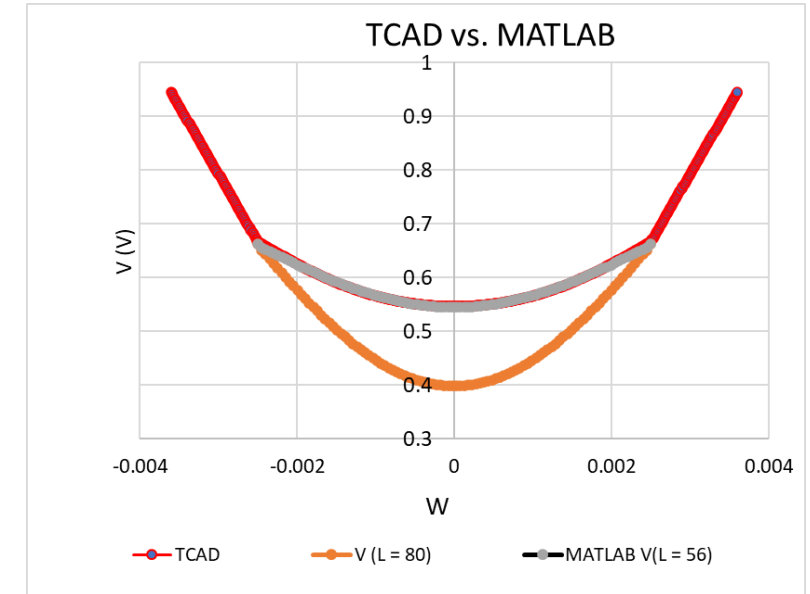
$$V_G = 0$$
$$V_D = 0.75$$



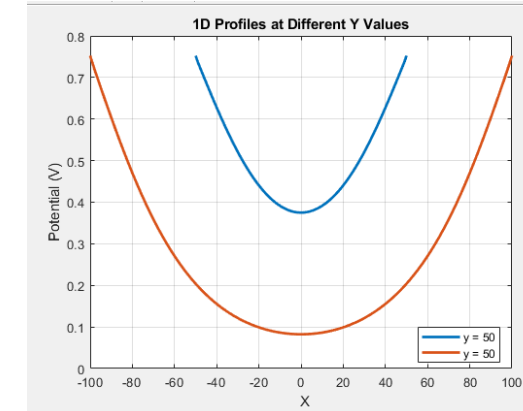
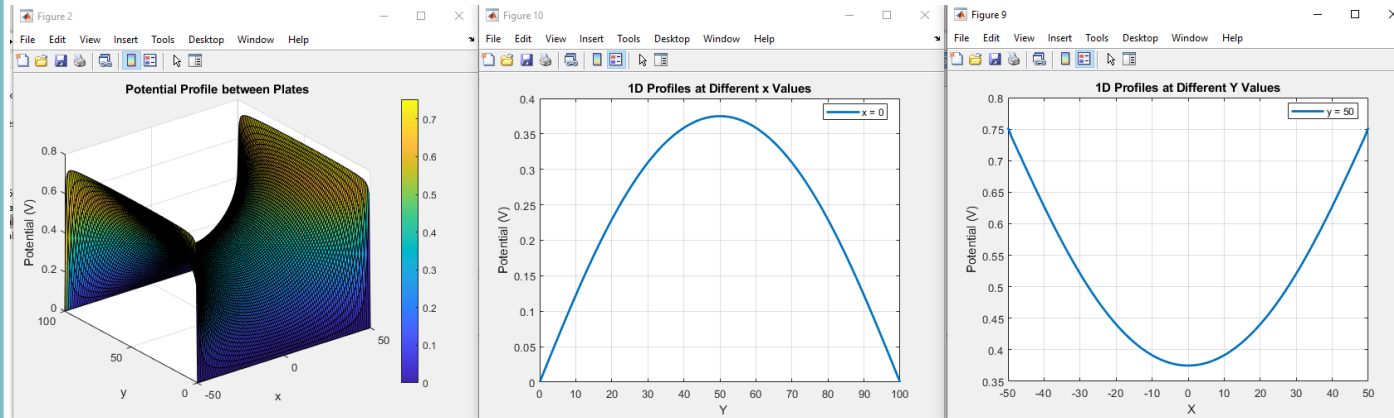
2D FinFET: Potential profile comparison vs. MATLAB



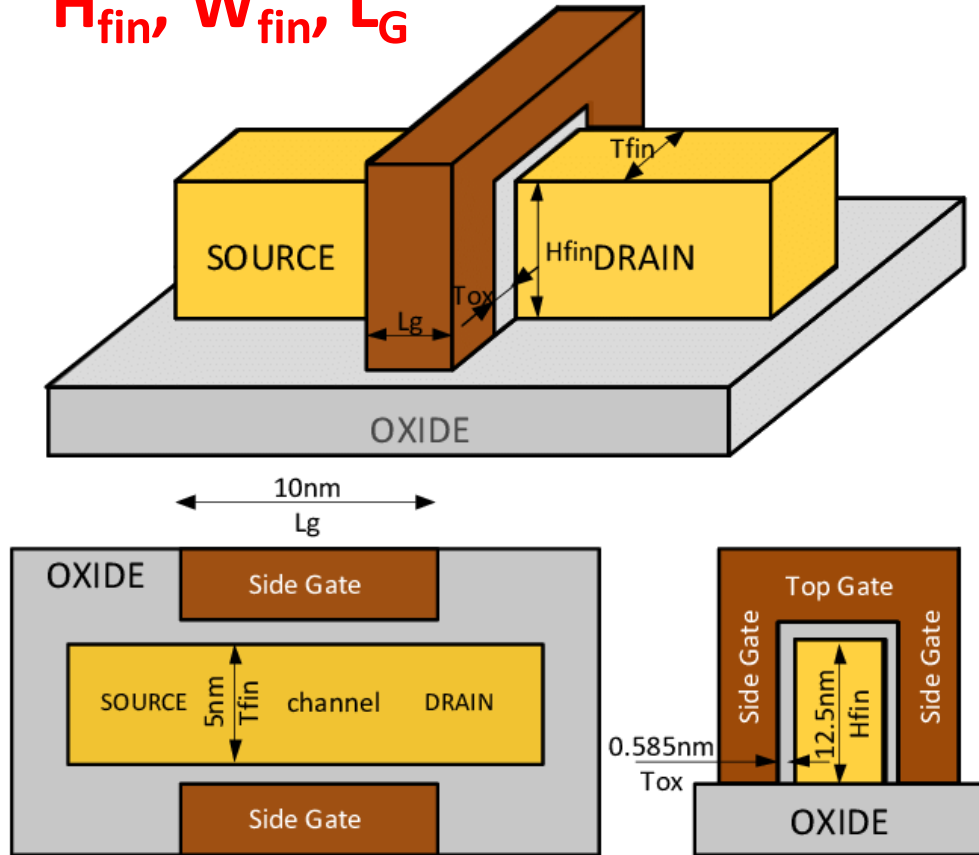
Decay $\rightarrow f(X)$



With proper scaling the dimension we can achieve this



H_{fin} , W_{fin} , L_G



$$I_D = \mu * C_{ox} * \frac{W}{L} * (V_{GS} - V_T)$$
$$V_T = f(N_{channel})$$

- Now you understand the FinFET
- Suppose you are a device engineer, how will you improve the FinFET performance?

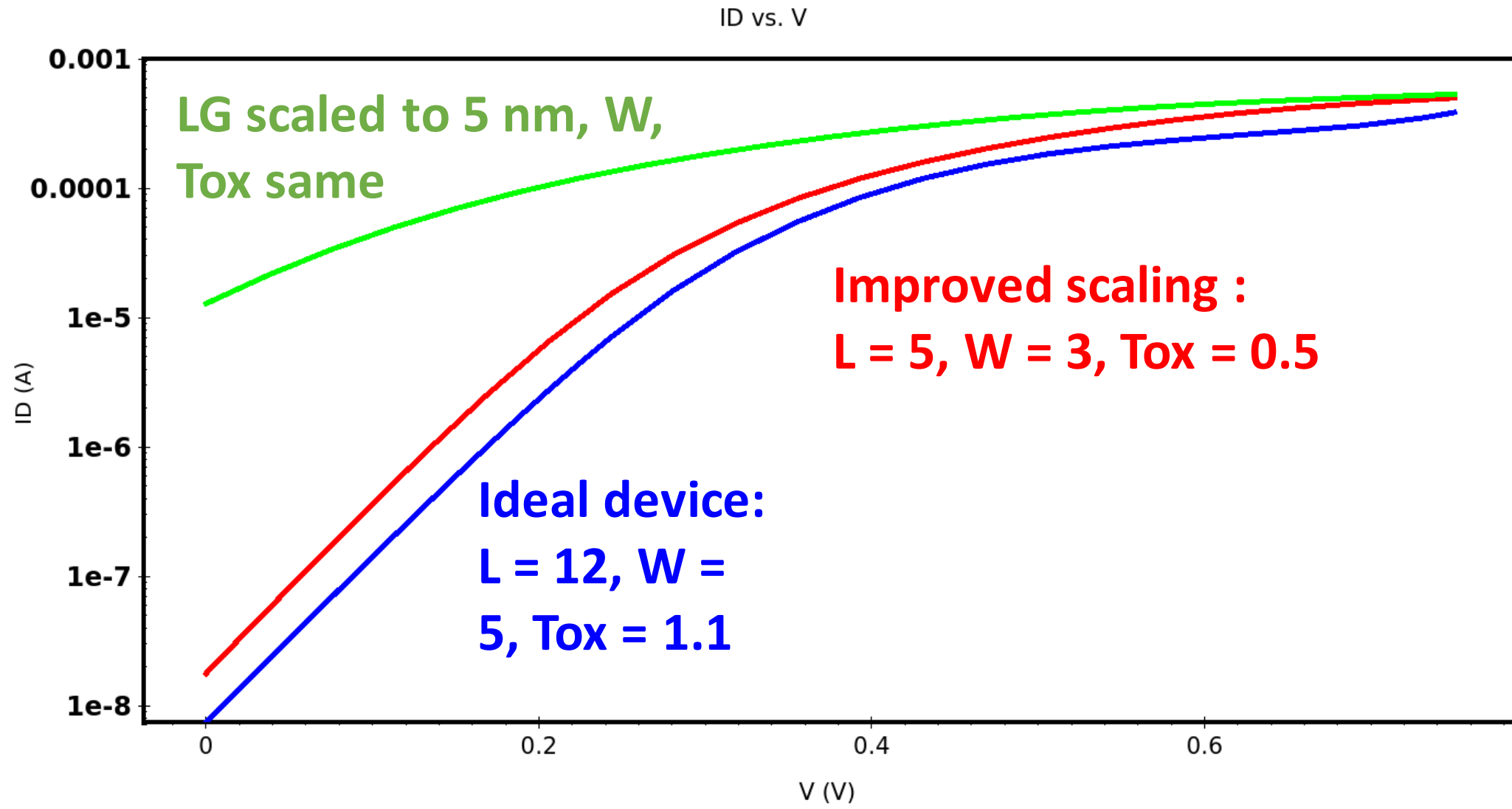
1. What are the parameters to be considered for performance improvement?

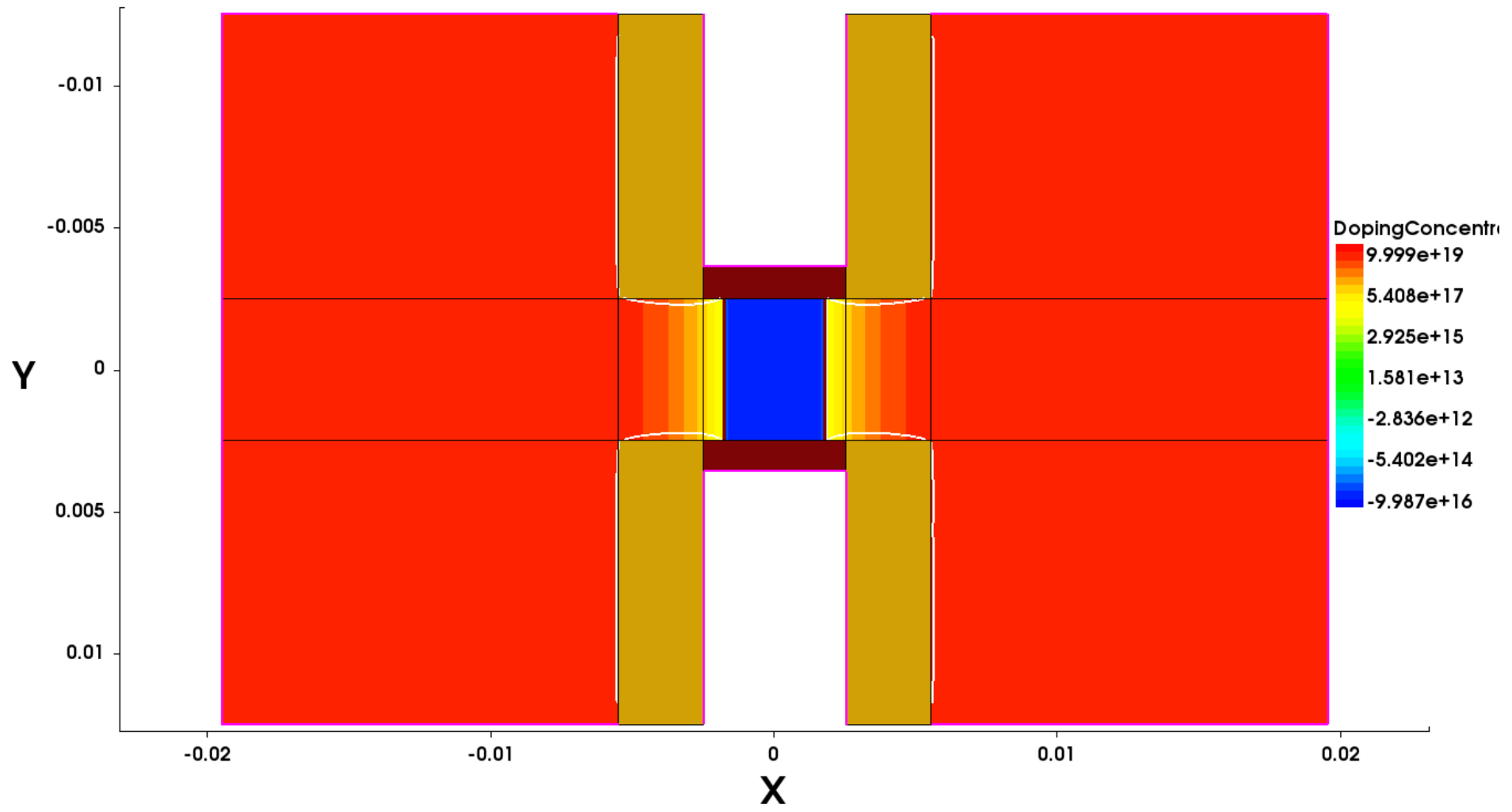
- On-current, OFF current, SS, DIBL
- What about parasitic capacitance?

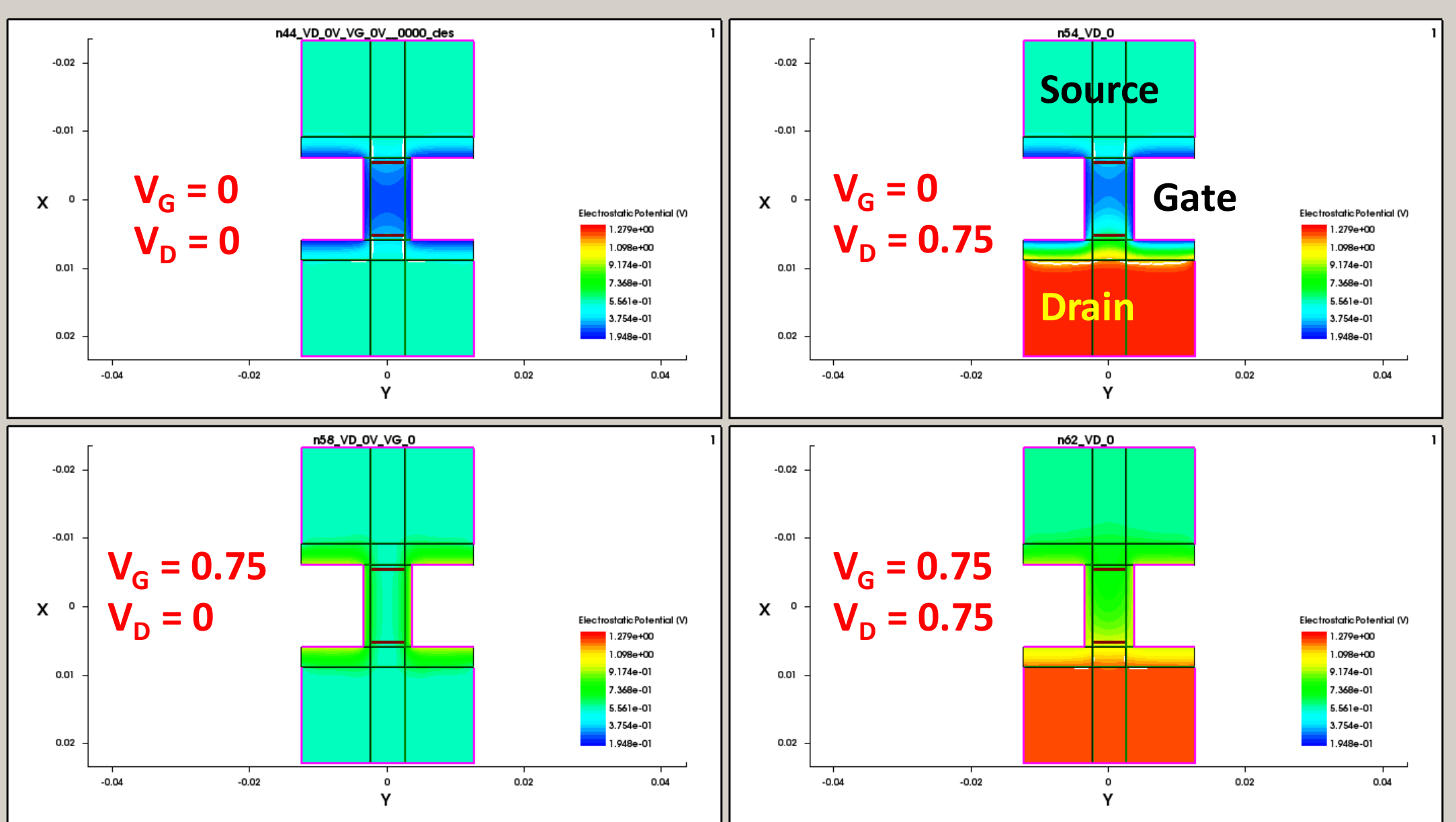
2. How to do it?

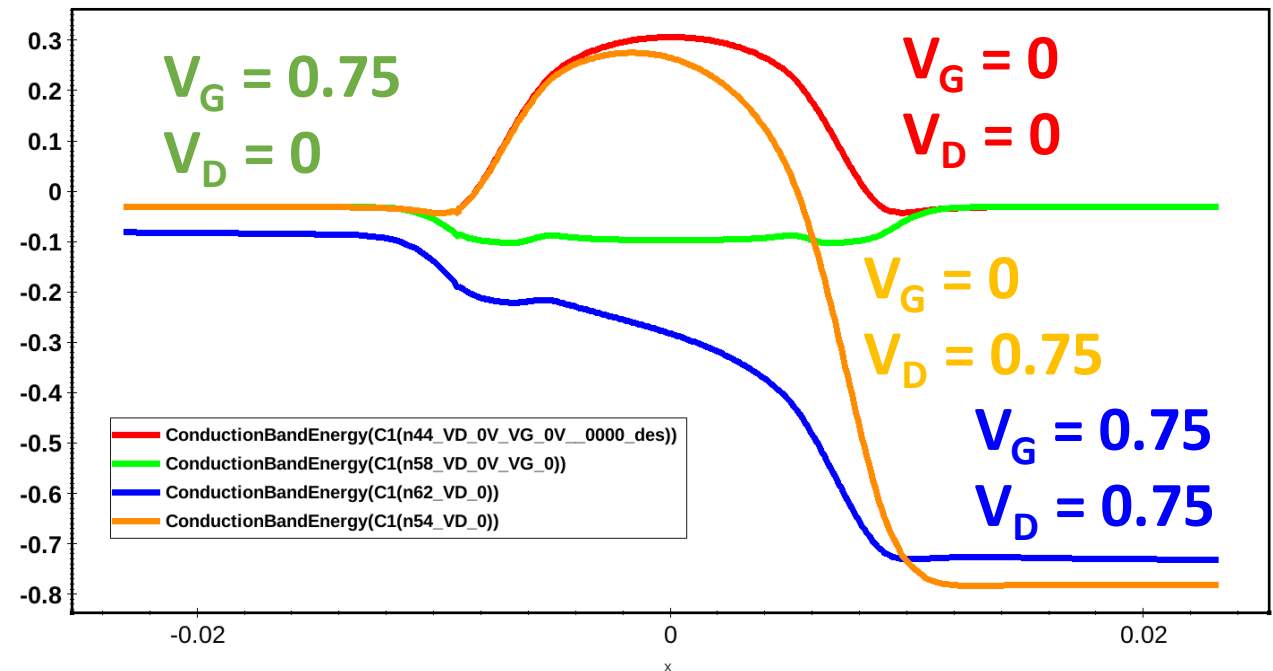
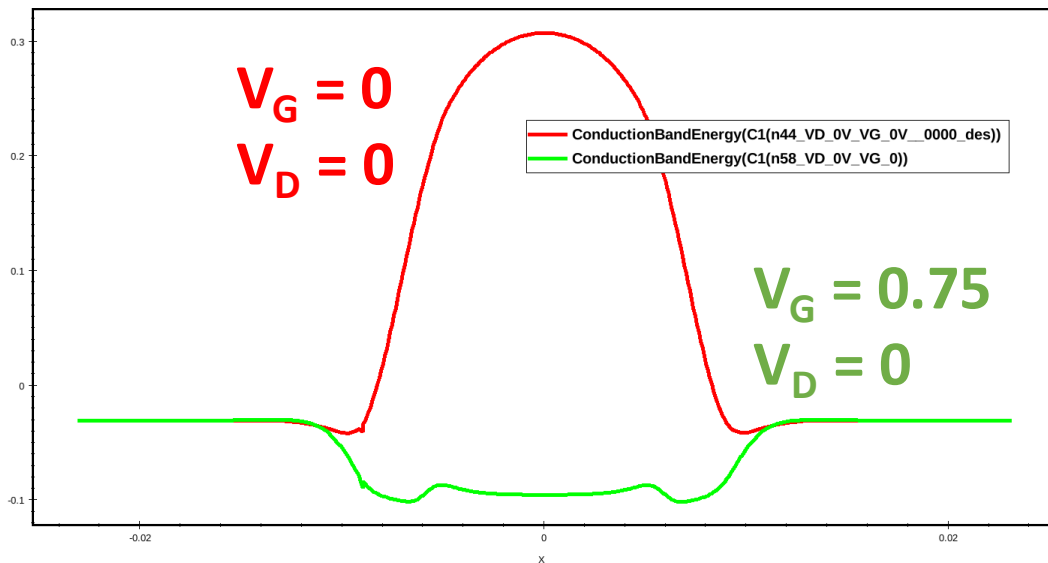
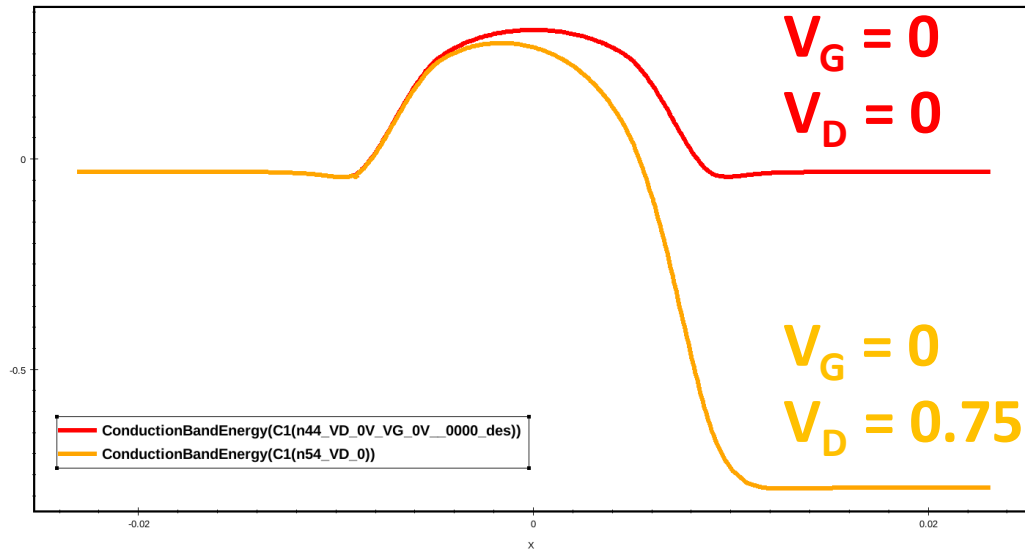
- L_G scaling: is it only enough?
 - Draw EBD for long and short L_G
- L_G and W : Will the performance improve
- What about T_{ox} ?
 - Can you keep on scaling it?
 - What about the gate leakage current?
- L_G , W , H , and T_{ox}

FinFET design: Designer perspective

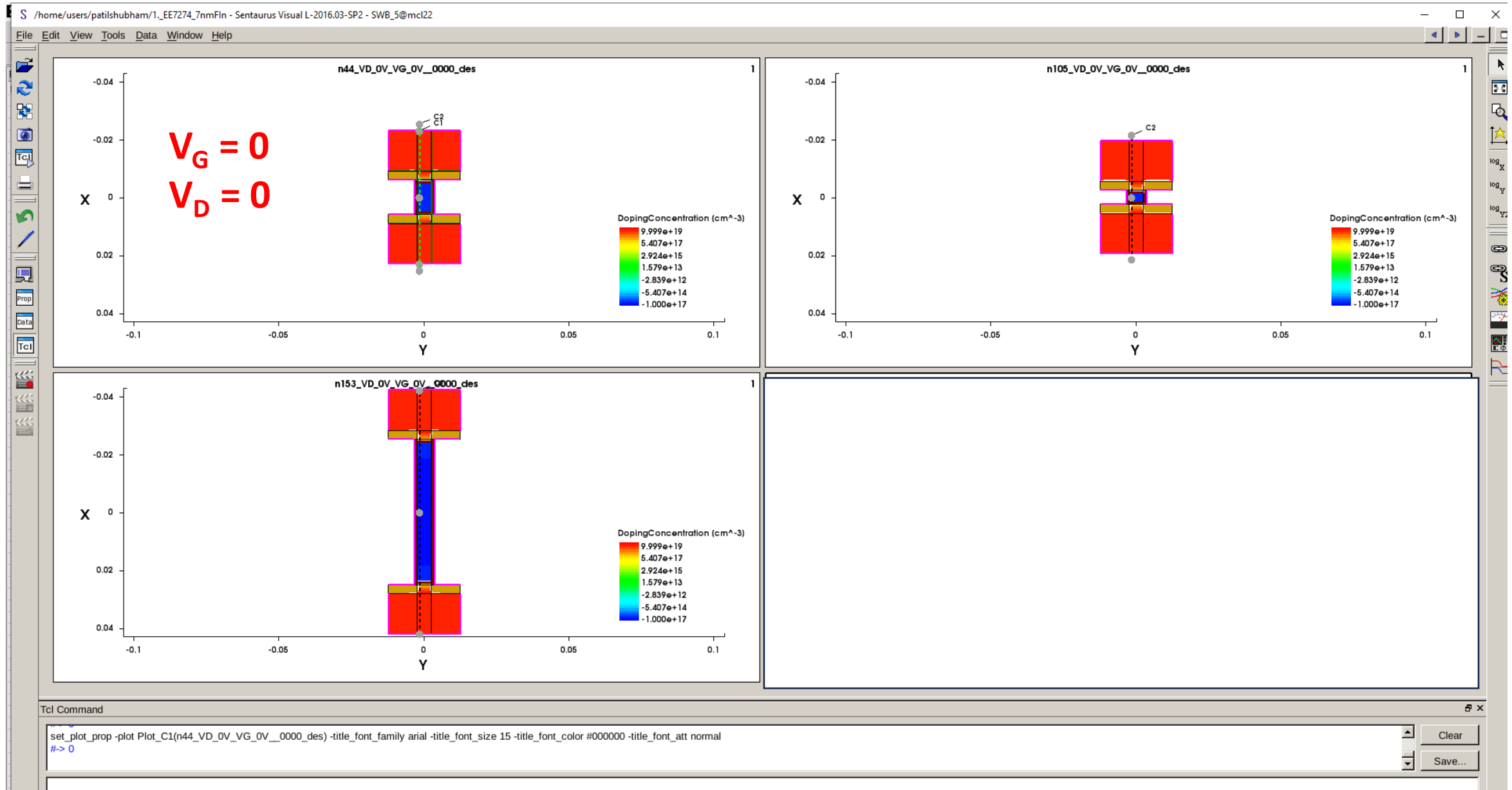




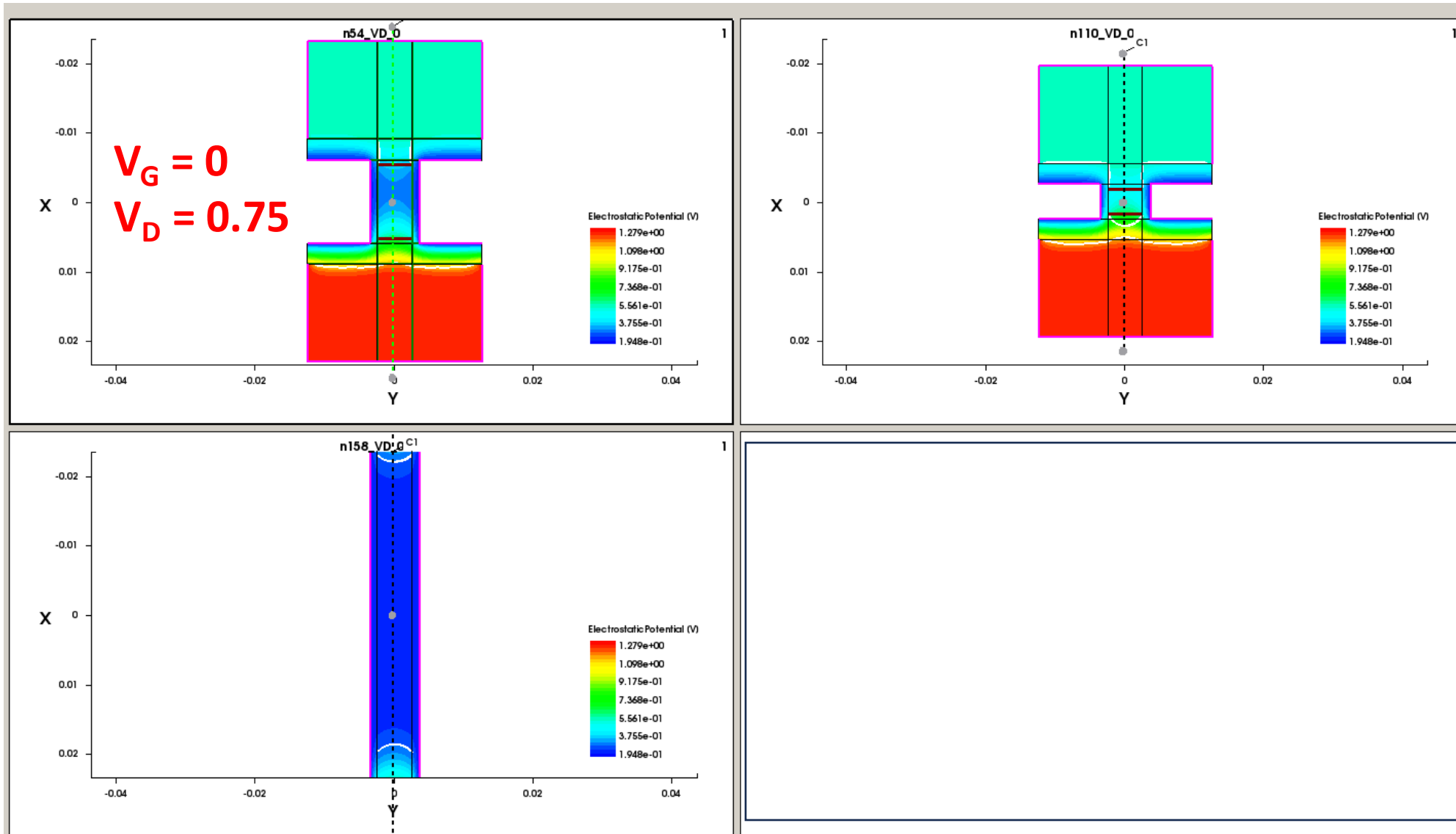




FinFET: L_G scaling impact



FinFET: L_G scaling impact



- Define BOX

(sdegeo:create-rectangle (position 0 0 0) (position L W 0) "Germanium" "R.Sub")

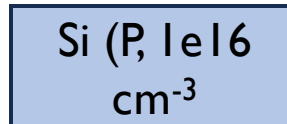
- Germanium: Replace your material (Silicon, Oxide, HfO₂, Nitride...)
- R.Sub**: Dummy name for the box, works as its identity



- Define doping in BOX

(sdedr:define-constant-profile "Const.Sub" "BoronActiveConcentration" 1e16)

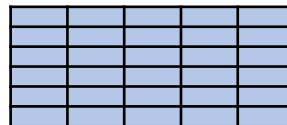
(sdedr:define-constant-profile-region "PlaceCD.Sub" "Const.Sub" "R.Sub")



- Meshing in BOX

(sdedr:define-refinement-size "size_R.Sub2" 0.01 0.01 00.01 0.002 0.005 0.005)

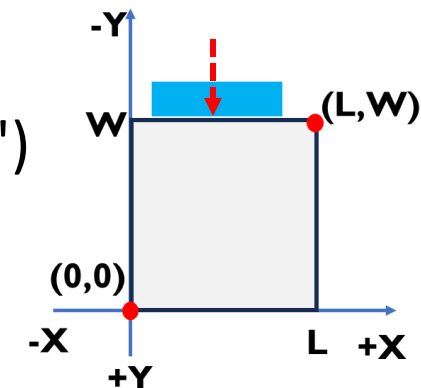
(sdedr:define-refinement-placement "Place_R.Sub" "size_R.Sub2" "R.Sub")



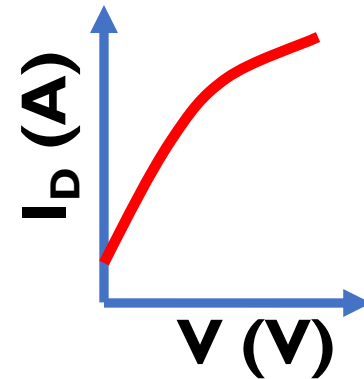
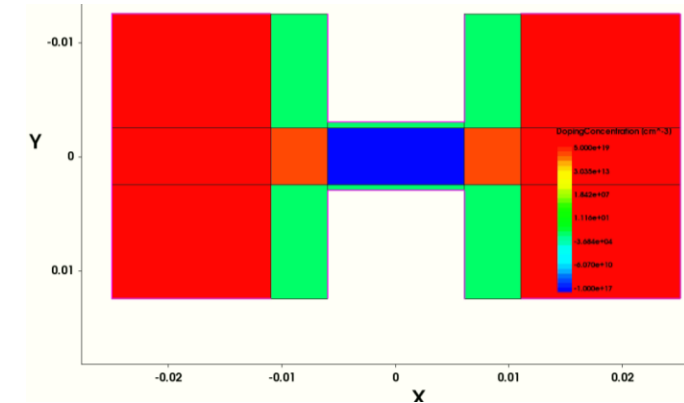
- Contact

(sdegeo:set-contact (find-edge-id (position (/ L 2) W 0.0)) "drain")

- Save TDR: (sde:build-mesh "SOI_n@node@")



- Syntax: _____.cmd
- Section
 - File: I/p and o/p files
 - Electrode: All the contacts (Source, Drain, Gate ...)
 - Physics: All models for simulation (Transport, Fermi, Recombination/Generation, Mobility models)
 - Plot: Variables to be visualized (V , E , I , n_e , n_h)
 - Math: Control for the solver (Iterations, accuracy, method...)
 - Solve: Simulation condition (Ramping of voltages)



[TCAD Sentaurus Hands-on Tutorial: Sentaurus Workbench and Structure Editor and SVisual](#)

MOSFET: Sdevice File for reference

- Working with TCAD
- Visualize TDR and analyze 3D and 2D structure
 - Electrostatic profiles
- FinFET Device designing
 - Scaling
 - EBD

Thank You

Stay cool