TMR0IF TMR0IE TMR0IP RBIF RBIE RBIP Wake-up if in Idle or Sleep modes INTOIF INTOIE INT1IF INT1IE INT1IP INT2IF INT2IE INT2IP Interrupt to CPU Vector to Location 0008h PIR1<7:0> PIE1<7:0> IPR1<7:0> INT3IF INT3IE INT3IP GIEH/GIE PIR2<7:6, 4:0> ___ PIE2<7:6, 4:0> ___ IPR2<7:6, 4:0> ___ IPEN-PIR3<7:0> PIE3<7:0> IPR3<7:0> IPEN GIEL/PEIE **IPEN** High-Priority Interrupt Generation Low-Priority Interrupt Generation PIR1<7:0> PIE1<7:0> IPR1<7:0> PIR2<7:6, 4:0> — PIE2<7:6, 4:0> — IPR2<7:6, 4:0>— Interrupt to CPU Vector to Location TMR0IF TMR0IE IPEN-PIR3<7:0> PIE3<7:0> TMR0IP IPR3<7:0> GIEH/GIE RBIP GIEL/PEIE INT1IF __ INT1IE __ INT1IP INT2IF INT2IP-INT3IF INT3IE INT3IP

FIGURE 10-1: PIC18F8722 FAMILY INTERRUPT LOGIC