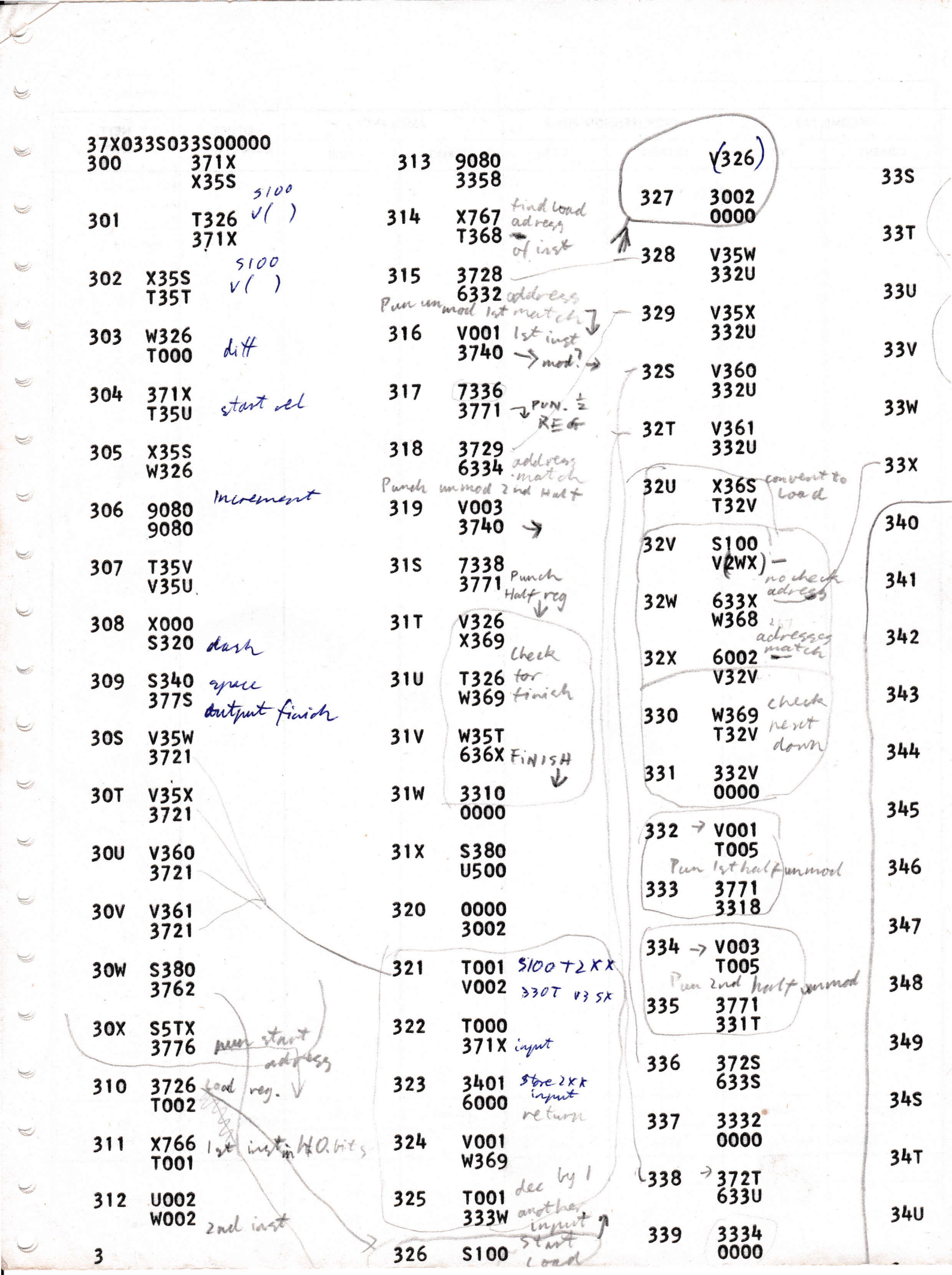
37X033S033S00000
300 371X X35S
301 T326 371X
302 X35S T35T
303 W326 T000
304 371X T35U
305 X35S W326
306 9080 9080
307 T35V V35U
308 X000 S320
309 S340 377S
30S V35W 3721
30T V35X 3721
30U V360 3721
30V V361 3721
30W S380 3762
30X S5TX 3776
310 3726 T002
311 X766 T001
312 U002 W002
3
313 9080 3358
314 X767 T368
315 3728 6332
316 V001 3740
317 7336 3771
318 3729 6334
319 V003 3740
31S 7338 3771
31T V326 X369
31U T326 W369
31V W35T 636X
31W 3310 0000
31X S380 U500
320 0000 3002
321 T001 V002
322 T000 371X
323 3401 6000
324 V001 W369
325 T001 333W
326 S100
(326)
327 3002 0000
328 V35W 332U
329 V35X 332U
32S V360 332U
32T V361 332U
32U X36S T32V
32V S100 V2WX)
32W 633X W368
32X 6002 V32V
330 W369 T32V
331 332V 0000
332 V001 T005
333 3771 3318
334 V003 T005
335 3771 331T
336 372S 633S
337 3332 0000
338 372T 633U
339 3334 0000
33S
33T
33U
33V
33W
33X
340
341
342
343
344
345
346
347
348
349
34S
34T
34U
S100 V( )
S100 V( )
diff
start rel
increment
dash
space
output finish
find load address of inst
address match 1st inst
1st inst mod?
PUN. ½ REG
address match 2nd Half
Punch Half reg
Check for finish
FINISH
convert to load
no check address
2 addresses match
check reset down
Pun 1st half unmod
Pun 2nd half unmod
S100 T2XX
330T V35X
input
store 2XX input return
dec by 1 another input
start load
pun start address
load reg.
1st inst in HO bits
2nd inst

1st set no mod 1st half
2nd set no mod 2nd half
3rd set forced mod on 1st half if begin Ø
4th set forced mod on 2nd half if begin Ø

k

NA
A
NA
A
NA
A
A
A
NA

```
34V   U500   9  NA
      3002

34W   U500   IS NA
      3002

34X   V005   F  A
      3354

350   U500   D  NA
      3002

351   V005   V  A
      3354

352   V005   W  A
      3354

353   V005   X  A
      3354

354   X76V   find adress
      W36W

355   7350   FA.REG
      V005   orig inst

356   X35V   inc
      T005

357   3350
      0000

358   9080
      T003   2nd inst in H.O. Bits

359   V326
      3314

35S   S100   Data
      V000

35T   S100   Finishing
      V886   Load (326)

35U   0000   ~~diff~~ start reloc
      0300

35V   0100   increment top half
      0000

35W   S100
      T2XX

35X   S100
      T2WX

360   S100
      T2VX

361   S100
      T2UX
```

Leader

```
362   U401   hitt on 1 no leader
      7002

363   V369
      8002   Gen 100

364   S540
      W369

365   6002
      3364

366   XXXX   (311)
      0000

367   0000   (314)
      0XXX

368   0000   load address of inst
      0267
      (314)

369   0000
      0001

36S   0000
      2000

36T   X000   (341)
      0000

36U   3344
      0000

36V   0TXX   (394)
      0000

36W   0007   (354)
      0000
```

FINISH

```
36X   S380
      S5W0   End code

370   3762   Leader
      3300
```

~~Print~~ Half reg

```
371   V005
      S07X   PUNCH

372   8U20   6
      S47X

373   8U20   6
      S47X

374   9802   ?
      8U20   6

375   S47X
      3002

376   V35U
      9080
```

```
377   9080
      9008   PUNCH START

378   ADRES  8U20
             S47X

379          8U20
             3375

37S   S07X   Output finis
      9080   register

37T   9008
      9080

37U   377W
      377W

37V   377W
      330S

37W   8U08
      U005

37X   6383
      W384

380   7386
      X385

381   U005
      S27X

382   3002
      0000

383   9410
      3381

384   0000
      000S

385   0000
      0012

386   X384
      3381
```