

[illegible]

2SV 3601 3601 2X0 3006 6400
2SW 36TU V2T8 2X1 V005 32WW 340
2SX X3U5 T2T8 2X1 V005 X771 341
2TO V004 X3U3 2X2 14 X3U8 32WW 342
2T1 T004 32S5 2X3 V005 X771 343
2T2 V2T3 T238 2X4 7 X3U9 32WW 344
2T3 00SS 32T3 2X5 35X3 X36S 345
2T4 XXXX XU00 2X6 62X9 X36V 346
2T5 0000 00XX 2X7 T005 3623 347
2T6 T000 V08S 2X8 32W8 6400 348
2T7 02T7 W000 2X9 3620 32V5 349
2T8 0UW9 0869 2XS X4 V002 T3W2 34S
2T9 T2T8 T08S 2XT 35X3 X3US 34T
2TS T000 V1WW 2XU 16315 X3UT 34U
2TT 6234 326U 2XV 7314 W374 34V
2TU type V3VW W36T 2XW 5 6363 X3TU 34W
2TV out 62TX T3VW 2XX T005 3623 34X
2TW next S35W 3002 300 6310 3400 350
2TX line? S380 V370 301 V3W0 X36T 351
2U0 T3VW 3002 302 Tab 362T 6305 352
2U1 S07X 8U08 303 363S V3VT 353
2U2 U005 62U7 304 T3W0 6400 354
2U3 W393 72U8 305 V2T8 X773 355
2U4 X394 6400 306 9080 9080 356
2U5 U005 S27X 307 X3W2 370V 357
2U6 3002 6400 308 3727 330U 358
2U7 X384 32U5 309 0000 0026 359
2U8 X393 32U5 30S S351 X309 35S
2U9 V005 T008 30T S35V 3312 35T
2US V008 3002 30U 3655 32V5 35U
2UT line con 36TX 36S0 T.O. 30V S07X 8U20 35V
2UU 0001 6400 30W S47X 8U20 35W
2UV 36TX S380 30X S47X 3002 35X
2UW V3U6 36VX 310 3620 3301 360
2UX 36VV 3620 311 630S X309 361
2V0 6400 V003 312 U005 S27X 362
2V1 S5TX V3V8 313 623X 323V 363
2V2 9080 9080 314 X370 6400 364
2V3 9008 8U80 315 T003 3743 365
2V4 370W S47X 3727 316 V003 3319 366
2V5 36V8 36W1 317 V002 3741 367
2V6 36W6 3622 318 V003 9080 368
2V7 32W8 6400 319 9080 9080 369
2V8 V002 35X2 31S X3W2 370V 36S
2V9 X36U 634X 31T 3727 330U 36T
2VS W374 62X5 31U V002 T3W2 36U
2VT W36X 61X3 31V U500 T003 36V
2VU 3004 6400 31W 35X3 X36S 36W
2VV 2400 W3TU 31X 6326 W36X 36X
2VW 6002 32VV 320 6325 X36W 370
2VX S540 X36T 321 9080 9080 371
2W0 72VX 3002 322 X3T8 W3U3 372
2W1 V002 T001 323 3406 X003 373
2W2 V3VU X76T 324 T003 331W 374
2W3 6001 V3T6 325 V003 331S 375
2W4 370V 3727 326 3620 3325 376
2W5 3655 3001 327 S07X 8U08 377
2W6 2400 W36V 328 S47X 3002 378
2W7 6002 32W6 329 0001 0000 379
2W8 V005 X6T4 32S 0002 0000 37S
2W9 62X0 V005 32T 0004 0000 37T
2WS X790 62X1 32U 0008 0000 37U
2WT V005 X784 32V 0010 0000 37V
2WU 62X3 V005 32W 0020 0000 37W
2WV X771 X3U7 32X 0040 0000 37X
2WW X3T6 W394 330 0080 0000

3345 6400
T3W2 U500
T003 6400
V002 T004
35X3 X36S
7349 6348
W36X 6004
0055 3344
3620 3004
X3UV 734W
634T X372
U003 9008
X003 T003
3344 6400
X384 334T
36W1 V3TS
T351 6400
V012 6356
370V 3727
370V 3727
V351 X3U3
T351 3351
S5W0 V3U6
36VX 0000
V005 T008
6400 V003
6234 326U
U500 T3VU
T3VS T008
V3T9 T001
V3T7 T002
V3UW T003
V362 T005
V3UX T004
7002 31X8
3658 V000
W27V 9880
9880 X3VX
3306 6400
36XS W000
36XS T000
0000 003S
0000 0021
0000 0001
0000 002W
0000 001W
0000 0080
0000 0062
0000 0004
0000 003X
0000 0008
0000 03XX
0000 000V
0000 006X
36XS 3000
371U U400
371U 9000
36XS 5000
373T 6400
3731 S100
36XS X400
0000 0002
371U 9800
0000 000T
Assemble
(21)
Sum
TAB
(82) -> ER
discard to
(5-X)
orig char
much
constant
final
branch
(constant)
mess start
for restart
from 363
2XW
S
T
prog regs typed per line
for X4
0000 00
1 8 1
R B

380	36XS	3400	JM
381	36XS	7000	JN
382	36XS	6000	JZ
383	37IU	9U00	
384	0000	0010	
385	3717	S07X	O
386	31 36XS	X000	A W
387	20 36XS	0000	B
388	3396	0000	C
389	36XS	1000	D
38S	35 379T	0800	E
38T	0000	000X	
38U	27 3731	0000	G
38V	373T	0000	
38W	39 3717	2000	I
38X	36XS	V000	CA
390	0000	0020	
391	339V	0000	
392	33T1	0000	
393	0000	000S	
394	0000	0012	
395	3334	0000	
396	35X3	X369	35
397	6399	W36T	B
398	639S	31X3	6
399	373T	S07X	2
39S	373T	U500	
39T	V002	37S4	
39U	U500	331S	
39V	V005	9820	
39W	W3V0	63T0	
39X	W3UT	63SX	
3S0	W3V1	63S3	
3S1	V3V2	6400	
3S2	37S4	331S	
3S3	V3V3	33S2	
3S4	T3W2	V3V9	
3S5	63S6	331S	
3S6	V002	T004	
3S7	35X3	X3V4	
3S8	63SU	X3V5	
3S9	63SV	W3V5	
3SS	T003	373W	
3ST	V003	3319	
3SU	3620	3004	
3SV	V3V6	X3W2	
3SW	3741	33ST	
3SX	371U	8U00	
3T0	36XS	U000	
3T1	V005	9820	
3T2	W3V7	63T4	
3T3	33T5	6400	
3T4	371U	8000	
3T5	371U	8800	
3T6	6400	3367	
3T7	U500	T08S	
3T8	V329	3002	
3T9	U500	T1WX	
3TS	V008	6356	
3TT	V005	T08S	
3TU	0000	0011	
3TV	8000	00TX	
3TW	0000	0300	
3TX	423U	0000	

331	V002	3741
332	V003	3319
333	3620	331S
334	36W1	3655
335	V3V9	633S
336	U500	T003
337	V003	370V
338	WV 3727	370V
339	WV 3727	330U
33S	3741	3337
33T	V002	T3W2
33U	V3V9	6333
33V	U500	331S
33W	V002	T004
33X	U500	U003

read, punch

clear

11,011111,0111

0000	0VX7
3U1	6400 V003
3U2	V000 X004
3U3	0001 0000
3U4	6100 1000
3U5	0010 0000
3U6	XXXX XX9U
3U7	0000 0009
3U8	0000 0014
3U9	0000 0007
3US	0000 002X
3UT	0000 000U
3UU	8000 0000
3UV	0000 000W
3UW	9401 X002
3UX	T002 W001
3V0	0000 0017
3V1	0000 0003
3V2	4000 0000
3V3	4800 0000
3V4	0000 0021
3V5	0000 000V
3V6	0200 0000
3V7	0000 0023
3V8	0000 0010
3V9	0000 0001
3VS	0000 000S
3VT	0000 007V
3VU	0000 0188
3VV	TM V000 3364
3VW	0000 0003
3VX	0000 0072
3W0	0000 007U
3W1	0000 0300
3W2	3000 3377

→ start address
 1 on CR input
 → clear on tab input
 1st or 2nd? 0-2nd 1-4th
 clearable
 → store address
 clearable
 instruction count
 registers to type on this line
 half reg count?
 saved reg

6500
 507X