Jinwei YAO

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EDUCATION

College of Information Science & Electronic Engineering, **Zhejiang University**
B.Eng. in Electronic Science and Technology Sept. 2018 - Jun. 2022 (expected)

Overall GPA: 3.87/4.00 (86.91/100)
Selected EECS courses: Network and Communication Security, Computer Organization and Architecture, Artificial Intelligence, Numerical Analysis, Fundamentals of C Programming, Fundamentals of Data Structures, Digital Image Processing

RESEARCH EXPERIENCE

Accelerating Graph Neural Network Sampling by Customizing FPGA Subsystem Nov. 2021 - Present
Ongoing. Advisor: Prof. Zeke Wang RC4ML Laboratory, Zhejiang University, China

- Motivation: Graph sampling, as the first step for GNN training, is a time-consuming irregular computation on modern CPU.
- Goal: Customize an FPGA-based memory subsystem with High Bandwidth Memory (HBM) for graph sampling acceleration.

Power-based Side-channel Disassembly Attacks on Shared FPGA Jul. 2021 - Nov. 2021
Advisor: Dr. Mirjana Stojilovic Parallel Systems Architecture Laboratory, EPFL, Switzerland

- Accepted to **Summer@EPFL Program(acceptance rate in 2021 was 1.5%)**.
- The research was about power side-channel disassembly attacks on an FPGA softcore processor.
- Skills in this project: VHDL, python, assembly
- Sincerely hope you understand: Details are omitted as we have a DAC submission under double-blind review.

Frequency and Transfer Learning-based Power Analysis Jul. 2020 - June. 2021
Advisor: Prof. Fan Zhang Institute of Cyber Security Research, Zhejiang University, China

- Motivation: The limited traces from profiling device causes traditional deep-learning based side-channel attacks difficult to work, especially cross-device attacks.
- Goal: Overcome the gap in different data distributions between traces from different devices.
- Insight: Transfer learning can make use of the similarities between data distributions of different devices, and the information in the frequency domain has more leakages.
- Contribution: Proposed and applied frequency transfer learning-based power analysis (FTL-PA) to perform cross-device attacks by using frequency information of the traces.
- Results: FTL-PA is significantly more effective than existing works (including transfer learning-based side-channel analysis) with fewer (e.g, 10) profiling traces needed.

PROJECTS

Parallel Matrix Multiplication Multi-accelerators based on Gemmini May. 2021 - June. 2021

The final project for Computer Organization and Architecture (earned 4.0/4.0) course is to design an architecture based on Berkeley Rocket Ecosystem to speed up the multiplication of two matrices.

The main idea of my design is to split metrix A to two metrices A1 and A2, then calculate A1*B and A2*B in two different accelerators parallelly.

Designed an architecture that has a rocket core with 2 Gemmini-based accelerators using different RoCC custom settings.

Realized the address mapping between two accelerators and DRAM to output the result.

PAPERS

J. Yao, Z. Lu, F. Zang, et al. "Transfer Learning-based SCA in Sample-constrained Scenario: Fine-tune the DNNs with Prior Knowledge of Cross-device," In DAC 2021, December 2021. (Co-first author, EDA Top Conference, rejected, but accepted as WIP (Work-in-progress), ready to be resubmitted)

O. Glamocanin, **J. Yao**, N. Ardo, M. Stojilovic. "Title omitted for double-blind review". CHES 2022(under review). **Key Words: Power side-channel attack, Disassembly, FPGA, Softcore processor.**

HONORS & AWARDS

Academic Fellowship and Academic Excellence Award	2020-2021
Innovation Achievement Award	2020-2021
Winner's Prize of National College Student Information Security Contest	Aug. 2021
The Third Prize of Zhejiang Province Physics Competition for College Students	2020
Third Prize of Kaitai Cup Entrepreneurship Competition(co-organized by Zhejiang Univ. and Kaitai Investment Company)	2020
Academic Fellowship and Academic Excellence Award	2018-2019
Artistic and Athletic Achievement Award	2018-2019
Outstanding Student of Zhejiang University	2018-2019

SKILLS

Programming	Experienced: C, Python, Verilog, MATLAB Familiar: VHDL, Scala, C++
Language	IELTS: 7.0 (Listening 6.5/Reading 8.5/ Writing 6/ Speaking 6)