A Novel Single Switch Transformerless Quadratic DC/DC Buck-Boost Converter

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« Buck-boost converter », « Converter circuit », « Converter control », « DC/DC converter », « Efficiency », « MOSFET»

Abstract

A novel quadratic buck-boost DC/DC converter is presented in this study. The proposed converter utilizes only one active switch and can step-up/down the input voltage, while the existing single switch quadratic buck/boost converters can only work in step-up or step-down mode. First, the proposed converter is analyzed in steady-state. Then, its performance is validated using simulations in MATLAB/Simulink software. Finally, an experimental prototype is built for further verification.

Introduction

DC/DC converters with step-up/down ability are widely used in renewable energy systems such as photovoltaic and fuel cells, where the input voltage is varying by the time and is depending on many factors. The conventional buck/boost converter is the simplest structure with step-up/down ability. However, its voltage gain is limited due to the parasitic effect of the circuit elements [1]. The voltage gains of the other conventional buck-boost converters such as CUK, SEPIC and ZETA is same as the gain of the basic buck-boost converter, which may not be sufficient in renewable energy systems. In recent years, many DC/DC converters with high step-up ability have been introduced in literature [2]-[9]. However, they only work in step-up mode and cannot step-down the input voltage. Several quadratic DC/DC converters have been presented in [10]-[15]. Despite of their quadratic voltage gain, the proposed converters in [10]-[11] are only able to work in step-down or step-up mode, in practice. Single switch buck-boost converters are introduced in [12]-[13]. However, the negative terminal of the input voltage and output voltage do not share the common ground, which is not desired in many applications such as photovoltaic system. A new quadratic buck-boost converter has been recently introduced in [14], which utilizes two power switches in its structure. Therefore, two distinct gate drivers are required that may lead to a higher cost and lower reliability. Another new buck-boost converter has been introduced in [15]. In this topology, three inductors and four capacitors are used which increases the cost and size.

In this study, a new quadratic buck-boost converter is presented. The main features of the proposed converter are listed below

i. Higher voltage gain in comparison with the similar counterparts in [10]-[15], can be obtained.
ii. Unlike the existing single switch quadratic buck-boost converters [10]-[11], the proposed converter can work properly in both step-up/down modes.
iii. The input and output voltage is sharing a common ground, unlike the converters in [12]-[13].
iv. The proposed converter has fewer components in comparison with [15], while the voltage gain is improved.

This paper is organized as follows. In the next section, the proposed converter is introduced along with its voltage gain and characteristics. In addition, a comparison has been made with the existing structures in terms of the voltage gain and the voltage stress of the switches. Then, the proposed converter is simulated using MATLAB/Simulink software. The performance of the proposed converter is also validated using experimental results with 12 V input voltage, while the output is set at 5 V and 48 V in step-up and step-down modes, respectively.

Proposed converter

The proposed converter is shown in Fig. 1. It consists of a power switch, three diodes, two inductors and two capacitors. There are two operational modes when the converter works in continuous conduction mode (CCM). Fig. 2(a) and Fig. 2(b) respectively show the equivalent circuits when the power switch is ON and OFF.

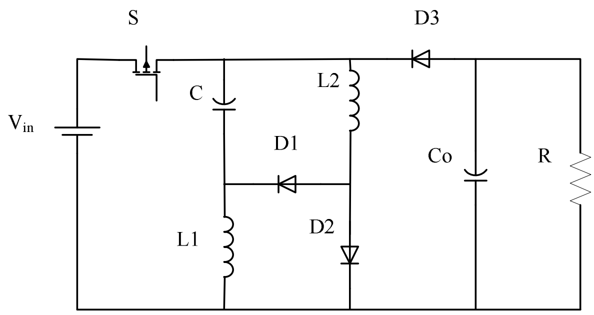


Fig. 1. Proposed single switch quadratic buck-boost converter

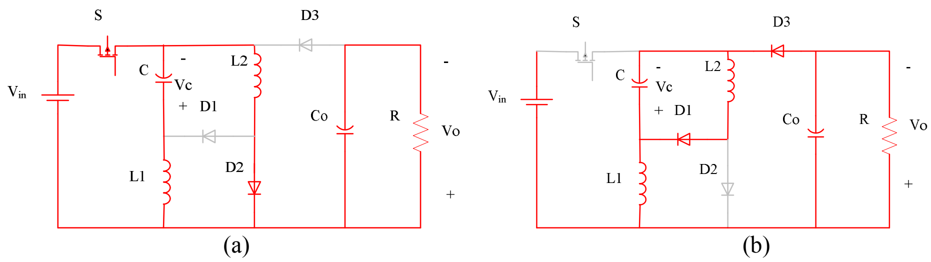


Fig. 2. Equivalent circuits when (a) the power switch is ON (b) the power switch is OFF

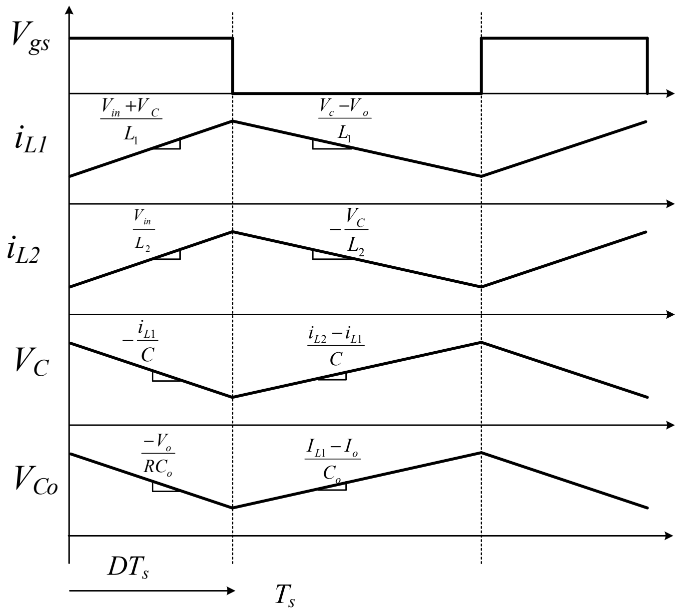


Fig. 3. Key waveforms of the proposed converter

The key waveforms of the converter namely the current waveforms of inductors L_1 and L_2 and also the voltage waveforms of the voltage across the capacitors C and C_o are shown in Fig.3.

Using Fig. 2(a) and applying the KVL, the following equations can be obtained when the power switch is turned on:

$$V_{L1}(on) = V_{in} + V_c \quad (1)$$

$$V_{L2}(on) = V_{in} \quad (2)$$

Also, using Fig. 2(b) when the power switch is turned off, these equations can be obtained

$$V_{L1}(off) = V_C - V_O \quad (3)$$

$$V_{L2}(off) = -V_C \quad (4)$$

Therefore, using volt-second balance principle on L_1 and L_2, one can obtain (5) and (6) which result to (7) and (8).

$$D(V_{in} + V_C) - (1-D)V_C = 0 \quad (5)$$

$$DV_{in} + (1-D)(V_C - V_O) = 0 \quad (6)$$

$$V_C = \frac{DV_{in}}{1-D} \quad (7)$$

$$V_O = \frac{(2D-D^2)V_{in}}{(1-D)^2} \quad (8)$$

Hence, the voltage gain for proposed converter is defined by

$$M = \frac{(2D-D^2)}{(1-D)^2} \quad (9)$$

Fig. 4 compares the voltage gain of the proposed converter with the conventional buck-boost converter and the other converters in [12]-[15].

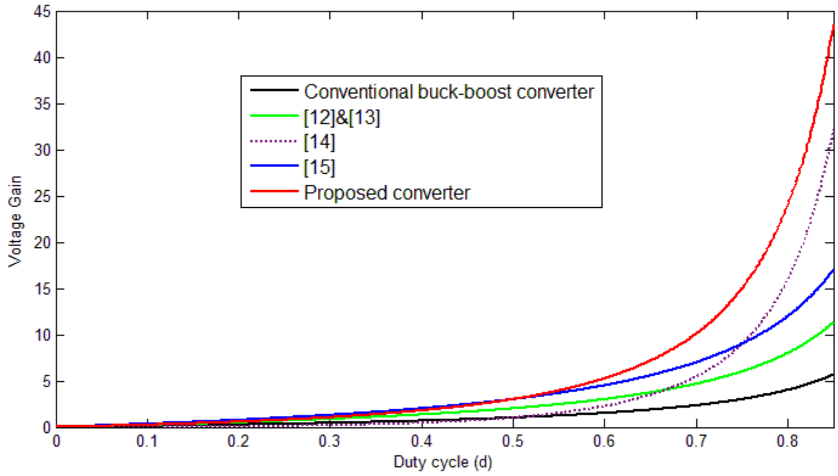


Fig. 4. Voltage gain comparison of the proposed converter and other converters

Referring to Fig. 4, it is clear that the proposed converter has the highest voltage gain in comparison with the other buck-boost converters. Also, Table I compares the number of circuit components of the proposed converter with the existing topologies. According Table I, the proposed converter and converters in [12] and [14] have the lowest number of elements. It is worth noting that the converter in [14] has two power switches and consequently two gate drivers are required which leads to higher cost. The converter in [12], has lower voltage gain than the proposed converter, and its input - output terminals do not share the common ground that is not desirable in some applications. The converters in [13] and [15] have higher circuit elements and lower voltage gain in comparison with the proposed converter.

The voltage stress across the power switch is equal to

$$V_s = V_{in} + V_O = \frac{V_{in}}{(1-D)^2} \quad (10)$$

Using (10), the normalized voltage stress on switch is

$$V_S(N) = M + 1 \tag{11}$$

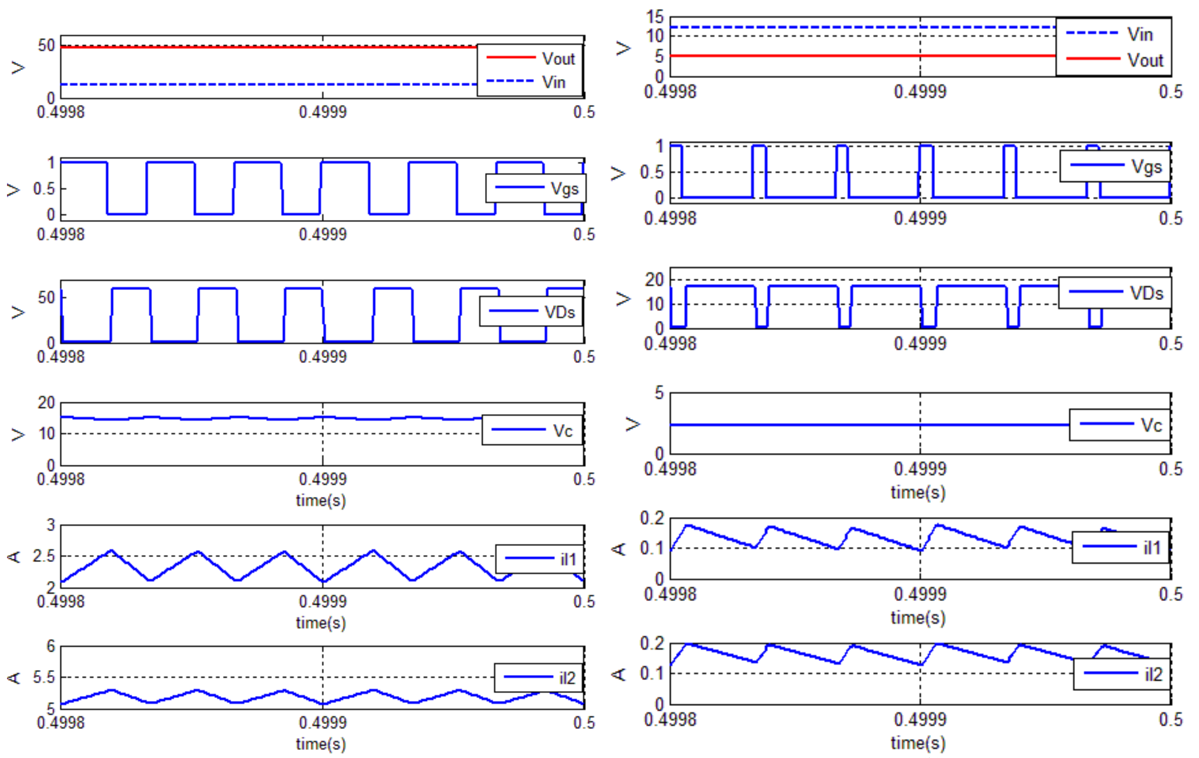
where, M is the voltage gain. From (11), it is clear that the normalized switch voltage stress of the proposed converter is equal to the normalized switch voltage stress of the conventional buck-boost converter.

TABLE I. The number of circuit components in the proposed and the other converters

Topology	No. of switches	No. of diodes	No. of inductors	No. of capacitors	Total
Proposed converter	1	3	2	2	8
Converter in [12]	1	2	2	3	8
Converter in [13]	1	2	3	4	10
Converter in [14]	2	2	2	2	8
Converter in [15]	1	3	3	4	11

Simulation results

The proposed converter has been firstly simulated by MATLAB/Simulink, and then tested by a laboratory prototype. The parameter specifications are presented in Table II. The proposed topology was firstly tested in the step-up mode to augment the voltage level from *12 V* to *48 V*. Fig. 5(a) shows the simulation results in this mode. The input voltage is set to *12 V*, while the obtained output voltage is *48 V*. Furthermore, the gat-source signal and the drain-source voltage are presented which are in accordance to the analysis. The drain-source voltage varies between $0 \sim V_{in}+V_o$ which is observed in V_{DS} ($0 \sim 60V$). Besides, the voltage across the capacitor C is shown which is in compliance with (7) and is equal to *15 V*. Fig. 5(b) shows the simulation results, when the converter was then tested in step-down mode to step-down the voltage level from *12 V* to *5 V*. The gate-source signal and the drain-source voltage are also presented, which are in agreement with the analysis. The drain-source voltage varies between $0 \sim V_{in}+V_o$ which is observed in V_{DS} ($0 \sim 17V$). Also, the voltage across the capacitor C is in compliance with (7) and is equal to *2.5 V*.



(a) (b)

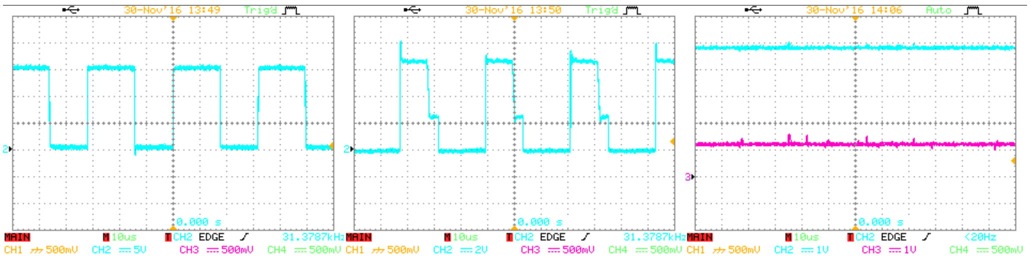
Fig 5. Simulation results : (a) step-up mode (b) step-down mode

Implementation results

Further verification was carried out by implementation of a laboratory prototype. The desired gating pulses for the switches are produced by *Arduino ATmega 2560*. The switching frequency was 32 *kHz* in both modes.

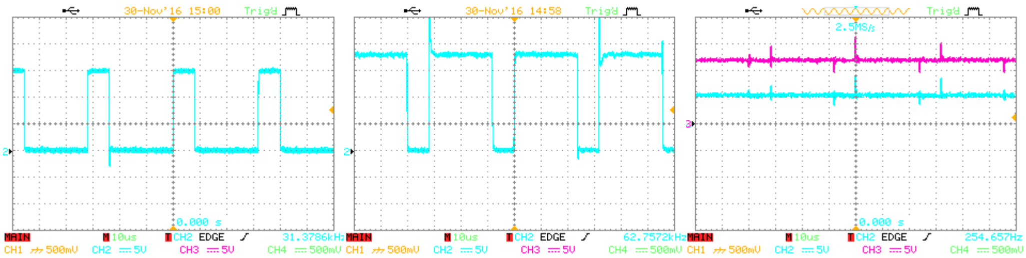
Fig. 6 shows the experimental results in the step-up mode. Fig. 6(a) shows the gate-source voltage of the switches. Fig. 6(b) illustrates the voltage across the MOSFETs which is in accordance to the simulation results and varies almost between *0~60 V*. The output voltage has been shown in Fig. 6(c) which is in accordance to the analytical and simulation results *(48 V)*.

The circuit was also tested in the step-down mode. Fig. 7(a) shows the gate-source voltage of the switches in this mode. Fig. 7(b) illustrates the voltage across the MOSFETs which is in accordance to the simulation results and varies between *0~17 V*. The output voltage has been shown in Fig. 7(c) which is in accordance to the analytical and simulation results *(5 V)*.



(a) (b) (c) (d)

Fig.6. experimental results in the step-up mode (time:10us/div)
(a) V_{GS} (5V/div), (b) V_{DS} (20V/div), (c) V_O (blue), V_{in} (red) (10V/div)



(a) (b) (c) (d)

Fig. 7. experimental results in the step-down mode (time:10us/div)
(a) V_{GS} (5V/div), (b) V_{DS} (5V/div), (c) V_O (blue), V_{in} (red) (5V/div)

TABLE II. Elements Specifications

Symbol	Description	Value
V_{in}/V_{out}	Input /output Voltage	Step-up mode: 12 *V* - 48 *V* Step-down mode: 12 *V* - 5 *V*
P	Power	Step-up mode: 49 *W* Step-down mode: 12.5 *W*
f_s	Switching frequency	32 *kHz*
D_1, D_2, D_3	DSEI12	11 *A*, 1200 *V*
S	IRF644	14 *A*, 250 *V*
L_1, L_2	2100HT-102-H-RC	1 *mH*
C	Nichicon, 200 *V*	47 μF
C_o	Elna, 200 *V*	270 μF
Microcontroller	Arduino Atmega 2560	--

Conclusion

A new buck-boost dc-dc converter was introduced in this paper. It has the ability to step-up/down the input voltage using only one power switch. The number of the components has been reduced in comparison with the existing topologies, while higher boost ability has been obtained. Performance of the proposed converter was verified both in step-up/down modes with simulations in MATLAB/Simulink as well as the experiments on a laboratory prototype.

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