A Controller for Cascaded H-Bridge Multilevel Inverter

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***Abstract*—The multilevel inverter technology has gained a tremendous significance in the research area. This paper proposed a new controller for generating the switching sequence of power devices used in multilevel inverter to produce the desired output. An embedded code has been developed to control the switching states of different IGBT switches. To validate the effectiveness of the proposed technique to control the multilevel inverter switching states MATLAB simulation of 3-level, 5-level and 17-level using cascaded H bridge topology of multi-level inverter is presented in this paper. Each multilevel inverter configuration presented in this paper is explained by the corresponding schematic diagram, operating principle, and simulation results**

Keywords — H-bridge, multilevel inverter, symmetrical DC-sources, asymmetrical H bridge topology.

I. INTRODUCTION

The power conversion from DC to AC plays a key role in modern system in generation, distribution, transmission, and utilization of an electric power. These are used in various applications such as induction heating, power supply, air conditioning, transmission of HVDC power, active filter, electric drives, uninterruptible power supply [1, 2]. Earlier, multilevel inverters were used in low power applications [3] but recently, requirement of higher power apparatus in different industries has reached a megawatt level. It is difficult to bond a single power device directly to low and medium voltage grid (2.3 kV, 3.3 kV, 4.16 kV, or 6.9 kV) that has received an increasing attention in recent years as an alternative in high power and medium or high-voltage situation [4-7]. Multilevel inverter has a potential to generate output voltage waveform at a reduced switching frequency with less harmonic distortion if low voltage ratings using devices are used which make them a better choice for medium and high-voltage power applications [8-10]. Various power quality improvement techniques are reported in [11-23].

[1]This paper proposed a new controller using embedded function coding to produce the gate pulses for different switching topologies of multilevel inverter. This new scheme can be implemented digitally using DSP controller. The various single phase cascaded H bridge multilevel inverter systems (3, 5 and 17 level) based on the proposed control algorithm is simulated on the MATLAB platform and there results were also discussed in this paper. On increasing the number of levels in the output-voltage number of components also increases. So to reduce the components DC-sources of different magnitudes are used to implement 17-level inverter on the MATLAB/Simulink platform. Total harmonic distortion in output current of various simulated multilevel inverter system were compared in this paper under RL load.

II. SYSTEM CONFIGURATION AND OPERATING PRINCIPLE

M-level multilevel inverter using H bridge topology consists of (M - 1)/2 number of single phase H-bridge cells, each having individual DC source. Total amplitude of voltage in the output is equal to the sum of synthesized voltage of each H bridge cell individually. Each H bridge cell produces three output voltages $+V_{dc}$, 0, and $-V_{dc}$. It can synthesize output voltage waveform that approaches sinusoidal shape. Fig. 1 shows the schematic diagram of three-level cascaded H bridge multi-level inverter. It consists of single H bridge cell that has four power switching devices (s_1, s_2, s_3 and s_4) and a single DC-source.

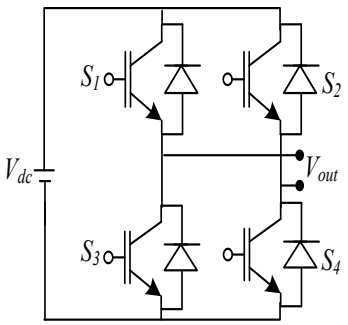

Fig. 1 Schematic diagram of single phase 3-level inverter

For the output-voltage $v_0 = +V_{dc}$ switches s_1 and s_4 should be turned ON. Either switch (s_1, s_2) or (s_3, s_4) should be turned ON for output-voltage $v_0 = 0$. For output-voltage $v_0 = -V_{dc}$ s_2 and s_3 should be turned ON. The output-voltage generated consists of three-levels. Table I shows the switching of devices for 3-level inverter.

TABLE I
SWITCHING SEQUENCE FOR THREE-LEVEL INVERTER

Output Voltage level	Switches to be turned ON
$+V_{dc}$	s_1, s_4
0	s_1, s_2 or s_3, s_4
$-V_{dc}$	s_2, s_3

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The schematic diagram of single phase 5-level cascaded H bridge multilevel inverter is shown in Fig. 2. It consists of 2 H bridge cell that has 8 switching devices (s_1, s_2, s_3, s_4, s_5, s_6, s_7, and s_8) and two DC-sources of equal magnitude. This inverter system generates five levels in the output voltage ($+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$,). Switching states to produce the five steps in the output voltage is explained in Table II. These states are fed to the gate terminal of the switching devices.

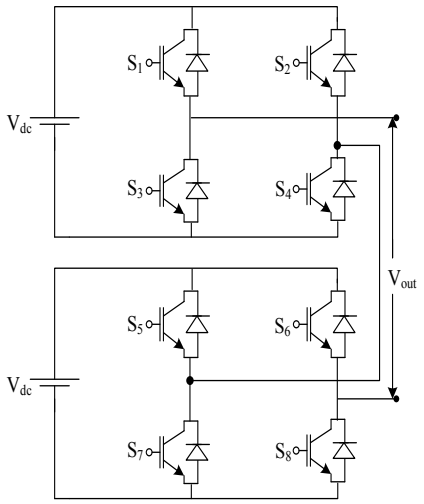

Fig. 2 Schematic diagram of single phase 5-level inverter

TABLE II
SWITCHING SEQUENCE FOR FIVE-LEVEL INVERTER

Output Voltage	Switches to be turned ON
$+2V_{dc}$	s_1, s_4, s_5, s_8
$+V_{dc}$	(s_1, s_4, s_5, s_6) OR (s_1, s_2, s_5, s_8)
0	(s_1, s_2, s_5, s_6) OR (s_1, s_2, s_7, s_8)
$-V_{dc}$	(s_2, s_3, s_5, s_6) OR (s_1, s_2, s_6, s_7)
$-2V_{dc}$	s_2, s_3, s_6, s_7

Similarly, on increasing the number of H bridge cells in the inverter system number of steps in the output AC voltage can be increased. According to this topology higher level such as seventeen-level uses eight H-bridge cell, i.e., it requires large number of DC sources and power devices. To reduce the components used in higher levels cascaded H-bridge topology can be modified. DC-source of each H-bridge cells should be of different magnitude. This modified topology reduces the part counts on increasing the steps in the output AC voltage. Fig. 3 shows the asymmetric arrangement of DC- sources producing seventeen-level in the output-voltage. It consists of 12 switching devices (S_1 to S_{12}) and 3 DC-sources of different magnitude (V_{dc}, $3V_{dc}$, and $9V_{dc}$) which is much lesser than symmetrical arrangement of seventeen-level inverter system. Switching sequences is explained in Table III.
According to the switching states seventeen-level can be obtained in output voltage.

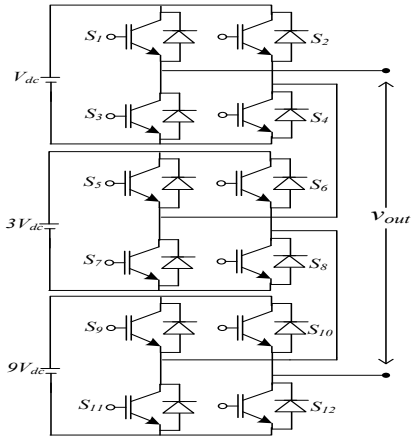

Fig. 3 Schematic diagram of single phase 17-level inverter

TABLE III
SWITCHING SEQUENCE FOR SEVENTEEN-LEVEL INVERTER

Output voltage levels	Switches to be turned ON
$+8V_{dc}$	s_2, s_3, s_5, s_6, s_9, s_{12}
$+7V_{dc}$	s_1, s_4, s_6, s_7, s_9, s_{12}
$+6V_{dc}$	s_1, s_2, s_6, s_7, s_9, s_{12}
$+5V_{dc}$	s_2, s_3, s_6, s_7, s_9, s_{12}
$+4V_{dc}$	s_1, s_4, s_5, s_8, s_9, s_{10}
$+3V_{dc}$	s_1, s_2, s_5, s_8, s_9, s_{10}
$+2V_{dc}$	s_2, s_3, s_5, s_8, s_9, s_{10}
$+V_{dc}$	s_1, s_4, s_5, s_6, s_9, s_{10}
0	s_1, s_2, s_5, s_6, s_9, s_{10}
$-V_{dc}$	s_2, s_3, s_5, s_6, s_9, s_{10}
$-2V_{dc}$	s_1, s_4, s_6, s_7, s_9, s_{10}
$-3V_{dc}$	s_1, s_2, s_6, s_7, s_9, s_{10}
$-4V_{dc}$	s_2, s_3, s_6, s_7, s_9, s_{10}
$-5V_{dc}$	s_1, s_4, s_5, s_8, s_{10}, s_{11}
$-6V_{dc}$	s_1, s_2, s_5, s_8, s_{10}, s_{11}
$-7V_{dc}$	s_2, s_3, s_5, s_8, s_{10}, s_{11}
$-8V_{dc}$	s_1, s_4, s_5, s_6, s_{10}, s_{11}

III. CONTROL ALGORITHM FOR MULTILEVEL INVERTER

This section presents the proposed scheme for controlling the gating signals fed to gate terminals of the power semiconductor devices used in multilevel inverter to get the desired output voltage. The block diagram of the proposed scheme is shown in Fig. 4. This block diagram includes a gating signal generator which is the main controlling unit. Pulses fed to different switches are generated through this unit using an embedded code. Multilevel inverter generates the desired output in response to the gating signal received. This unit consists any of the multilevel inverter structure mentioned above. And the output waveforms can be seen through any of the displaying unit. These embedded code can directly loaded to any microcontroller or DSP controller for real time implementation.

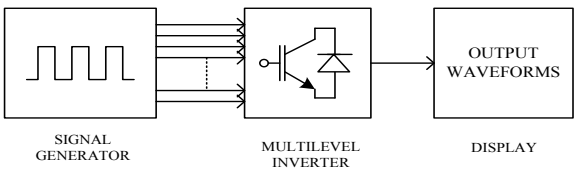

Fig. 4 Block diagram of the proposed scheme

A simple coding has been done to produce 3-level, 5-level and 17-level inverter with the help of an embedded function

on MATLAB. Fig. 5 shows the flow chart describing the coding sequence for the three-level cascaded H bridge multilevel inverter.

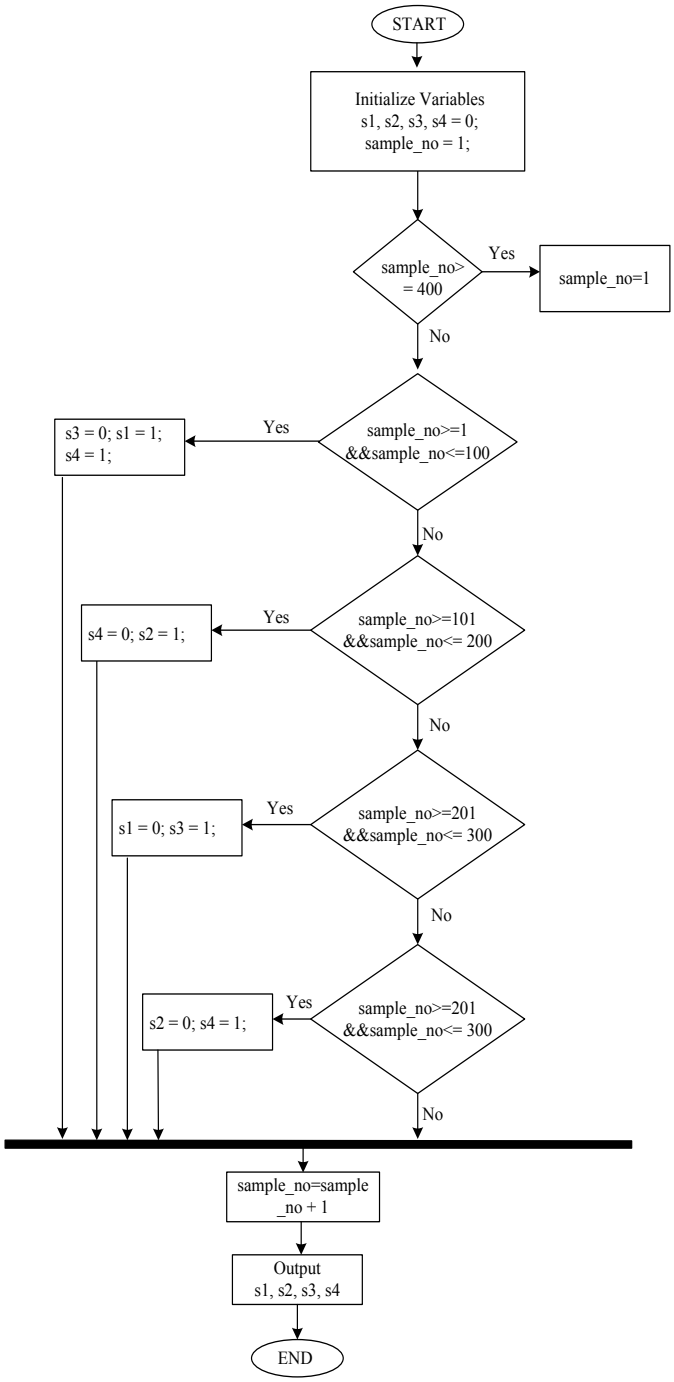

Fig. 5 Flow chart for generating the gating signals for three-level multilevel inverter

Embedded coding has been done on the basis of the switching sequence explained in section II for different levels in the output voltage. At starting different variables (switches and sample number) are initialized. Total number of samples in one period is 400. So, for 3-level inverter there will be 4 intervals. Each interval will have 100 samples. For five-level there are 8 intervals and each will have 50 samples. For seventeen-level there are 32 intervals and each interval will have 12.5 samples in each interval. According to these intervals switching states are generated. Now, the first condition is checked if sample is greater than or equal to 400. If the condition is not found true than it will check second condition if it is found true then switches s_1 and s_4 have to be turned ON and the sample number is incremented generating the output pulses, else it will check the third condition. In this way when all the conditions are checked and the sample number reaches 400, then first condition will hold true that will make the sample number again to 1 and the process is repeated for the next cycle. To implement 5-level and 17-level cascaded H bridge multilevel inverter coding can be done in the similar manner as explained for the three-level inverter.

IV. RESULTS AND DISCUSSION

The MATALB/Simulink models of different multilevel inverter system using the proposed embedded controller are presented in this section and their results are also discussed in this section. Fig. 6(a) shows MATLAB model of single-phase three-level cascaded H-bridge multilevel inverter. DC-source voltage is equal to 250 V for three-level inverter and it is simulated under RL load. Embedded MATLAB function block is used to write the coding for generating the gate pulses.

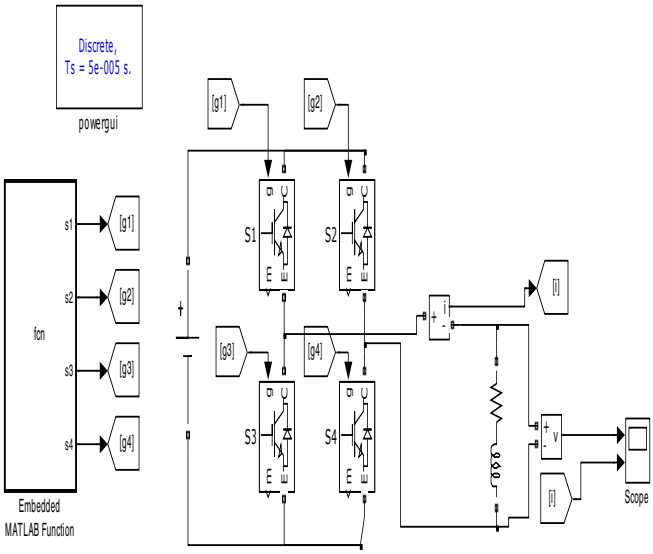

Fig. 6 (a) Single phase 3-level cascaded H bridge multilevel inverter

For 3-level inverter there will be 4 output gate signals from this block. Fig. 6(b) shows MATLAB model of single phase five-level cascaded H bridge multilevel inverter. Each DC source voltage is equal to 115 V for 5-level inverter and it is simulated under RL load. There are 8 output gate signals from embedded function block for 5-level inverter system. Fig. 6(c) shows MATLAB model of single phase 17-level cascaded H bridge multilevel inverter. DC-source voltage for each level is equal to 28.75 V for seventeen-level inverter and it is simulated under RL- load. For seventeen-level there are 12 output gate signals from embedded function block.

the output-voltage waveform of developed 3-level inverter system is shown Fig. 7(a), whereas Fig. 7(b) and 7(c) demonstrate the output-voltage waveforms of 5-level and 17-level inverter system respectively.

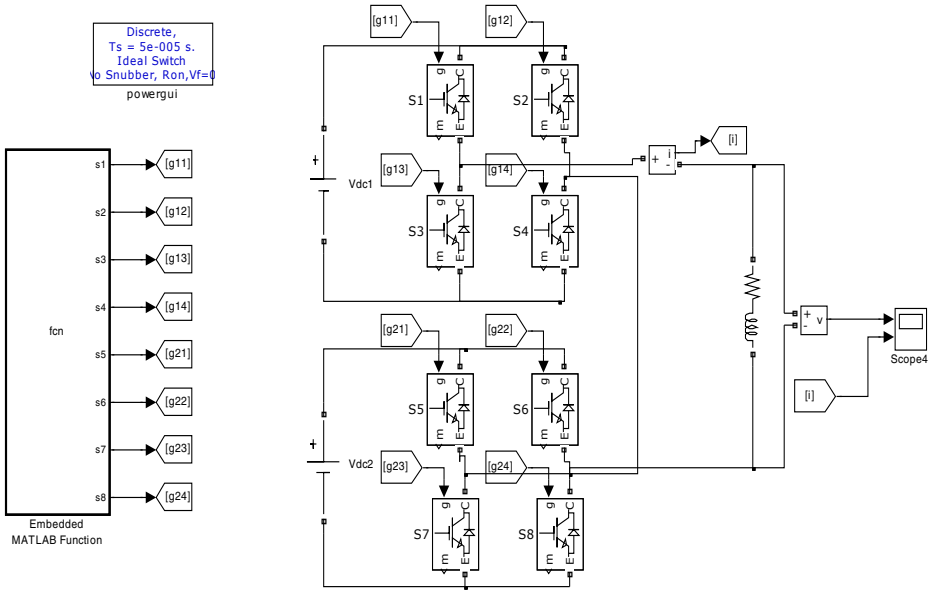

Fig. 6 (b) Single phase 5-level cascaded H bridge multilevel inverter

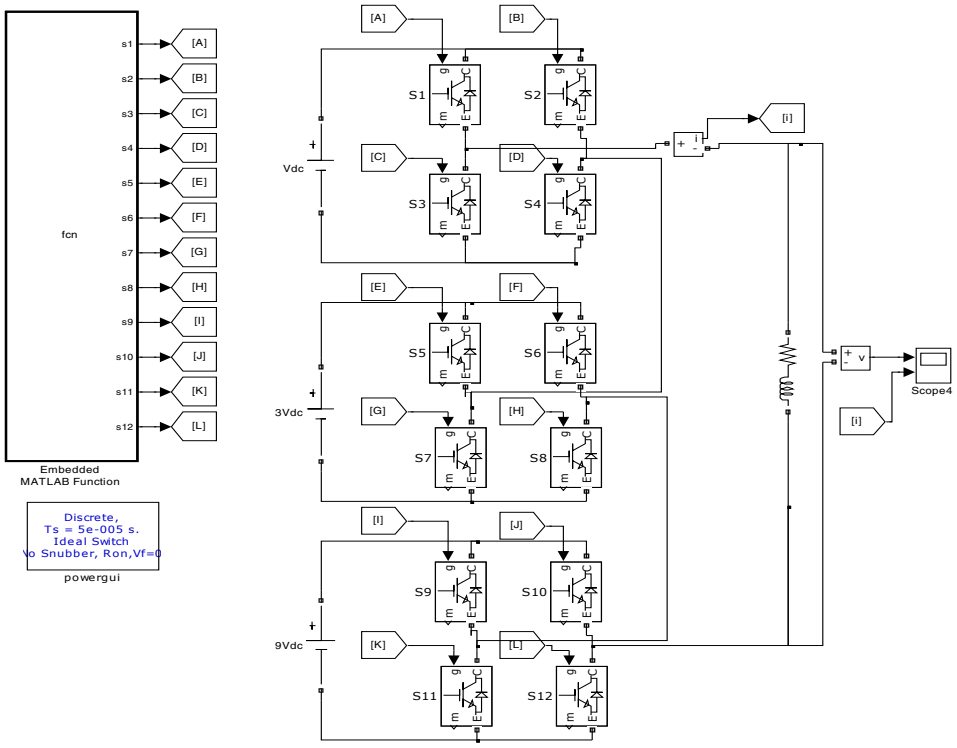

Fig. 6 (c) Single phase 17-level cascaded H bridge multilevel inverter

It can be seen from Figs. 7(a) to 7(c) that the waveform of the AC output-voltage for the developed inverter system is improved significantly from 3-level to 17-level. The waveform becomes more sinusoidal as we increase the steps in the output voltage. Fig. 7(d) shows the THD in output-voltage of the 3-level cascaded H bridge multilevel inverter system is 46.41%. The THD in output voltage further reduces to 27.36% when the level in the output voltage reaches 5. Fig. 7(e) shows the harmonic spectrum of output-voltage of 5-level cascaded H bridge multilevel inverter system and the harmonic spectrum of output-voltage of 17-level inverter system that indicate 13.18% THD in output-voltage is shown in Fig. 7(f). It shows that on increasing the levels in the output-voltage decreases the THD in the output-voltage which improves the power quality. The fundamental voltages of three, 5 and 17-level are found to be 225.9 V, 233.4 V and 227.2 V respectively which is near to ideal AC voltage 230 V.

Fig. 7(g) shows the output-current waveform of cascaded H bridge 3-level inverter system, whereas Fig. 7(h) and 7(i) shows the output-current waveforms of 5-level and 17-level inverter system respectively. It can be seen from Figs. 7(g) to 7(i) that the current waveform of the developed inverter system becomes more sinusoidal from 3-level to 17-level as the level in the output-voltage is increased. Fig. 7(j) shows the THD in output-current of the 3-level cascaded H bridge multilevel inverter system is 22.71%. The THD in output-current further reduces to 10.52% and 7.30% when the level in the output voltage is increased to five and seventeen steps respectively as shown in Fig. 7(k) and Fig. 7(l). The fundamental current is almost equal to 40 A.

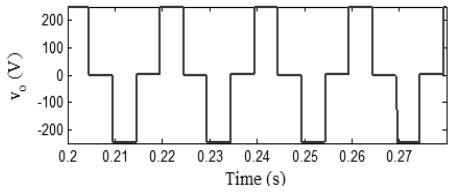

Fig. 7(a) Output voltage waveform of single-phase three-level cascaded H-bridge multilevel inverter

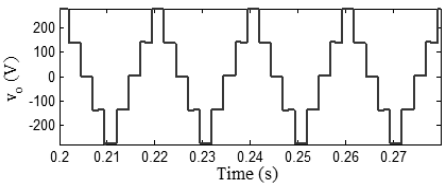

Fig. 7(b) Output voltage waveform of single-phase five-level cascaded H-bridge multilevel inverter

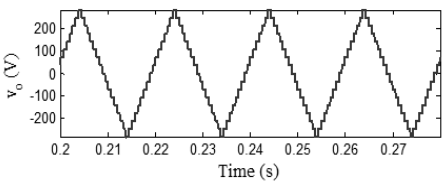

Fig. 7(c) Output voltage waveform of single-phase seventeen-level cascaded H-bridge multilevel inverter

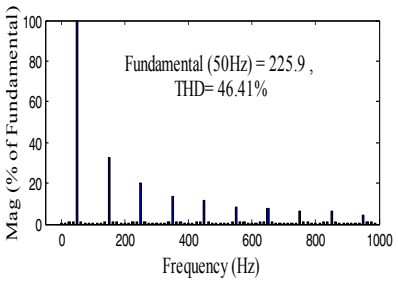

Fig. 7(d) Harmonic spectrum of THD of output-voltage of 3-level inverter

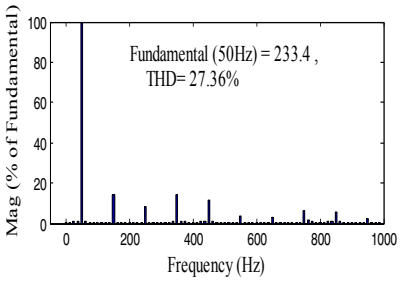

Fig. 7(e) Harmonic spectrum of THD of output-voltage of 5-level inverter

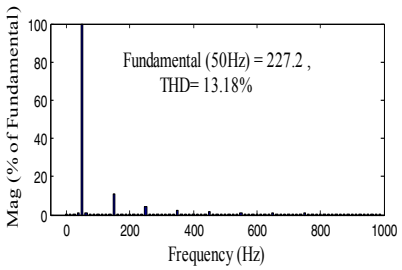

Fig. 7(f) Harmonic spectrum of THD of output-voltage of 17-level inverter

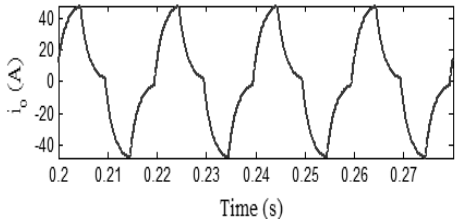

Fig. 7(g) Output-current waveform of single phase 3-level cascaded H bridge multilevel inverter

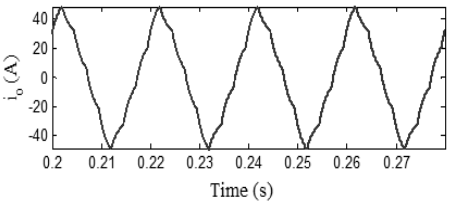

Fig. 7(h) Output- current waveform of single phase 5-level cascaded H bridge multilevel inverter

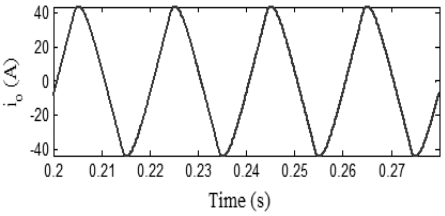

Fig. 7(i) Output-current waveform of single phase 17-level cascaded H bridge multilevel inverter

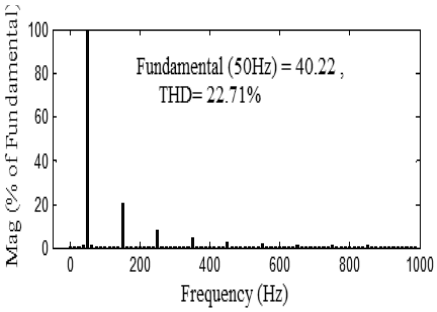

Fig. 7(j) Harmonic spectrum of THD of output-current of 3-level inverter

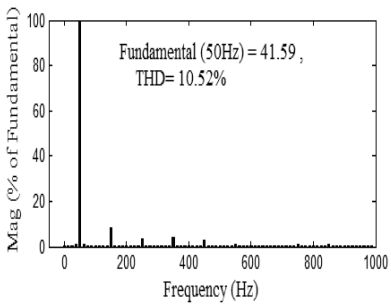

Fig. 7(k) Harmonic spectrum of THD of output-current of 5-level inverter

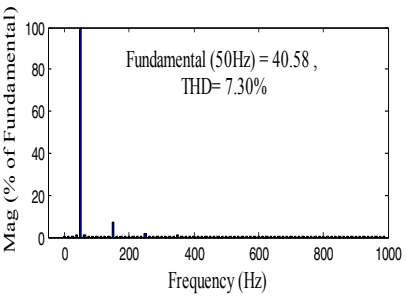

Fig. 7(l) Harmonic spectrum of THD of output-current of 17-level inverter

V. CONCLUSIONS

The implementation of the proposed embedded controller has been successfully presented in this paper for different multilevel inverter system. The results of the simulation of 3-level, 5-level, and seventeen-level inverter using the embedded function on MATLAB platform prove that the proposed scheme can be used to develop multilevel inverter system of any level number in the output-voltage. It can also be concluded that on increasing the steps in the output-voltage value of THD decreases that improves the power quality and the waveform near to sinusoidal waveform can be achieved easily using the proposed scheme.

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