AC690N Series Hardware Design Guide V1.3

Special Precautions:

1. The main control input voltage should not exceed 5.0V.

2. The AC690N series Bluetooth crystal oscillator can omit the capacitor, but the position must be reserved. 3. For speakers or headphones with an internal soft power-on/off scheme, please use the PR2 pin to wake up with a low level.

4. For schemes with particularly low power consumption requirements during soft shutdown, please use an external MOSFET switch circuit. Please refer to the attachment 'MOSFET Soft Power-On/Off Circuit'. 5. For customers with high FM requirements, please reserve an FM amplification circuit in the circuit design or use an external radio chip. For FM design and debugging, please refer to 'AC690N Series FM PCB Layout Instructions'.

6. For schemes using internal charging, a current-limiting resistor must be connected in series with the charging input terminal. 7. To ensure the safety and reliability of the product, please use a battery with a protection board.

<Note: LDO solutions are generally used for Bluetooth speaker products; DC-DC solutions are generally used for Bluetooth headphone products>

1. Power and Ground

1. Ground

LDO solution:

1) The AC690N (LDO) scheme must separate AGND and GND into two grounds, with AGND connected to the amplifier or battery and shorted to GND,

2) FMVSS does not separate grounds, connect to digital GND nearby.

DC-DC scheme:

1) The AC690N (DC-DC) scheme must separate AGND and GND into two grounds, and they must be shorted at the battery entry; priority must be given to ensuring the connectivity of the ground return loop to avoid overly thin routing of the loop.
2) PGND does not separate grounds and should be connected close to digital GND.

Note: This requirement must be strictly followed to eliminate various noises caused by common ground.

2. BT_AVDD

For the LDO scheme, the decoupling capacitor value for BT_AVDD must be at least 10μF, and it must be placed close to the main control unit, with the ground return path being as short as possible to the main control unit.

3. DC-DC Switching Power Supply

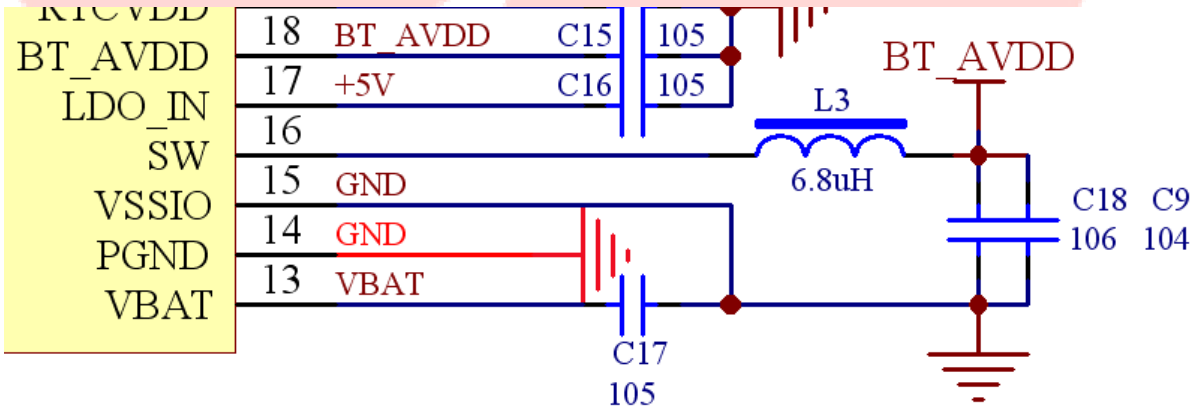

Figure 1 DC-DC Switching Power Supply Circuit

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As shown in Figure 1, the DC-DC switching power supply consists of SW, PGND, BT_AVDD, VBAT, and L3, C18, C9, C15 (red part); during layout, L3/C18/C9/C15 should be placed as close as possible to the corresponding pins; the routing of L3's BT_AVDD must first go through the C18 (106) capacitor before entering the main control; L3 should be kept as far away as possible from parts that are easily interfered with (such as RF, DAC); please choose a wire-wound inductor or power multilayer inductor for L3, with a rated circuit greater than 120mA and an internal resistance of less than 0.5R.

4. FMVDD/ VDDIO

1) The decoupling capacitor for AC6901A's FMVDD must be placed close to the main control, and the ground return loop should be as short as possible back to the main control FMVSS pin.

2) For chips other than AC6901A, the decoupling capacitor for VDDIO must be placed close to the main control unit, and the ground return path should be as short as possible back to the main control unit.

Note: If the ground return path of this decoupling capacitor is poorly routed, it directly affects the performance of Bluetooth.

II. Signal Lines

1. Crystal Oscillator

1) The AC690N scheme must reserve positions for the crystal oscillator matching capacitors, with the capacitor value being NC; each scheme or prototype must be tested for frequency deviation using a test box, with the frequency deviation controlled within ±10KHz. If the deviation is too large, software or load capacitance can be modified.

2) The crystal oscillator must be selected for good stability and consistency, with a frequency deviation of within ±10PPM; (it is recommended to use the crystal oscillator that comes with the Jieli package).

2. RF Antenna

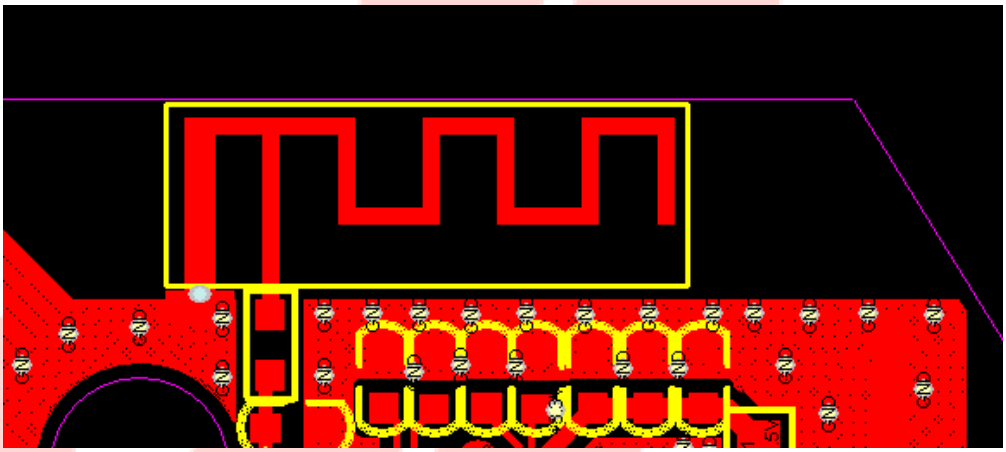

Figure 2 RF antenna layout

1) The RF antenna should preferably use an inverted F shape, as shown in Figure 2.

2) The RF antenna must be placed at the edge of the board, strictly prohibited from being wrapped by GND, and there must be no metallic components on both sides. A three-sided hollow design (top, left, right) should be adopted, as shown in Figure 2.

3) The RF antenna should preferably use an I-shaped routing.

DC-DC scheme:

4) The RF antenna and DAC circuit should preferably adopt a 180-degree layout to minimize RF interference with the DAC.

3. DACL, DACR, VCOMO DC-DC

Solutions:

1) The anti-interference circuits and solder joints of DACL, DACR, and VCOMO should be placed as far as possible at 180 degrees from the RF antenna to reduce RF radiation interference.

2) The anti-interference circuits and solder joints of DACL, DACR, and VCOMO should have AGND laid on both sides, or not laid at all, and must not use 'digital GND'. They should also be kept away from 'digital GND' to effectively eliminate high-frequency noise.

Three, Others

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1. RF antenna and TDD radiation noise

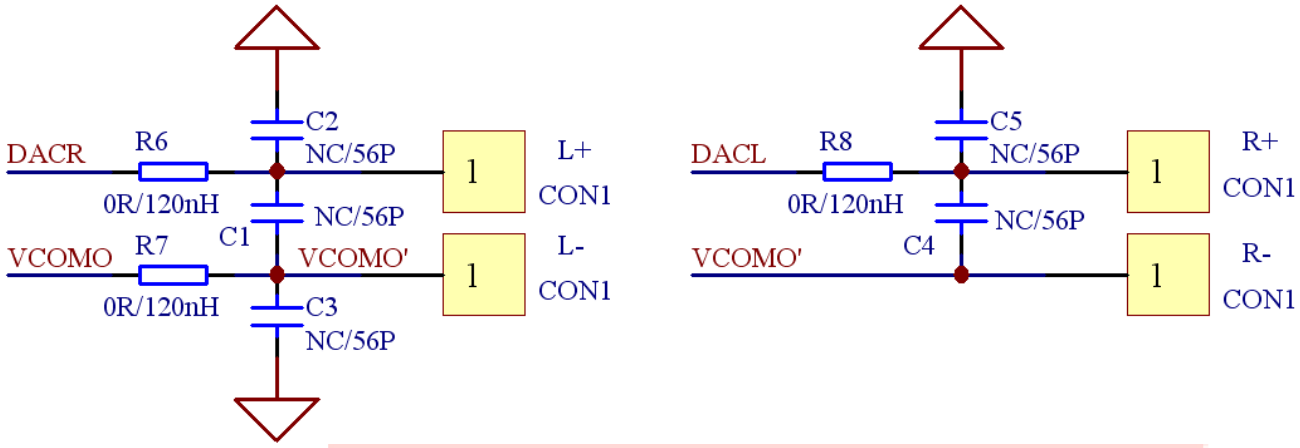

Figure 3 DAC suppression RF antenna interference circuit

DC-DC scheme:

1) Figure 3 is the circuit for DAC suppression of RF antenna interference and TDD interference, it is recommended to reserve; if space is limited, only R6/R7/R8 can be reserved.

2) The leads of the DAC, power supply, and speaker cavity should avoid the position of the RF antenna; the connection points for the speaker and battery are best located at the reverse side of the RF antenna.

180 .

3) R6 and R8 should use 100nH or 120nH to effectively eliminate high-frequency TDD noise generated when the phone is close to the prototype during Bluetooth calls; R7 should use 220nH or 330nH to effectively eliminate high-frequency noise during music playback (if the layout is unreasonable, this method can be tried to eliminate it).

(Note: The reserved noise processing circuit at the DAC end will increase costs. If the design of the scheme is reasonable and the noise requirements are not strict, it can be omitted.)

2. ESD Static Electricity

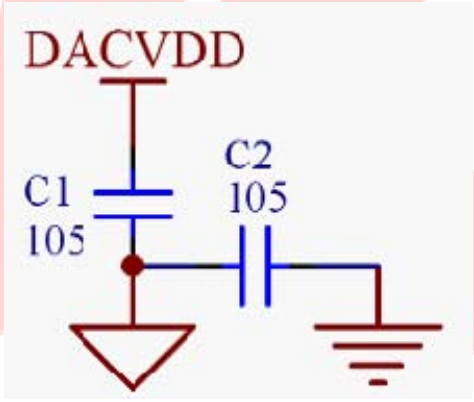

Figure 4 ESD Static Electricity Processing Circuit

1) At the decoupling capacitor C1 of the DACVDD power supply, connect AGND and GND nearby using a 105 capacitor, as shown in Figure 4.

2) The routing of the analog parts such as DACL and DACR, along with related components, is susceptible to electrostatic interference, so protection is important. (Consider increasing the spacing from GND and not placing GND under the components, etc.)

(Note: ESD handling will increase material costs; if the design does not require this, it can be disregarded.)

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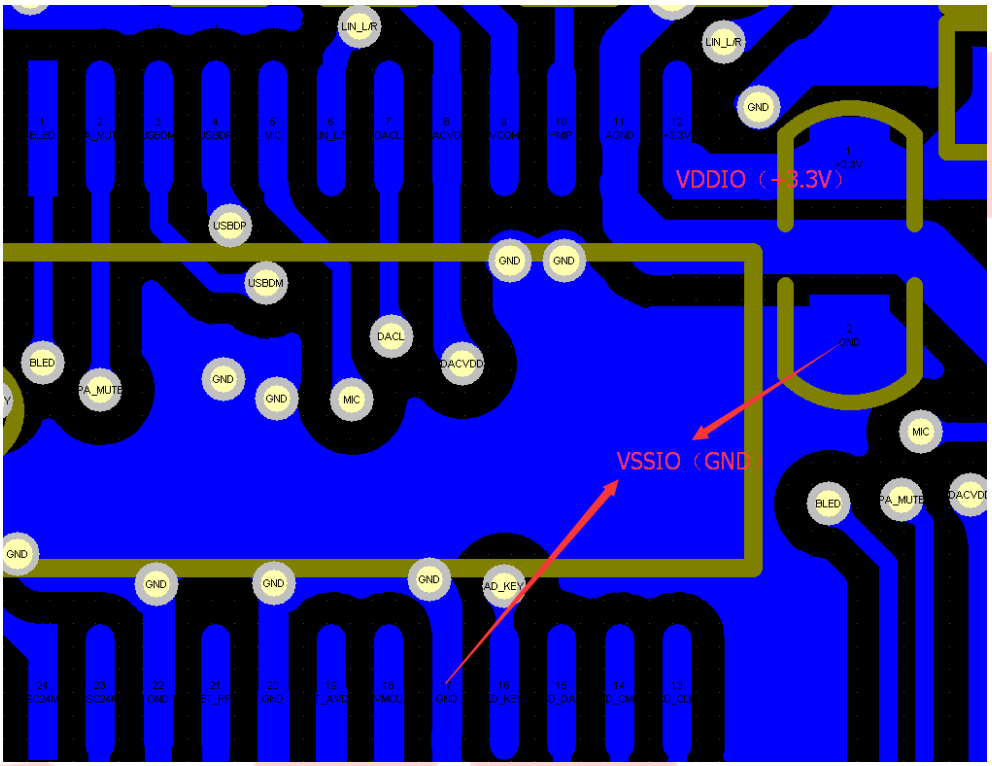
3. When designing chips with QFN packaging, please reserve programming test points.

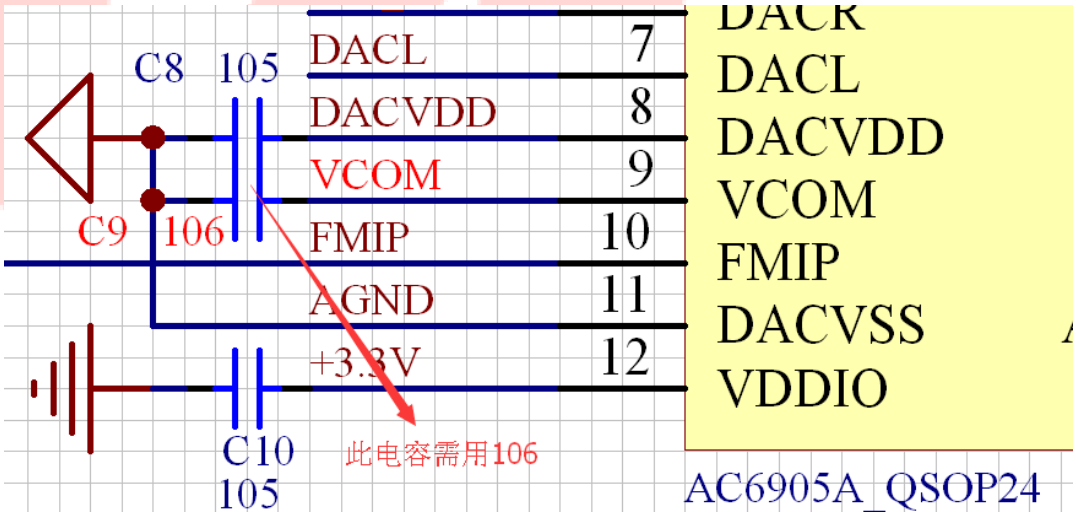
Given that QFN packaged chips are relatively small, making it difficult for programming stations or manual programming, it is advisable to first mount the chips and then program them using a PC. However, the following programming points must be reserved during the design: VBAT, GND, DP, DM. (Note: It is essential to ensure that the voltage supplied to VBAT is +5V.)

4. The decoupling capacitor for VDDIO (+3.3V) must have the shortest return path to the chip's VSSIO (GND) pin.

The ground return path for the VDDIO power supply is the VSSIO (GND) pin. During the design process, it is necessary to ensure a large area with the shortest distance back to VSSIO. Refer to the design as shown in the figure:



5. The ADKEY reuse LED lighting application requires changing the VCOM capacitor to 106; for non-reuse schemes, 105 should still be used.



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IV. Version Information

Date	Version Number	Description
2016.10.11	V1.0	Original Version
October 18, 2016	V1.1	The special notes section has been updated to include points 5, 6, and 7 regarding the FVVSS and PGND grounding point descriptions.
November 18, 2016	V1.2	Update points: 1. Update the shape of the Bluetooth antenna 2. Please reserve a programming point for the QFN package 3. The decoupling capacitor for VDDIO must return to VSSIO over a large area and in the shortest path. 4. The ADKEY multiplexing LED scheme requires the VCOM capacitor to be increased to 106.
December 22, 2016	V1.3	Update points: 1. Once again, emphasize the capacitance value of BT_AVDD; for designs without a DC-DC solution, at least a 106 (0603 package) must be used.

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