AC695N, AC696N Hardware Design Guide **V1.0**

special attention items:

1. The VBAT power pin input voltage should not exceed **5.0V.**

2. The LDO_IN charging input voltage cannot exceed **5.5V.**

3. LDO_IN must reserve a capacitor to ground.

4. For speakers or headphones with internal soft power on/off solution, please use **PB1** port low level to wake up the power on/off button.

5. To ensure the safety and reliability of the product, please use batteries with protection boards.

6. **The test points must be pulled out when burning IO (VMCU, USBDM, USBDP, VDDIO, VSSIO).**

1. Version Information

date	version number	describe
2020.6.11	V1.0	Original version

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Table of contents

AC695N, AC696N Hardware Design Manual V1.0.....1 1.
Circuit Design Guidelines.....3
1.1 Crystal Oscillator Selection Instructions.....3
1.2 DCDC Selection and Circuit Description.....3
1.3 LDO_IN Charging Circuit Description.....3
1.4 DAC Anti-interference Circuit Description.....4
1.5 MIC Circuit Description.....5
1.6 ESD Circuit Description.....5
2. PCB Layout Design Guidelines.....6 2.1
Crystal Oscillator Design Guidelines.....6
2.2 DCDC Design Guidelines.....6
2.3 Audio Signal Line and AGND Design Guidelines.....6
2.4 FM Design Guidelines.....
6 3. Other Notes.....
6 3.1 About Bluetooth Headset Assembly Requirements..... 6
3.2 About LDOIN Charging Issues..... 7
Appendix 1: Crystal Oscillator Module Layout Notes.....8
Appendix 2: DCDC Module Layout Notes.....8
Appendix 3: Audio Signal Line and AGND Layout Notes.....10
Appendix 4: FM Module Layout Notes.....10

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1. Circuit Design Guidelines

1.1 Crystal Oscillator Selection Instructions

Since Bluetooth has high requirements for frequency deviation, the quality of the crystal oscillator is crucial to the performance of Bluetooth.

The frequency deviation of the crystal oscillator must be ÿ±10ppm, and the load CL is recommended to be 12pF.

brand	Capacitance to ground	model	Frequency Deviation
Daming Electronics reserves 24M ground capacitor position (CL=12pF)			±20K

Recommended manufacturer: Yantai Daming Electronics. If you use crystal oscillators from other manufacturers, you must test and verify them.

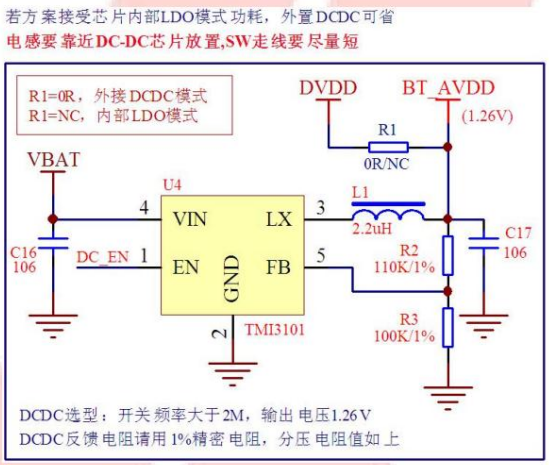
1.2 DCDC selection and circuit description

ÿ If the solution accepts the power consumption of the chip's internal LDO mode, external DCDC can be saved.

ÿ DCDC chip selection: The switching frequency is required to be greater than 2M and the output voltage is 1.26V. Recommended model: TMI3101

ÿ Please use 1% precision resistors for DCDC feedback resistors R2 and R3.

The schematic diagram is as follows:



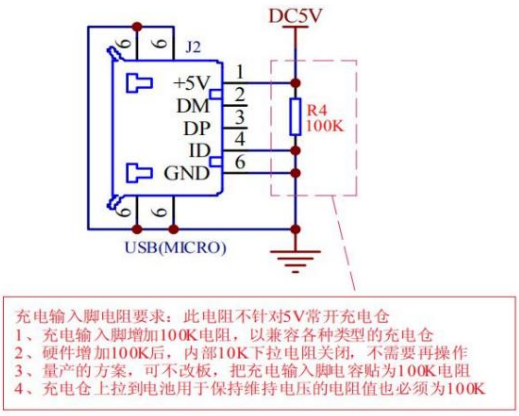
1.3 LDO_IN charging circuit description

AC695N and AC696N have built-in charging modules, and the design requirements are as follows:

1 TWS headset model

1) The charging input pin requires the addition of a 100K resistor to be compatible with various types of charging compartments;

[Note: This resistor is not for the 5V normally open charging compartment], as shown in the figure below.



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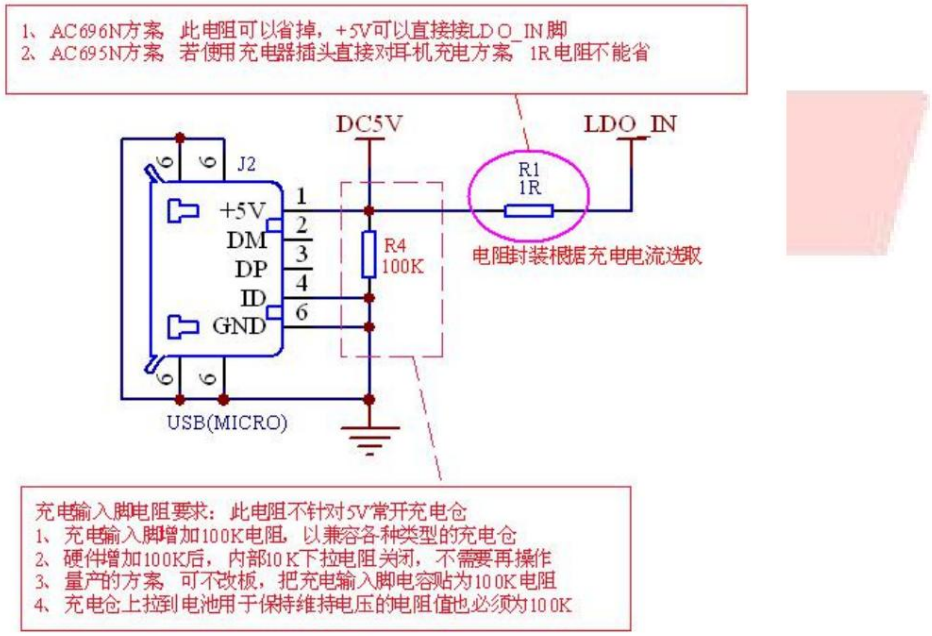
2) If you use a charger plug or external DC power supply to charge the **AC695N** TWS solution,

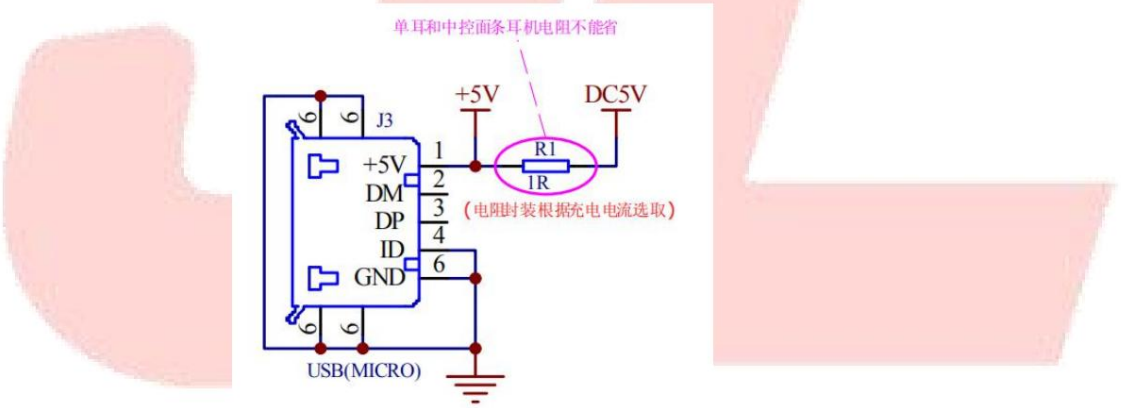
the LDO_IN charging input terminal must be connected in series with a current limiting resistor 1R, as shown in the figure below. [Note: For the AC695N solution, this requirement is not required if it is only equipped with a charging bin] **[Note: For the AC696N solution, this requirement is not required]**



2 single ear/noodle earphones

For the AC695N single-ear/noodle headset solution, the charging input pin must be connected in series with a current-limiting resistor of 1R, as shown in the figure below.

[Note: AC696N solution does not have this requirement]



1.4 DAC Anti-interference Circuit Description

AC695N and AC696N support DACL/DACR differential mode and DACL/DACR/VCOMO stereo mode. The schematic diagram is as follows:

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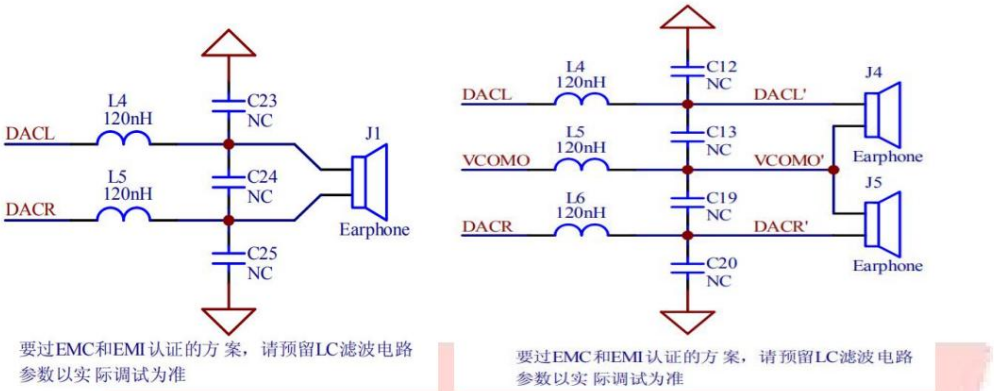


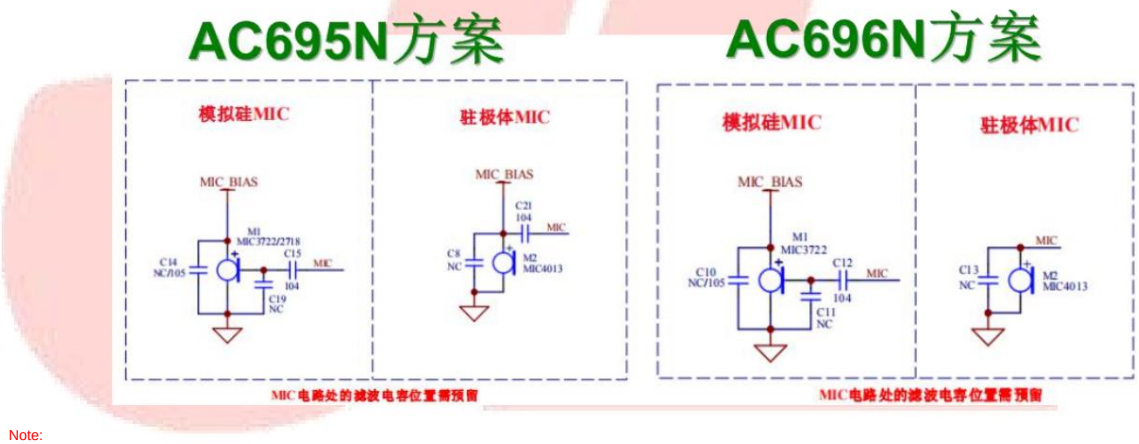
1) It is recommended to reserve anti-interference circuit for the DAC part; if space is limited, only L4/L5/L6 can be reserved.

2) If the noise requirement is strict, it is recommended to lay AGND on the front and back sides of the DAC circuit and welding points, or not lay ground, and never lay "digital GND", and stay away from "digital GND", which can effectively remove high-frequency noise.

3) L4/L5 is fixed at 100nH or 120nH, which can effectively remove the high-frequency TDD noise generated when the mobile phone is close to the prototype during Bluetooth calls; L6 uses 220nH or 330nH, which can effectively remove high-frequency noise when playing songs (if LAYOUT is unreasonable, you can try this method to remove it). Note: The noise processing circuit reserved at the DAC end will increase the cost. If the solution design is reasonable enough and the noise requirement is not high, it can be No reservation

1.5 MIC Circuit Description

AC695N and AC696N support two modes: analog silicon MIC and electret MIC. The schematic diagram is as follows:



Note:

For the electret MIC solution, AC695N requires a DC-blocking capacitor at the MIC input. This must be distinguished from AC696N during design.

1.6 ESD Circuit Description

ÿ The routing of analog parts such as DACL, DACR, and related components are easily disturbed by static electricity, so pay attention to protection (you can increase the distance between GND and spacing, no GND under components, etc.)

ÿ At the decoupling capacitor C1 of the DACVDD power supply, it is recommended to reserve C2:105 capacitor nearby to connect AGND and GND (if The scheme design is reasonable enough and no reservation is required) The schematic diagram is as follows:

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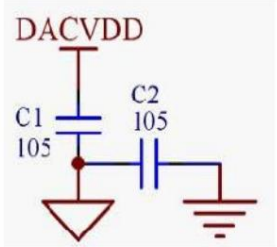

2.PCB Layout Design Guide The following points

should be noted in **PCB Layout** design:

1) All decoupling capacitors on the main control chip must be placed as close to the chip pins as possible, and the decoupling capacitor-to-ground loop must be as short as possible.

2) Prioritize the placement of the Bluetooth antenna and place the RF antenna as close to the edge of the board as possible.

3) The FM antenna matching network should be placed as close to the chip pins as possible, and the antenna routing should be kept away from interference sources (such as LCD/LED screen data lines)

4) The 24M crystal oscillator must be placed close to the chip's clock pins (BTOSCO and BTOSCI). The 24M crystal oscillator wiring must be grounded in a three-dimensional manner, away from

Avoid routing the cable in parallel with other data lines to avoid interference.

5) When routing audio signals such as DACL, DACR, AUXL, AUXR, and MIC, be careful to stay away from digital signals (LCD/LED signals, USB,

SD, etc.)

For specific module design guidelines, please refer to the following:

2.1 Crystal Oscillator Design Guide

Refer to Appendix 1: Crystal oscillator module layout considerations.

2.2 DCDC Design Guidelines

Refer to Appendix 2: DCDC module layout considerations.

2.3 Design Guidelines for Audio Signal Lines and **AGND**

Refer to Appendix 3: Layout considerations for speaker audio signal lines and AGND.

2.4 FM Design Guidelines

Refer to Appendix 4: FM module layout considerations.

3. Other instructions

3.1 About the Bluetooth headset assembly requirements

The impact of assembly on Bluetooth performance cannot be ignored. It may introduce noise and degradation in distance. The following optimizations are recommended: 1)

The Bluetooth antenna or DCDC chip should be structurally away from the speaker, speaker cable, and MIC device. 2) It is recommended to use

sponge glue to pad the battery and try to increase the distance from the antenna RF; the height and position of the sponge glue pad should be uniform. 3) The touch copper

foil should be uniformly positioned during assembly and try to avoid the antenna. 4) The speaker and battery

cables should be twisted into pairs and placed away from the antenna and DCDC chip.

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3.2 Explanation of **LDOIN** charging issues

1. Key configuration items (in board.c), set different values according to different charging compartments, as shown in Table ÿ:

ldo5v_off_filter

ÿÿldo5v_pulldown_en

ÿÿint eSystemConfirmStopStatus(void);

Charging compartment type	Charging compartment description	ÿ	ÿ	ÿ	Hardware circuit requirements
Type 1	5V normally open charging case	------	0	Comment out this function	No need to add LDOIN 100K resistance to ground
Type 2	Automatic boost charging station	Filter time according to actual warehouse configuration	0	Keep this function	The LDOIN needs to increase 100K resistance to ground
Type 3	The button boost with pull-up resistor provides a charging compartment that maintains the voltage. Other	Filter time according to actual warehouse configuration	0	Keep this function	The LDOIN needs to increase 100K resistance to ground

types of charging compartments will be analyzed separately.

2. AC695N, AC696N charging hardware circuit adjustment:

1. The headphone charging pin LDOIN hardware reserves a resistor to ground to prevent the need to change the board when adding materials later.

2. For charging case type 3, the case output maintains the maintenance voltage. After the earphones are placed in the case, the LDOIN voltage should be maintained at 1~2V, the pull-up resistor of the charging case should be changed to 100K, and the LDOIN at the earphone end should be increased with a pull-down resistor of 100K.

3. Common charging problems of AC695N and AC696N, the solutions are as follows:

Question 1: For Type 2 charging case, charge it in a loop after it is fully charged

Cause: The filtering time was set too small, causing the program to judge that the warehouse was out and mistakenly open the 10k pull-down resistor.

Solution: ldo5v_off_filter needs to be set longer than the time it takes for the charging case to drop to 0 and then rise to the maintenance voltage (note that the rise time may be different when one ear and two ears are in the case)

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Question 2: For Type 2 or Type 3 charging cases, the first earphone placed in the case can be charged, but the second earphone placed in the case cannot be charged

Reason: The output ripple of the charging case may be too large, causing the charging de-bouncing detection to be unstable.

Solution: Reduce the charging current of the earphones until the output ripple of the charging case is small.

Question 3: For charging case type 3, the charging case does not increase voltage, and the red light flashes after the earphones are placed in the case

Reason: The pull-up resistor value of the charging case is small. After the earphones are in the case, their own power consumption is not enough to pull down the maintenance voltage. The earphones detect that the LDOIN voltage is greater than the earphone battery voltage, and the earphones start charging. After charging is turned on, the maintenance voltage will be lowered again.

Solution: Change the pull-up resistor of the charging case to 100K, and add a pull-down resistor of 100K to the LDOIN of the earphone end (after the earphone is put into the case, the LDOIN voltage can be kept at 1~2V, and the actual value is subject to testing). For the mass-produced models, change the 222 capacitor at the LDOIN pin to 100K Resistor. If this type of model also needs to support serial port upgrade, add a 222 capacitor at the serial port of the test box.

Question 4: For charging case type 3, it is slow to start up after unplugging the device

Cause: After leaving the warehouse, LDOIN has reverse leakage, which causes the LDOIN voltage to take a long time to drop to the unplug voltage.

Solution: Add a 100K pull-down resistor to the earphone LDOIN to speed up the discharge of LDOIN. The pull-up resistor at the charging compartment should follow point 3 and be changed to 100K to configure.

Appendix 1: Notes on crystal oscillator module **layout**

ÿ The crystal oscillator should be placed as close to the main control pin as possible, and the placement distance should not exceed 1CM. ÿ There should be no digital signal lines near the crystal oscillator, especially SD card signal lines, USB signal lines, IIC signal lines, infrared receiving signals, And other CLK signals, and do not run them in parallel. Both sides of the crystal oscillator wiring must be wrapped with power or ground. The schematic diagram is as follows:

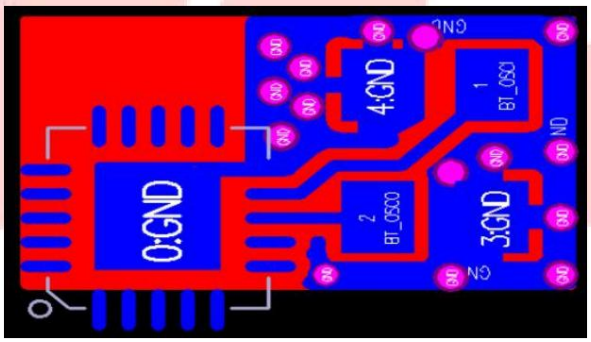

Figure 1: Crystal oscillator layout and wiring diagram

Appendix **2: DCDC** module **layout** considerations

ÿ Give priority to ensuring the connectivity of the ground loop and avoid the ground loop line being too long or too thin

ÿ Place the power decoupling capacitors such as VMCU, VDDIO, and BTAVDD as close to the chip pins as possible, and keep the ground loop as short as possible.

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ÿ Focus on the layout of the DCDC power supply, which should be kept away from the antenna and close to the battery end. The schematic diagram is as follows:

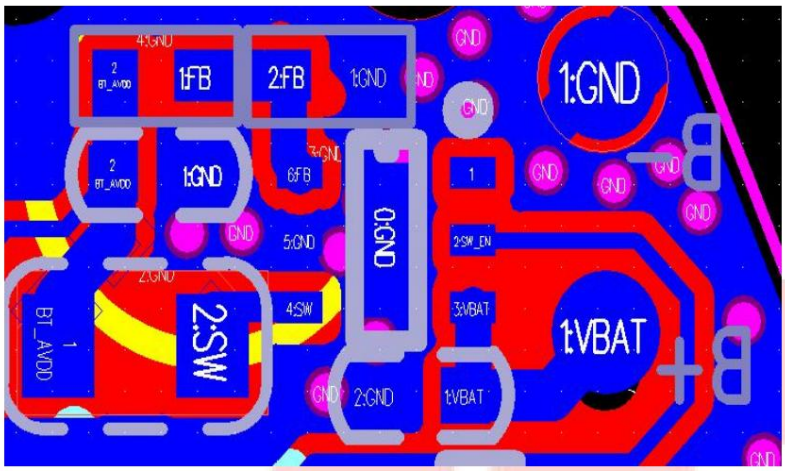


Figure 2: DCDC layout and routing diagram

Specific requirements are as follows:

1) The DCDC chip ensures the integrity of the three ground points, at least one side of the ground (the input capacitor ground, output capacitor ground, and chip ground confluence routing should be as close as possible).

Short), pay special attention to the two-layer board;

2) The output inductor of the DCDC chip must pass through the filter capacitor before supplying power to the main control BT-AVDD. The DCDC inductor should be a winding inductor as much as possible.

Rated current greater than 120mA, DC resistance less than 0.5R

3) The inductor should be close to the SW pin. The SW network should not be drilled as much as possible. It should be as short and thick as possible. Do not run wires or place components under or on the reverse side of the inductor. Pay

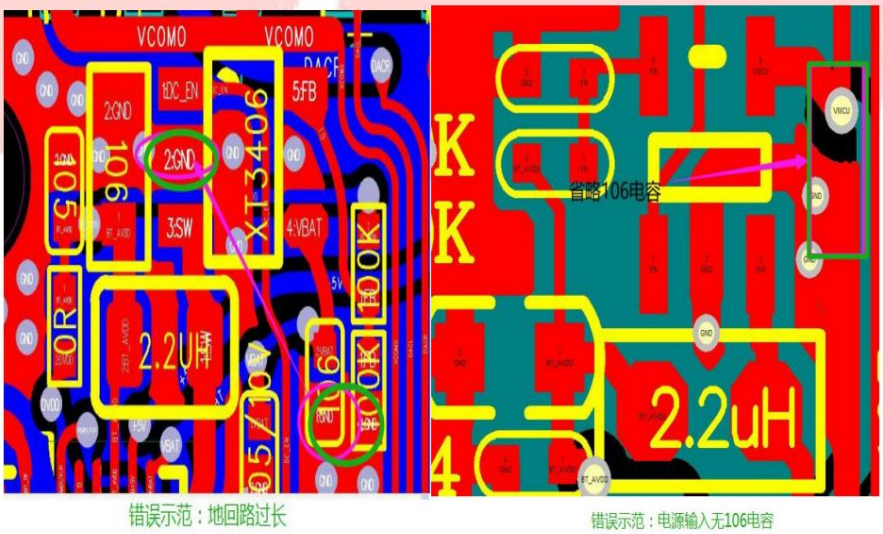
special attention to the routing and layout of the mic to avoid interfering with the mic.

4) The FB sampling point is taken after the output capacitor is filtered, and the voltage divider resistor is close to the FB pin to ensure that the wiring after voltage division is as short as possible.

5) Keep the DCDC circuit as far away from the Bluetooth antenna as possible to avoid interference with Bluetooth.

6) The component parameters and requirements on the standard schematic diagram cannot be changed at will. If you want to modify them, you must conduct a trial production test.

The following figure is an error demonstration:



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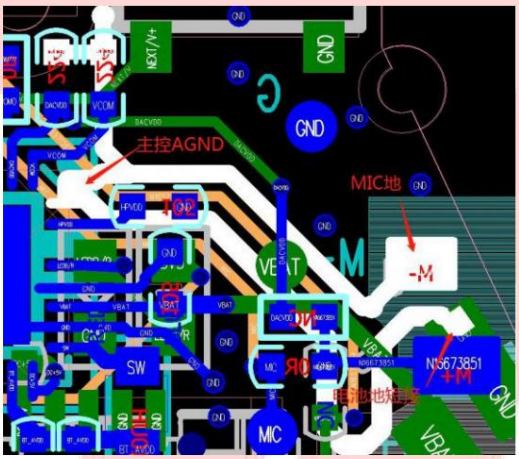
Appendix 3: Notes on **the layout** of audio signal lines and **AGND**

Mainly involves the processing of audio signal lines and ground lines:

1. About the processing of audio signal lines:

When routing audio signals such as DACL, DACR, AUXL, AUXR, and MIC, be careful to keep them away from digital signals (LCD/LED signals, USB, SD, etc.) 2. About

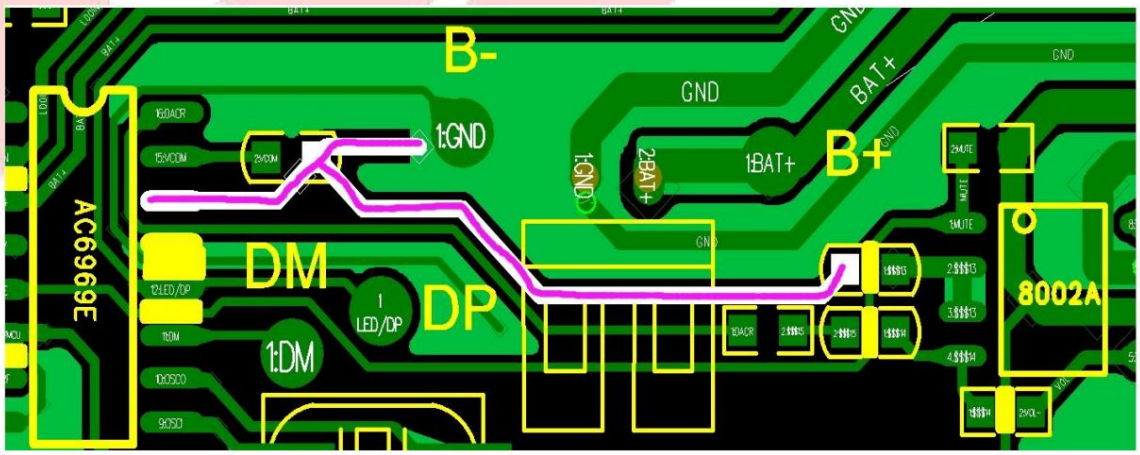
the processing of MIC AGND: Prioritize to ensure that the MIC ground loop is clean, and the MIC ground is required to be connected to the analog ground AGND; when wiring, the MIC ground is connected to AGND, and the order of the ground loop is MIC ground-->main control AGND-->battery ground GND short-circuited; the schematic diagram is as follows:



Note: If the board frame is limited and the battery ground cannot be shorted, the microphone ground AGND is routed to the main control AGND and shorted to the digital ground nearby. GND (This method depends on the actual test results)

3. About the processing of speaker AGND:

PCB requires digital ground GND and analog ground AGND; when wiring, the bypass capacitor of the power amplifier needs to be connected to AGND, and the order of the ground loop is bypass capacitor AGND--> main control VCOM decoupling capacitor ground DACVSS--> battery ground GND. The short circuit requires the routing to be as short as possible and as large as possible. The schematic diagram is as follows:



Appendix **4: FM** module **layout** considerations

1. FM reception is more sensitive and easily interfered with. When placing the IC, the positions of the Bluetooth antenna and FM antenna should be considered.

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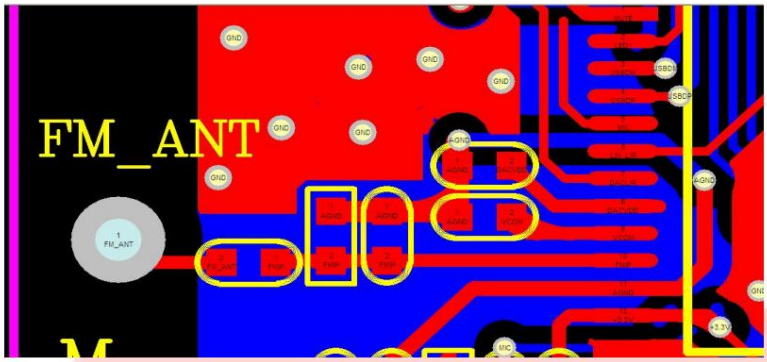
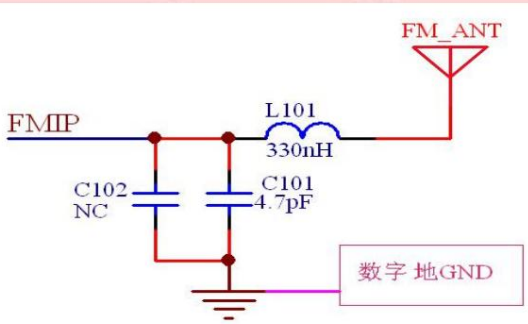
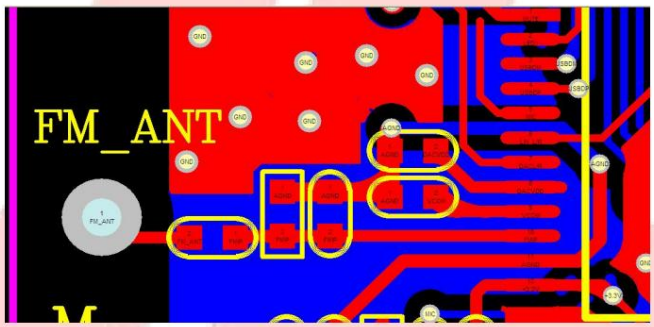
Place it on the edge of the board. The FM antenna has the shortest trace on the board. Be careful not to coil the soldered external antenna too much on the PCBA.



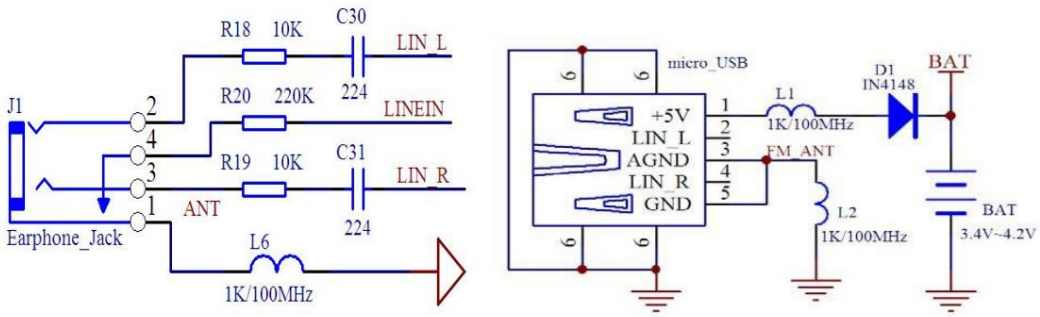
2. The antenna matching network is placed close to the chip pins. The antenna circuit uses GND as the reference ground. The parameters are shown in the figure below.



3. The FM antenna must be routed away from other signal lines. The antenna must be routed close to the board edge. A large area of GND must be laid around the FM antenna matching network to ensure the integrity of the FM reference ground plane. The battery ground welding point should be placed as close to the FM as possible to ensure the shortest GND loop and reduce interference. The safe distance between the antenna and GND copper should be increased, and 0.6mm or more is recommended.



4. Anti-interference treatment of FM antenna reuse circuit. Some circuit designs will reuse antennas such as audio sockets and micro USB charging sockets to improve FM performance. However, when designing the circuit, be careful not to make the antenna routing too "winding", "long", or have too many forks. When the FM antenna is lengthened, reduce the interference of other lengthened signal lines to FM. As shown in the figure below, please place R18, R20, R19, L6, L1, and L2 close to the corresponding sockets.



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