Name - Monu
Entry No. - 2020CSS0432

Notebook
Date: / /
Page

Conditional checking → Cond_check.

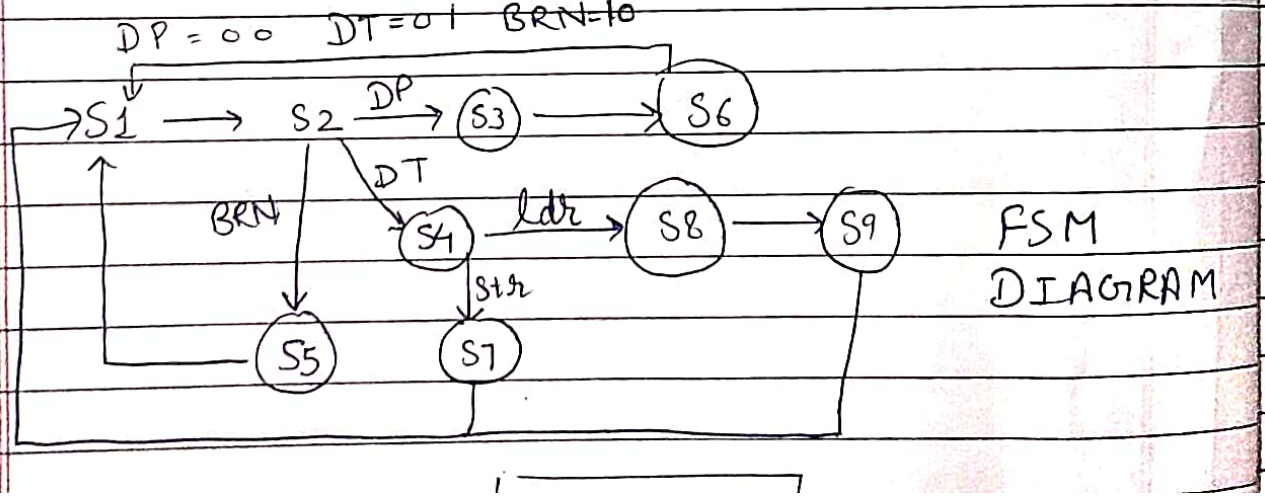
We had used different components for making Multicycle Processor.

Finite state machine have 3 states which outputs the different control signals as shown below:

depending on IR goto S3/S4/S5 → S6

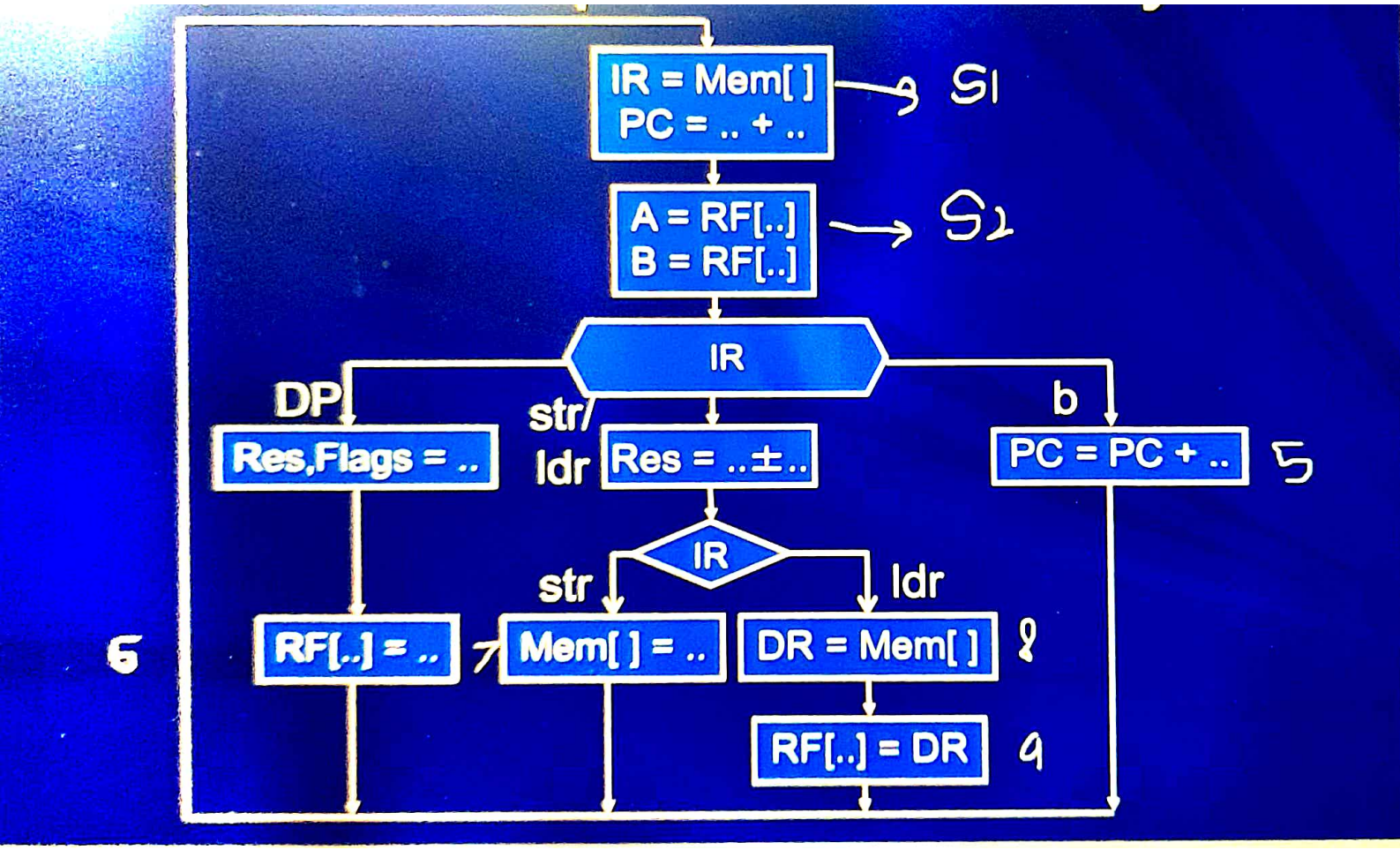
according ld/str. S7/S8 → 1 → 1 → 1 → 9 →

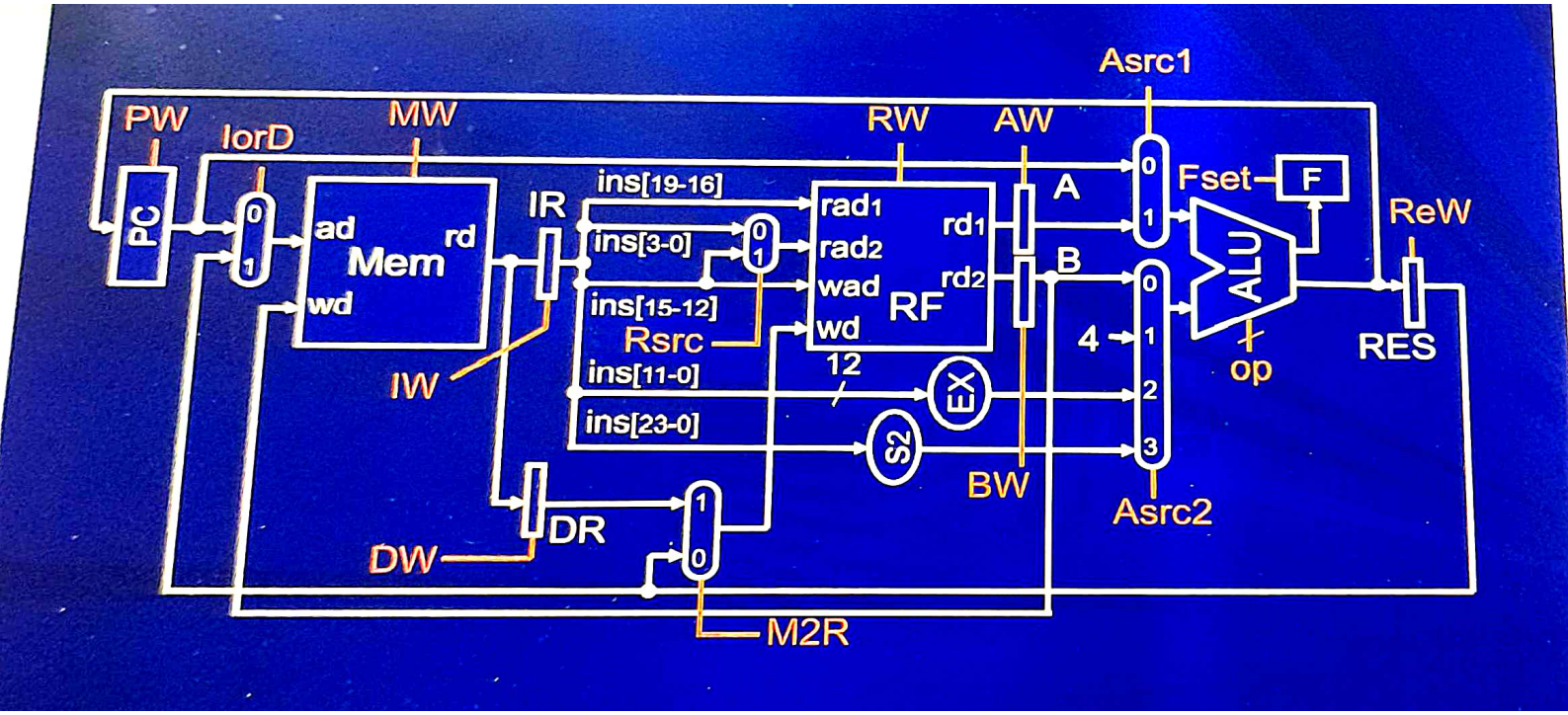
out \ state	S1	S2	S3	S4	S5	S6	S7	S8	S9
IW	1	0	0	0	0	0	0	0	0
AW	0	1	0	0	0	0	0	0	0
BW	0	1	0	0	0	0	0	0	0
DW	0	0	0	0	0	0	0	1	0
ReW	0	0	1	1	1	0	0	0	0
PW	1	0	0	0	0	0	0	0	0
IorD	0	x	x	x	x	0	1	1	x
MW	0	0	0	0	0	0	1	0	0
RW	0	0	0	0	0	1	0	0	1
RSrc	0	1	x						
M2R	x	x	x	x	x	0	x	x	1
ASrc1	0	x	1	1	0	x	x	x	x
ASrc2	1	x	0	2	3	x	x	x	x
~~oop~~ add		x	~~op~~	op					
Fset	0	0	1	0	0	0	0	0	0



FSM DIAGRAM

Here S1 – S9 are states. and outputs are also shown in figure above.


IR = Mem[ ]
PC = .. + ..
S1
A = RF[..]
B = RF[..]
S2
IR
DP
Res,Flags = ..
str/
ldr
Res = ..±..
b
PC = PC + ..
5
IR
str
ldr
RF[..] = ..
Mem[ ] = ..
DR = Mem[ ]
8
RF[..] = DR
9
6


Asrc1
PW
IorD
MW
RW
AW
PC
ad
rd
Mem
wd
IR
ins[19-16]
ins[3-0]
ins[15-12]
Rsrc
ins[11-0]
ins[23-0]
rad1
rad2
wad
wd
RF
rd1
rd2
12
EX
S2
A
B
BW
4
Fset
F
ALU
op
ReW
RES
Asrc2
IW
DR
DW
M2R

All different components are combined in file controller.vhd.