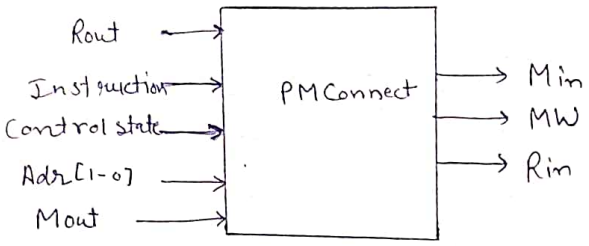
NAME = MONU
ENTRY No. = 2020CS50432
Assignment = 2
Subtask = 6.

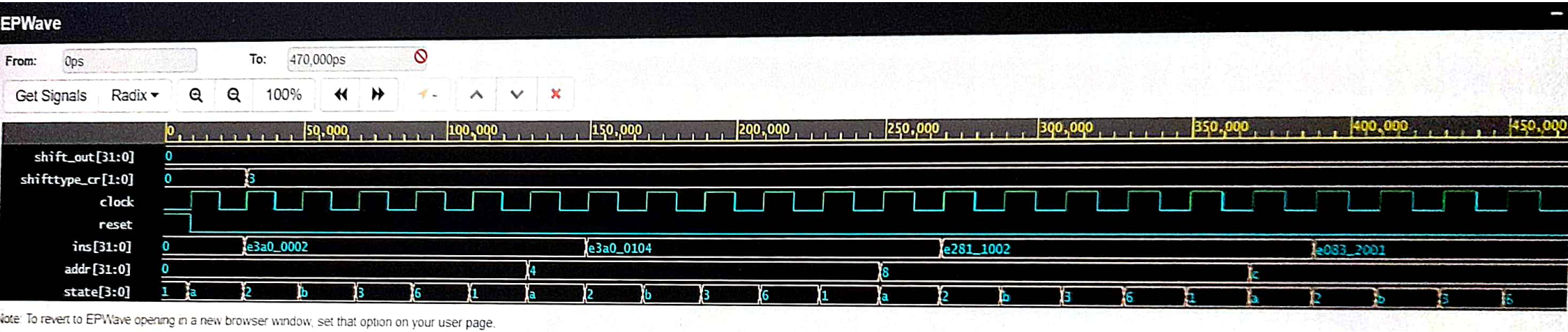


Files and Folders in Submission

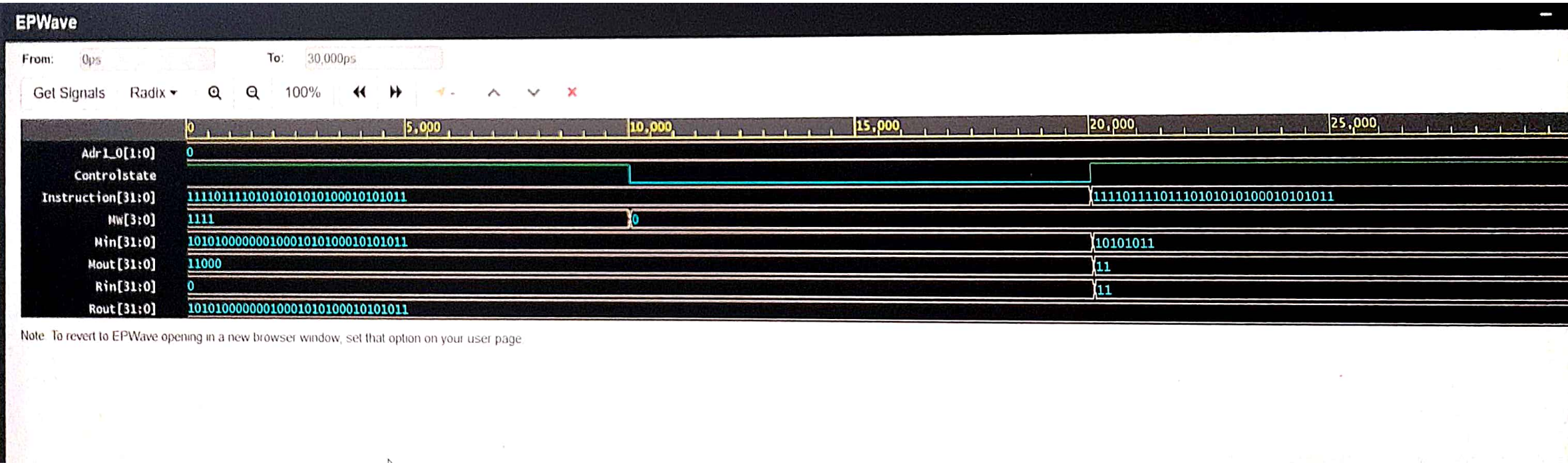
Multicycle Processor folder contain Design.vhd and testbench.vhd with glue and logics implemented for PMconnect.

PMConnect.vhd → Design file for PMCo
PMConnect_tb.vhd → testbench for PMCon
Mem.vhd → New Memory file.

There is change in Memory, now we have to change 1-bit Memory write enable signal to 4-bit signal. So that we can write in Memory in different forms.



Note: To revert to EPWave opening in a new browser window, set that option on your user page.


EPWave
From:
0ps
To:
30,000ps
Get Signals
Radix
100%
0
5,000
10,000
15,000
20,000
25,000
Adr1_0[1:0]
Controlstate
Instruction[31:0]
11110111101010101010100010101011
11110111101110101010100010101011
MW[3:0]
1111
0
Min[31:0]
10101000000010001010100010101011
10101011
Mout[31:0]
11000
11
Rin[31:0]
0
11
Rout[31:0]
10101000000010001010100010101011
Note: To revert to EPWave opening in a new browser window, set that option on your user page.