CRUSOE PROCESSOR

1. INTRODUCTION

Mobile computing has been the buzzword for quite a long time. Mobile computing devices like laptops, notebook PCs etc are becoming common nowadays. The heart of every PC whether a desktop or mobile PC is the microprocessor. Several microprocessors are available in the market for desktop PCs from companies like Intel, AMD, Cyrix etc. The mobile computing market has never had a microprocessor specifically designed for it. The microprocessors used in mobile PCs are optimized versions of the desktop PC microprocessor.

Mobile computing makes very different demands on processors than desktop computing. Those desktop PC processors consume lots of power, and they get *very* hot. When you're on the go, a power-hungry processor means you have to pay a price: run out of power before you've finished, or run through the airport with pounds of extra batteries. A hot processor also needs fans to cool it, making the resulting mobile computer bigger, clunkier and noisier. The market will still reject a newly designed microprocessor with low power consumption if the performance is poor. So any attempt in this regard must have a proper 'performance-power' balance to ensure commercial success. A newly designed microprocessor must be fully x86 compatible that is they should run x86 applications just like conventional x86 microprocessors since most of the presently available software has been designed to work on x86 platform.

Crusoe is the new microprocessor, which has been designed specially for the mobile computing market .It has been, designed after considering the above-mentioned constraints. A small Silicon Valley startup company called Transmeta Corp developed this microprocessor.

The concept of Crusoe is well understood from the simple sketch of the processor architecture, called 'amoeba'. In this concept, the x86 architecture is an ill-defined amoeba containing features like segmentation, ASCII arithmetic, variable-length instructions etc. Thus Crusoe was conceptualized as a hybrid microprocessor, i.e. it has a software part and a hardware part with the software layer surrounding the hardware unit. The role of software is to act as an emulator to translate x86 binaries into native code at run time. Crusoe is a 128-bit microprocessor fabricated using the CMOS process. The chip's design is based on a technique called VLIW to ensure design simplicity and high performance. The other two technologies using are Code Morphing Software and LongRun Power Management. The crusoe hardware can be changed radically without affecting legacy x86 software: For the initial Transmeta products, models TM3120 and TM5400, the hardware designers opted for minimal space and power.

2. CRUSOE PROCESSOR VLIW HARDWARE
2.1. Basic principles of VLIW Architecture

VLIW stands for Very Long Instruction Word. VLIW is a method that combines multiple standard instructions into one long instruction word. This word contains instns that can be executed at the same time on separate chips or different parts of the same chip. It provides explicit parallelism, i.e. executing more than one basic (primitive) instn at a time. By using VLIW you enable the compiler, not the chip to determine which instructions can be run concurrently. This is an advantage because the compiler knows more information about the program than the chip does by the time the code gets to the chip.

Trace scheduling is an important technique in VLIW processing. i.e. the compiler processes the code and determines which path is the most frequently traveled, and then optimizes this path. Basic blocks that compose the path are separated from the other basic blocks. The path is then optimized and rejoined with the other basic blocks using split and rejoin blocks.

Dynamic scheduling is another important method when compiling VLIW code. The process called split-issue splits the code into two phases, phase one and two. This allows for multiple instns, instns having certain delays etc to execute at the same time. H/W support is needed to implement this, and needs delay buffers and temporary variable space (TVS) in the h/w. The TVS is needed to store results when they come in. The results computed in phase two are stored in temporary variables and are loaded into the appropriate phase one register when they are needed.

VLIW has been described as *a natural successor to RISC,* whose instn set consists of simple instructions (RISC-like). because it moves complexity from the hardware to the compiler, allowing simpler, faster processors. One objective of VLIW is to eliminate the complicated instruction scheduling. The compiler must assemble many primitive operations into a single "instruction word" such that the multiple functional units are kept busy.

2.2. Crusoe VLIW in Microprocessor

With the Code Morphing software handling x86 compatibility, Transmeta hardware designers created a very simple, high-performance, VLIW engine with two integer units, a floating-point unit, a memory (load/store) unit, and a branch unit. A Crusoe processor long instruction

word, called a molecule, can be 64 bits or 128 bits long and contain up to four RISC-like nstructions,called atoms. All atoms within a molecule are executed in parallel, and the molecule format directly determines how atoms get routed to functional units; this greatly simplifies the decode and dispatch hardware. Figure 1 shows a sample 128-bit molecule and the straightforward mapping from atom slots to functional units. Molecules are executed in order, so there is no complex out-of-order hardware. To keep the processor running at full speed, molecules are packed as fully as possible with atoms. In a later section, we describe how the Code Morphing software accomplishes this.

The integer register file has 64 registers, %r0 through %r63. By convention, the Code Morphing software allocates some of these to hold x86 state while others contain state internal to the system, or can be used as temporary registers, e.g., for register renaming in software.

Superscalar out-of-order x86 processors, such as the Pentium II and III processors, also have multiple functional units that can execute RISC-like operations (micro-ops) in parallel. Figure 2 depicts the hardware these designs use to translate x86 instructions into micro-ops and schedule (dispatch) the micro-ops to make best use of the functional units. Since the dispatch unit reorders the micro-ops as required to keep the functional units busy, a separate piece of hardware, the in-order retire unit, is needed. To effectively reconstruct the order of the original x86 instructions, and ensure that they take effect in proper order. Clearly, this type of processor hardware is much more complex than the Crusoe processor's simple VLIW engine.

Because the x86 instruction set is quite complex, the decoding and dispatching hardware requires large quantities of power-hungry logic transistors; the chip dissipates heat in rough proportion to their numbers.

6. CRUSOE PROCESSOR ARCHITECTURE

The Crusoe microprocessor is available in the market in the following versions: TM3120, TM3200, TM5400 and TM5600.The basic architecture of all the above models are same except for some minor changes since various models have been introduced for different segments of the mobile computing market. The following architectural description has taken Crusoe TM5400 as reference.

The Crusoe Processor incorporates integer and floating point execution units, separate instruction and data caches, a level-2 write-back cache, memory management unit, and multimedia instructions. In addition to these traditional processor features, there are some additional units, which are usually part of the core system logic that surrounds the microprocessor. The VLIW processor, in combination with Code Morphing software and the additional system core logic units, allow the Crusoe Processor to provide a highly integrated, ultra-low power, high performance platform solution for the x86 mobile market.

6.1. Processor Core

The Crusoe Processor core architecture is relatively simple by conventional standards. It is based on a VLIW 128-bit instn set. Within this VLIW architecture, the control logic of the processor is kept very simple and s/w is used to control the scheduling of instns. This allows a simplified and very straightforward h/w implementation with an in-order 7-stage integer pipeline and a 10-stage floating-point pipeline. By streamlining the processor h/w and reducing the control logic transistor count, the performance-to-power consumption ratio can be greatly improved over traditional x86 architectures.

The Crusoe Processor includes an 8-way set-associative Level 1 (L1) instn cache, and a 16-way set associative L1 data cache. It also includes an integrated Level 2 (L2) write-back cache for improved effective memory bandwidth and enhanced performance. This cache architecture assures maximum internal memory bandwidth for performance intensive mobile applications, while maintaining the same low-power implementation that provides a superior performance-to-power consumption ratio relative to previous x86 implementations.

Other than having execution h/w for logical, arithmetic, shift, and floating point instns, as in conventional processors, the Crusoe has very distinctive features from traditional x86 designs. To ease the translation process from x86 to the core VLIW instn set, the h/w generates the same condition codes as conventional x86 processors and operates on the same 80-bit floating-point numbers. Also, the TLB has the same protection bits and address mapping as x86 processors. The s/w component of this solution is used to emulate all other features of the x86 architecture. The s/w that converts x86 programs into the core VLIW instns is the CMS.

6.2. Integrated DDR SDRAM Memory Controller

DDR SDRAM interface is the highest performance memory interface available on the Crusoe. The DDR SDRAM controller supports only Double Data Rate (DDR) SDRAM and transfers

data at a rate that is twice the clock frequency of the inter-face. This feature is absent in the model TM 3200.

The DDR SDRAM controller supports up to four banks, the equivalent of two Dual In-line Memory Modules (DIMMs), of DDR SDRAM using a 64-bit wide inter-face. The DDR SDRAM memory can be populated with 64M-bit, 128M-bit, or 256M-bit devices. The frequency setting for the DDR SDRAM interface is initialized during the power-on boot sequence.

6.3. Integrated SDR SDRAM Memory Controller

The SDR SDRAM memory controller supports up to four banks, equivalent to two Small Outline Dual In-line Memory Modules (SO-DIMMS), of Single Data Rate (SDR) SDRAM that can be configured as 64-bit or 72-bit SO-DIMMs. These SO-DIMMs can be populated with 64M-bit, 128M-bit or 256M-bit devices. All SO-DIMMs must use the same frequency SDRAMs, but there are no restrictions on mixing different SO- DIMM configurations into each SO-DIMM slot. The frequency setting for the SDR SDRAM interface is initialized during the power-on boot sequence.

6.4. Integrated PCI Controller

The Crusoe Processor includes a PCI bus controller that is PCI 2.1 compliant. The PCI bus is 32 bits wide, operates at 33 MHz, and is compatible with 3.3V signal levels. It is not 5V tolerant, however. The PCI controller on provides a PCI host bridge, the PCI bus arbiter, and a DMA controller.

6.5. Serial ROM Interface

The Crusoe serial ROM interface is a five-pin interface used to read data from a serial flash ROM. The flash ROM is 1M-byte in size and provides non-volatile storage for the CMS. During the boot process, the Code Morphing code is copied from the ROM to the Code Morphing memory space in SDRAM. Once trans-erred, the Code Morphing code requires 8 to 16M-bytes of memory space. The portion of SDRAM space reserved for CMS is not visible to x86 code. Transmeta supplies programming information for the flash ROM device. This interface may also be used for in-system reprogramming of the flash ROM

7. FEATURES OF VARIOUS CRUSOE PROCESSORS

7.1. Crusoe Processor Model TM3200 Features

• VLIW processor and x86 Code Morphing software provide x86-
   compatible mobile platform solution.
  • Processor core operates at 366 and 400 MHz.
  • Integrated 64K-byte instruction cache and 32K-byte data cache.
  • Integrated Northbridge core logic features facilitate compact system
   designs.
  • SDR SDRAM memory controller with 66-133 MHz, 3.3V interface
  • PCI (Peripheral Component Interface) bus controller (PCI 2.1 compliant)
   with 33 MHz, 3.3V interface
  • Advanced power management features and very-low power operation
   extend mobile battery life
  • Full System Management Mode (SMM) support
  • Compact 474-pin ceramic BGA (Ball Grid Array) package

7.2. Crusoe Processor Model TM5400

 • VLIW processor and x86 Code Morphing software provide x86-
   compatible mobile platform solution
 • Processor core operates at 500-700 MHz
 • Integrated 64K-byte L1 instruction cache, 64K-byte L1 data cache, and
   256K-byte L2 write-back cache
 • Integrated north bridge core logic features facilitate compact system
   designs
 • DDR SDRAM memory controller with 100-133 MHz, 2.5V interface
 • SDR SDRAM memory controller with 66-133 MHz, 3.3V interface
 • PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3V interface
 • LongRun advanced power management with ultra-low power operation
   extends mobile battery life! 1-2 W @ 500-700 MHz, 1.2-1.6V running
   typical multimedia applications! 50 mW in deep sleep.
 • Full System Management Mode (SMM) support

• Compact 474-pin ceramic BGA package

7.3. Crusoe Processor Model TM5600 Features

- VLIW processor and x86 Code Morphing software provide x86-compatible mobile platform solution
- Processor core operates at 500-700 MHz
- Integrated 64K-byte L1 instruction cache, 64K-byte L1 data cache, and 512K-byte L2 write-back cache
- Integrated north bridge core logic features facilitate compact s/m designs
- DDR SDRAM memory controller with 100-133 MHz, 2.5V interface
- SDR SDRAM memory controller with 66-133 MHz, 3.3V interface
- PCI bus controller (PCI 2.1 compliant) with 33 MHz, 3.3V interface
- LongRun advanced power management with ultra-low power operation extends mobile battery life! 1-2 W @ 500-700 MHz, 1.2-1.6V running typical multimedia applications! 100 mW in deep sleep
- Full System Management Mode (SMM) support

8. CONCLUSION

In 1995, Transmeta set out to expand the reach of microprocessors into new markets by dramatically changing the way microprocessors are designed. The initial market is mobile computing, in which complex power-hungry processors have forced users to give up either battery running time or performance. The Crusoe processor solutions have been designed for lightweight (two to four pound) mobile computers and Internet access devices such as handhelds and web pads. They can give these devices PC capabilities and unplugged running times of up to a day.

To design the Crusoe processor chips, the Transmeta engineers did not resort to exotic fabrication processes. Instead they rethought the fundamentals of microprocessor design. Rather than "throwing hardware" at design pblms, they chose an innovative approach that employs a unique combination of hardware and software. Using software to decompose complex instructions into simple atoms and to schedule and optimize the atoms for parallel execution saves millions of logic transistors and cuts power consumption on the order of 60–70% over conventional approaches. Transmeta's Code Morphing software and fast VLIW hardware, working together, achieve low power consumption without sacrificing high performance for real-world applications.

Although the model TM3120 and model TM5400 are impressive first efforts, the significance of the Transmeta approach to microprocessor design is likely to become more apparent over the next several years. Freed to render their ideas in a combination of hardware and software, and to evolve hardware without breaking legacy code, Transmeta microprocessor designers may produce updated versions in the coming years.

8. REFERENCES

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