An Investigation of Power Consumption for Fault-Tolerant Digital Circuits

Thesis

Presented in Partial Fulfillment of the Requirements for the Degree Master of Science in the Graduate School of The Ohio State University

By

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Abstract

Power consumption is an important aspect in electronic systems. Lowering the power consumption of the components in the system can increase the system's energy efficiency and lower the heat dissipated to its surrounding area.

FPGAs and CPLDs are devices found in electronic systems. Depending on the digital circuit programmed onto them, the current consumption may vary. If this is the case, then a new way to define the efficiency of a digital circuit is possible; one that includes the power consumed by the FPGA or CPLD. Fault-tolerant digital circuits that include error detection may be able to operate on a FPGA or CPLD at a lower supply voltage and decrease its power consumption.

This thesis includes the preliminary and proof-of-concept work to show that devices do consume different amounts of power based on the digital circuit programmed onto them. Additionally, if fault-tolerant circuits are used, then the device can operate at a lower voltage and ultimately consume less power, even though the fault-tolerant digital circuit is larger and more complex.

To fully test this idea, the current and power consumed by Altera MAX7000S chips will be measured while operating various circuits. The circuits used will be a 4-bit binary code counter, a 4-bit gray code counter and a dual-rail 4-bit gray code counter with error detection. It will be found that the binary code counter consumed more power than the gray code counter and that, at a voltage of approximately 4.8 V, the dual-rail gray code counter with error detection consumed less power than the standard 4-bit gray code counter.

Dedication

This document is dedicated to my friends and family.

Acknowledgements

I would like to take this opportunity to acknowledge the assistance that I had during the course of this project.

First, I would like to thank my advisor, Dr. Joanne DeGroat, for allowing me the opportunity to further my education both as an undergraduate and as a graduate student. I have enjoyed working on this project with her and it has been a great opportunity for me and for my education. I would also like to thank her for being an excellent advisor and helping me in my future planning.

Second, I would like to thank my once T.A., once supervisor and always friend, Philippe Hall who acted as a second person I could bounce ideas off of during the initial phases of this project as I worked on the automated approach.

Third, I would like Dr. Füsun Özgüner for providing feedback on my thesis document and assisting me with the requirements for the M.S. thesis.

Fourth, I would like to thank Dr. Wladimiro Villarroel for being my second committee member and issuing my defense.

Fifth, I would like to thank the six anonymous reviewers from the IEEE VLSI Test Symposium that took the time to read a very rough submission and provide feedback. I do not have much experience in professional writing at the graduate and doctorial level but the comments I received were very helpful and have been integrated into this thesis document.

Last and most important, I would like to thank my family and friends who have supported me throughout my college career and have made the past five years more enjoyable than I could have imagined.

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Chapter 1: Introduction

Power consumption minimization is a high priority in today's electronics. Minimization of power consumption of the circuit's components leads to more energy efficient circuits and less heat dissipation to the surrounding circuit. Energy efficiency is also a popular topic in today's energy conscious and 'green' mindset.

Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) are devices used in these electronics [1]. These are referred to as devices collectively in this thesis though CPLDs were the devices worked with in the experiment. Both of these are programmable devices. Digital circuits are constructed using one or some combination of pictorial schematic editors or hardware description languages (HDLs) and uploaded to the device. These devices operate at some voltage specified by the manufacturer. If the device is not supplied with the correct voltage then errors may occur in the device. However, it is possible that extra logic can be added to a digital circuit that can detect errors from the device and thus the device can operate at a lower voltage and consume less power than it would under normal operating conditions.

There are some negatives that must be addressed, the largest of which is the increase in the digital circuit's size. The added fault-tolerance leads to less room on the chip for other components (e.g. memory for a processor or less resolution for ALUs). Additionally, if the fault-tolerance is added off-chip, or if the fault-tolerance pushes other digital circuitry off of the chip so that a new chip must be added, then there may be weight considerations as well. These weight considerations could be overcome with larger devices but with an increase in cost. However the positives of energy-efficiency and less heat dissipation will outweigh the negatives for several applications and whether or not a designer would want to include this feature will vary on a case-by-case basis.

This thesis is a proof-of-concept approach to this hypothesis. This thesis begins by taking a deeper look at the hypothesis and the theory behind it. Following that is an overview of the experiment that tested the hypothesis. The section after outlines the digital circuits used followed by a section discussing the parameters of the experiment. After this, the results from the experiment are shown and discussed. Following that, an automated approach is introduced. Lastly are the conclusions and future directions.

Chapter 2: Hypothesis and Theory:

There are two pieces to the hypothesis. First, there is a measurable difference between various digital architectures with regards to power consumption. This would imply an advantage to choosing one digital circuit over another. Second, if a digital circuit can be constructed which can detect errors then the voltage supplied to the device can be lowered and any errors that result can be caught. The combination of these leads to the full hypothesis: if a digital circuit can be constructed to detect errors while operating at a lower voltage then this design will be superior to the same design which does not contain any error detection or correction pieces but operates at the standard voltage.

Both CPLDs and FPGAs are CMOS (complementary metal-oxide semiconductor) devices. The power consumed by a CMOS device is [2]

$$[\text{Equation 1}]\ P = C * V^2 * f * n$$

Where P is the power, C is the capacitance of the device, V is the voltage supplied to the device, f is the frequency that the device switches from one state to the next and n is the number of bits that switch states.

The two terms of relevance to this hypothesis are V and n. With these terms, the hypothesis is written as: a decrease in P can be observed if n is raised due to adding fault tolerance but V is allowed to be lowered due to this fault tolerance. An increase in n must occur for fault tolerance because a fault tolerant version of the same circuit must add fault tolerant logic. By how much n increases is unknown. This increase in n will allow for a decrease in V, whose quantity is also unknown. However, this project will investigate if the decrease in power consumption resulting from a decrease in V is greater than the power consumption resulting from an increase in n.

Chapter 3: Experiment Overview:

To test the hypothesis, an experiment was devised that would measure the current through a CPLD as a digital circuit was running on it. The device itself was isolated, that is, it was not driving any outputs or extra peripherals. Four CPLDs were tested: two EPM7064SLC84-10 devices and two EPM7128SLC84-15 devices. All of these were from the MAX 7000S family of CPLDs manufactured by Altera and have a standard operating voltage of 5V. These devices were selected because they were cheap, available in a breadboard mountable package, and attainable. These devices can be programmed using Quartus, software developed by Altera for use with its products. Details on wiring and using the CPLDs were found on its pin-out sheet [3] and datasheet [4].

The devices were programmed using a Terasic USB-Blaster cable shown in Figure 1 below.

Figure 1: USB-Blaster Cable

This cable connected to the computer through a USB interface and connected to the CPLD device through a JTAG interface. The pin-outs of the USB-Blaster were found on its datasheet [5].

To run the CPLD, the largest frequency clock that was available was used. This clock was a 50 MHz oscillator generated by an Altera DE2 Development Board [6], shown in Figure 2, available in the laboratory.

http://www.altera.com/education/univ/images/boards/de2.jpg

Figure 2: Altera DE2 Board by Terasic

A simple digital circuit routed the 50 MHz clock usually used by the FPGA on the DE2 board to the its GPIO pins. Unlike the CPLDs, the DE2 Board already had a USB interface built in so it could be programmed immediately from the Quartus programmer. All of the trials used the 50 MHz clock from this board. The schematic shown in Figure 3 routed the 50 MHz clock to the GPIO pins.

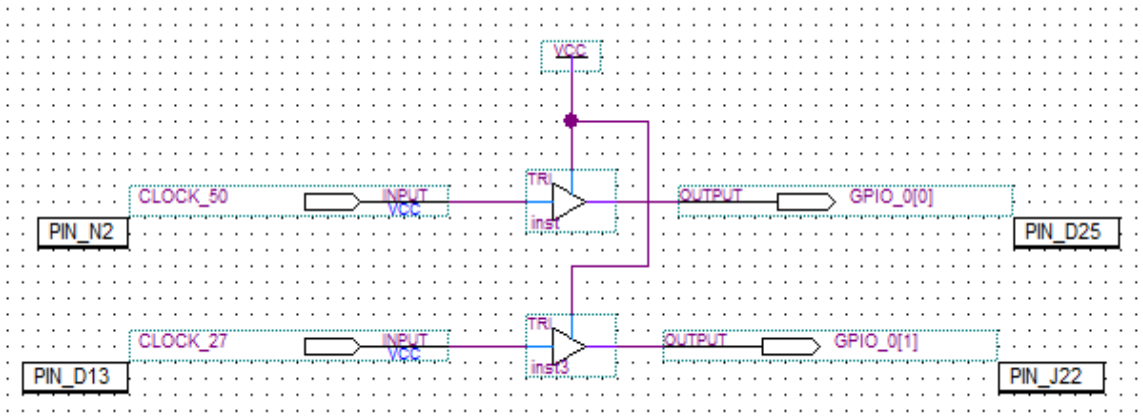

Figure 3: Schematic for routing the 50 and 27 MHz Oscillators to the DE2 Digital pins.

The current was measured using two devices: a Fluke 115 multi-meter and the voltage source. The voltage source (a RIGOL DP1308A) has a built in amp-meter and can display how much current it was supplying to the device. The recordings from both methods were compared.

All of the above components were linked together to construct the final circuit. A digital oscilloscope was used periodically to confirm that the correct digital circuit was programmed onto the CPLD and that the 50 MHz clock was functioning correctly. However, the oscilloscope consumed some current so the oscilloscope was not used during the experiment. The pins of the CPLD were chosen using Quartus' pin planner tool. Only the JTAG, VCC and GND pins were locked in their positions.

The voltage was lowered as each digital circuit was running on the device. The voltage started at the device's standard operating voltage of 5 V and the device was programmed. The voltage was lowered in increments of 0.1 V until 3.8 V was reached. The current and power consumed was measured at each voltage step. The device was not reprogrammed in between voltage steps and stayed at a voltage level until the multi-meter and built in amp-meter showed stable measurements. This usually took 5-10 seconds. If no stable measurement was found (the reading would oscillate between two values usually 0.001 amps apart) then the larger reading was taken.

After 3.8 volts was reached, the power was disconnected and the device was powered down for at least 30 seconds. Then, the device was powered back on at 5 volts and reprogrammed. This process was repeated five times for each circuit tested. When the digital circuit was programmed onto the device the first time, the oscilloscope was connected to verify that the device was working correctly. Then, the oscilloscope was disconnected, the device power cycled again, reprogrammed and the trial started. This entire process would be repeated four times, once for each CPLD available.

Chapter 4: Digital Circuits

Three distinct circuits were used in this experiment. The circuits were a four-bit binary counter (shown in Figure 4), a four-bit gray code counter (shown in Figure 5) and a dual-rail four-bit gray code counter with error detection (shown in Figure 6). Both the binary counter and gray code counter used four macro-cells and the dual-rail gray code counter with error detection used ten macro-cells. The binary counter was implemented using a LPM (library of parameterized modules) [7] block provided by Altera for use in its Quartus software. The gray code counter was implemented with VHDL code provided by Dr. DeGroat. The dual rail gray code counter used this VHDL code as well. Its error detection functioned by taking two independent gray code counters and comparing their results.

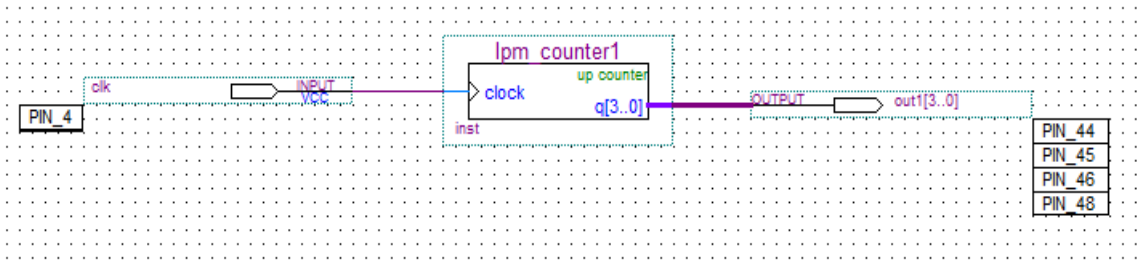

Figure 4: Four-Bit Binary Code Counter Digital Circuit

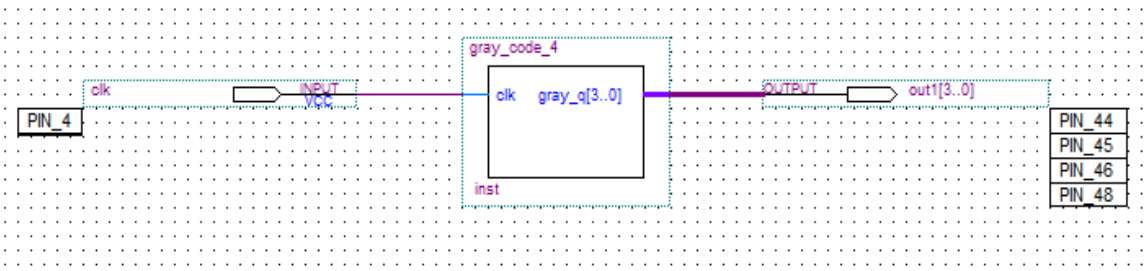

Figure 5: Four-Bit Gray Code Counter Digital Circuit

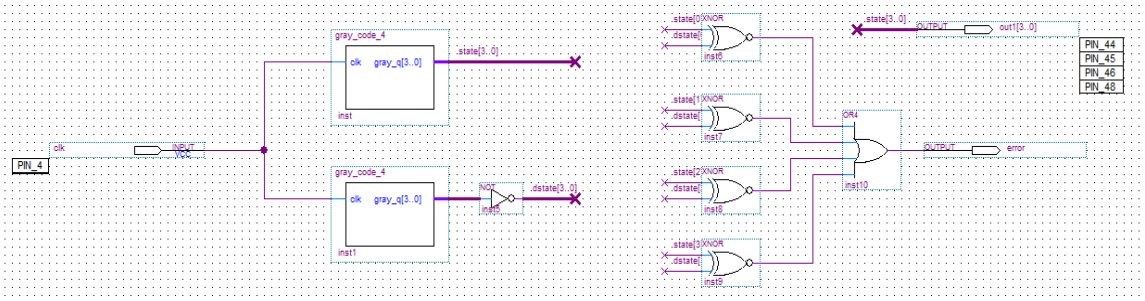

Figure 6: Dual Four-Bit Gray Code Counter with Error Detection

The binary counter and gray code counter allowed for the power consumption to be measured from a change in the number of bits that switched state (*P* and *n* in equation 1, respectively). This would show that there is an advantage to choosing one digital circuit over another. The power consumed by the dual rail counter was measured at various voltage levels to show that an increase in the number of bits that switch state is desirable with a decrease in the supply voltage (*P*, *n* and *V* in equation 1, respectively).

Based on equation 1, it is expected that the binary code counter will consume more power than the gray code counter. Also, since the supply voltage is squared, it is expected that the dual rail gray code counter will consume more power than the binary

code or gray code counters at 5 V but consume less power than them as the supply voltage is lowered to the dual rail counter.

Chapter 5: Parameters

In the experiment outlined, it may appear as if some of the parameters were arbitrarily chosen. Prior to this experiment, others were done that were inconclusive or had other issues (cost, lack of equipment, etc.) but observations were made nonetheless. The other experiments are not discussed in detail here but relevant portions are provided to show how the parameters for this experiment were chosen. The other experiments used the same CPLDs as this experiment.

One of the first attempts was to build a full product that would control the clock frequency, measure the current, check for errors and display the results. A microcontroller was used to operate the CPLD, including its clock. However, the maximum clock frequency that could be generated was 100 KHz and this was too slow to show any change in power consumption. The only faster clocks on hand were the 27 and 50 MHz oscillators on the DE2 Board. Both of these were sufficient but the 50 MHz clock showed the results more clearly and thus was chosen as the clock for this experiment.

Another test would output the results to external LEDs. The current consumption change at each state would be measured and it would be deduced that the current

behavior of the LEDs would reflect the current behavior of the device-internal flip-flops but on a larger, measureable scale. During this test, it was observed that the CPLDs would brownout or otherwise ceases to operate with any relation to the programmed circuit at 3.78 V and lower. The stopping point of 3.8 V was selected since it was known that operating the device below this voltage would not be possible and the results below this voltage would be irrelevant.

Since the beginning of this project, the parameter of a 0.1 V step was used. This step was chosen arbitrarily and was sufficient for this experiment.

The number of trials was arbitrarily selected to be five. When small, insignificant differences in power consumption from trial to trial were observed, this number was kept.

Chapter 6: Experiment Results

All trials for each device yielded very similar results. Additionally, the two similar devices yielded approximately the same results. The statistics of the results are shown below in Table 1 through Table 6.

Voltage Step (V)	Average Current (Multi-meter) (A)	Minimum Current (Multi-meter) (A)	Maximum Current (Multi-meter) (A)	Average Current (Power Supply) (A)	Minimum Current (Power Supply) (A)	Maximum Current (Power Supply) (A)	Average Power (Power Supply) (W)	Minimum Power (Power Supply) (W)	Maximum Power (Power Supply) (W)
5.0	0.0451	0.045	0.046	0.0445	0.044	0.045	0.22	0.22	0.22
4.9	0.043	0.043	0.043	0.0425	0.042	0.043	0.21	0.21	0.21
4.8	0.041	0.041	0.041	0.0405	0.04	0.041	0.19	0.19	0.2
4.7	0.039	0.039	0.039	0.0385	0.038	0.039	0.18	0.18	0.18
4.6	0.037	0.037	0.037	0.0365	0.036	0.037	0.17	0.17	0.17
4.5	0.0354	0.035	0.036	0.035	0.035	0.035	0.16	0.16	0.16
4.4	0.034	0.034	0.034	0.033	0.033	0.033	0.15	0.15	0.15
4.3	0.032	0.032	0.032	0.0319	0.031	0.032	0.14	0.14	0.14
4.2	0.031	0.031	0.031	0.0302	0.03	0.031	0.13	0.13	0.13
4.1	0.0295	0.029	0.03	0.0292	0.029	0.03	0.12	0.12	0.12
4.0	0.0285	0.028	0.029	0.0277	0.027	0.028	0.11	0.11	0.11
3.9	0.0275	0.027	0.028	0.0271	0.026	0.028	0.105	0.1	0.11
3.8	0.0269	0.026	0.028	0.0263	0.025	0.027	0.1	0.1	0.1

Table 1: Four-Bit Binary Counter, EPM064 Devices

Voltage Step (V)	Average Current (Multi-meter) (A)	Minimum Current (Multi-meter) (A)	Maximum Current (Multi-meter) (A)	Average Current (Power Supply) (A)	Minimum Current (Power Supply) (A)	Maximum Current (Power Supply) (A)	Average Power (Power Supply) (W)	Minimum Power (Power Supply) (W)	Maximum Power (Power Supply) (W)
5.0	0.0635	0.063	0.064	0.0635	0.063	0.064	0.315	0.31	0.32
4.9	0.0598	0.059	0.061	0.0594	0.058	0.06	0.29	0.29	0.29
4.8	0.0565	0.056	0.057	0.0555	0.055	0.056	0.27	0.27	0.27
4.7	0.0533	0.053	0.054	0.0525	0.052	0.053	0.249	0.24	0.25
4.6	0.0505	0.05	0.051	0.0495	0.049	0.05	0.23	0.23	0.23
4.5	0.0475	0.047	0.048	0.047	0.047	0.047	0.21	0.21	0.21
4.4	0.0454	0.045	0.046	0.0445	0.044	0.045	0.196	0.19	0.2
4.3	0.043	0.043	0.043	0.0425	0.042	0.043	0.18	0.18	0.18
4.2	0.0411	0.041	0.042	0.0405	0.04	0.041	0.17	0.17	0.17
4.1	0.0395	0.039	0.04	0.0385	0.038	0.039	0.16	0.16	0.16
4.0	0.0375	0.037	0.038	0.037	0.037	0.037	0.15	0.15	0.15
3.9	0.036	0.036	0.036	0.0354	0.035	0.036	0.14	0.14	0.14
3.8	0.0342	0.034	0.035	0.0335	0.033	0.034	0.13	0.13	0.13

Table 2: Four-Bit Binary Counter, EPM128 Devices

Voltage Step (V)	Average Current (Multi-meter) (A)	Minimum Current (Multi-meter) (A)	Maximum Current (Multi-meter) (A)	Average Current (Power Supply) (A)	Minimum Current (Power Supply) (A)	Maximum Current (Power Supply) (A)	Average Power (Power Supply) (W)	Minimum Power (Power Supply) (W)	Maximum Power (Power Supply) (W)
5.0	0.0426	0.042	0.043	0.042	0.042	0.042	0.21	0.21	0.21
4.9	0.0406	0.04	0.041	0.04	0.04	0.04	0.196	0.19	0.2
4.8	0.0386	0.038	0.039	0.038	0.038	0.038	0.18	0.18	0.18
4.7	0.0369	0.036	0.037	0.036	0.036	0.036	0.17	0.17	0.17
4.6	0.035	0.035	0.035	0.0341	0.034	0.035	0.16	0.16	0.16
4.5	0.0332	0.033	0.034	0.0328	0.032	0.033	0.15	0.15	0.15
4.4	0.032	0.032	0.032	0.031	0.031	0.031	0.14	0.14	0.14
4.3	0.0302	0.03	0.031	0.0299	0.029	0.03	0.13	0.13	0.13
4.2	0.0291	0.029	0.03	0.0285	0.028	0.029	0.12	0.12	0.12
4.1	0.0279	0.027	0.029	0.0275	0.027	0.028	0.11	0.11	0.11
4.0	0.027	0.026	0.028	0.0265	0.026	0.027	0.105	0.1	0.11
3.9	0.0263	0.025	0.027	0.0255	0.025	0.026	0.1	0.1	0.1
3.8	0.0254	0.024	0.026	0.0248	0.024	0.026	0.095	0.09	0.1

Table 3: Four-Bit Gray Code Counter, EPM064 Devices

Voltage Step (V)	Average Current (Multi-meter) (A)	Minimum Current (Multi-meter) (A)	Maximum Current (Multi-meter) (A)	Average Current (Power Supply) (A)	Minimum Current (Power Supply) (A)	Maximum Current (Power Supply) (A)	Average Power (Power Supply) (W)	Minimum Power (Power Supply) (W)	Maximum Power (Power Supply) (W)
5.0	0.0612	0.061	0.062	0.0605	0.06	0.061	0.3	0.3	0.3
4.9	0.0571	0.057	0.058	0.0565	0.056	0.057	0.279	0.27	0.28
4.8	0.0535	0.053	0.054	0.0529	0.052	0.053	0.255	0.25	0.26
4.7	0.0505	0.05	0.051	0.0499	0.049	0.05	0.235	0.23	0.24
4.6	0.0475	0.047	0.048	0.047	0.047	0.047	0.219	0.21	0.22
4.5	0.0452	0.045	0.046	0.0445	0.044	0.045	0.2	0.2	0.2
4.4	0.0426	0.042	0.043	0.0421	0.042	0.043	0.185	0.18	0.19
4.3	0.0405	0.04	0.041	0.04	0.04	0.04	0.17	0.17	0.17
4.2	0.0387	0.038	0.039	0.038	0.038	0.038	0.16	0.16	0.16
4.1	0.037	0.037	0.037	0.0365	0.036	0.037	0.15	0.15	0.15
4.0	0.0355	0.035	0.036	0.035	0.035	0.035	0.14	0.14	0.14
3.9	0.034	0.034	0.034	0.033	0.033	0.033	0.13	0.13	0.13
3.8	0.0325	0.032	0.033	0.0315	0.031	0.032	0.12	0.12	0.12

Table 4: Four-Bit Gray Code Counter, EPM128 Devices

Voltage Step (V)	Average Current (Multi-meter) (A)	Minimum Current (Multi-meter) (A)	Maximum Current (Multi-meter) (A)	Average Current (Power Supply) (A)	Minimum Current (Power Supply) (A)	Maximum Current (Power Supply) (A)	Average Power (Power Supply) (W)	Minimum Power (Power Supply) (W)	Maximum Power (Power Supply) (W)
5.0	0.0485	0.048	0.049	0.0475	0.047	0.048	0.24	0.24	0.24
4.9	0.0462	0.046	0.047	0.0455	0.045	0.046	0.22	0.22	0.22
4.8	0.0439	0.043	0.044	0.0435	0.043	0.044	0.21	0.21	0.21
4.7	0.0416	0.041	0.042	0.0415	0.041	0.042	0.195	0.19	0.2
4.6	0.0397	0.039	0.04	0.0395	0.039	0.04	0.18	0.18	0.18
4.5	0.038	0.038	0.038	0.0375	0.037	0.038	0.17	0.17	0.17
4.4	0.0361	0.036	0.037	0.0358	0.035	0.036	0.16	0.16	0.16
4.3	0.035	0.035	0.035	0.034	0.034	0.034	0.15	0.15	0.15
4.2	0.0335	0.033	0.034	0.033	0.032	0.034	0.14	0.14	0.14
4.1	0.033	0.032	0.034	0.032	0.031	0.033	0.13	0.13	0.13
4.0	0.032	0.031	0.033	0.031	0.03	0.032	0.125	0.12	0.13
3.9	0.0316	0.03	0.034	0.0308	0.029	0.033	0.12	0.11	0.13
3.8	0.032	0.029	0.035	0.032	0.029	0.035	0.12	0.11	0.13

Table 5: Dual Four-Bit Gray Code Counter with Error Detection, EPM064 Devices

Voltage Step (V)	Average Current (Multi-meter) (A)	Minimum Current (Multi-meter) (A)	Maximum Current (Multi-meter) (A)	Average Current (Power Supply) (A)	Minimum Current (Power Supply) (A)	Maximum Current (Power Supply) (A)	Average Power (Power Supply) (W)	Minimum Power (Power Supply) (W)	Maximum Power (Power Supply) (W)
5.0	0.0665	0.066	0.067	0.0655	0.065	0.066	0.33	0.33	0.33
4.9	0.0625	0.062	0.063	0.0615	0.061	0.062	0.3	0.3	0.3
4.8	0.0585	0.058	0.059	0.0581	0.057	0.059	0.28	0.28	0.28
4.7	0.05558	0.055	0.056	0.0545	0.054	0.055	0.26	0.26	0.26
4.6	0.0525	0.052	0.053	0.0515	0.051	0.052	0.24	0.24	0.24
4.5	0.0495	0.049	0.05	0.0491	0.049	0.05	0.22	0.22	0.22
4.4	0.0474	0.046	0.048	0.0465	0.046	0.047	0.205	0.2	0.21
4.3	0.0446	0.044	0.045	0.0445	0.044	0.045	0.19	0.19	0.19
4.2	0.0429	0.042	0.043	0.0421	0.042	0.043	0.18	0.18	0.18
4.1	0.0413	0.041	0.042	0.0405	0.04	0.041	0.17	0.17	0.17
4.0	0.04	0.04	0.04	0.0388	0.037	0.039	0.16	0.16	0.16
3.9	0.0384	0.038	0.039	0.0378	0.037	0.038	0.15	0.15	0.15
3.8	0.037	0.037	0.037	0.036	0.036	0.036	0.14	0.14	0.14

Table 6: Dual Four-Bit Gray Code Counter with Error Detection, EPM128 Devices

The results do verify the hypothesis. The binary counter consumed more power at each voltage step than the gray code counter. Additionally, the dual rail gray code counter with error detection consumed the most power at each voltage step. This was true for both models of the device. This information is shown graphically in Figure 7 through Figure 10 below.

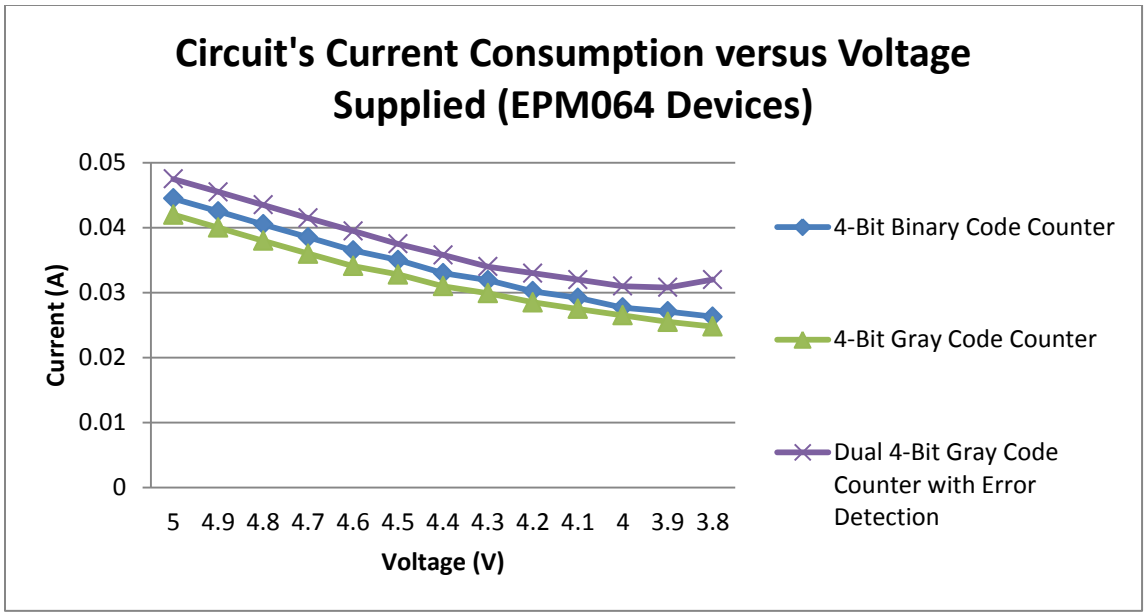

Figure 7: Circuit's Current Consumption versus Voltage Supplied (EPM064 Devices)

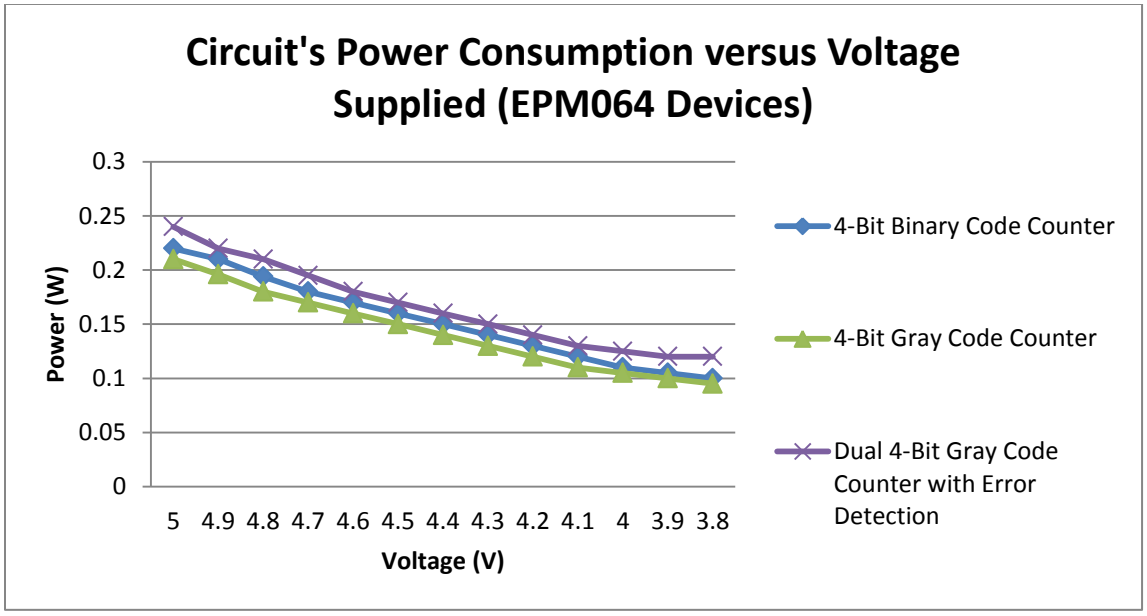

Figure 8: Circuit's Power Consumption versus Voltage Supplied (EPM064 Devices)

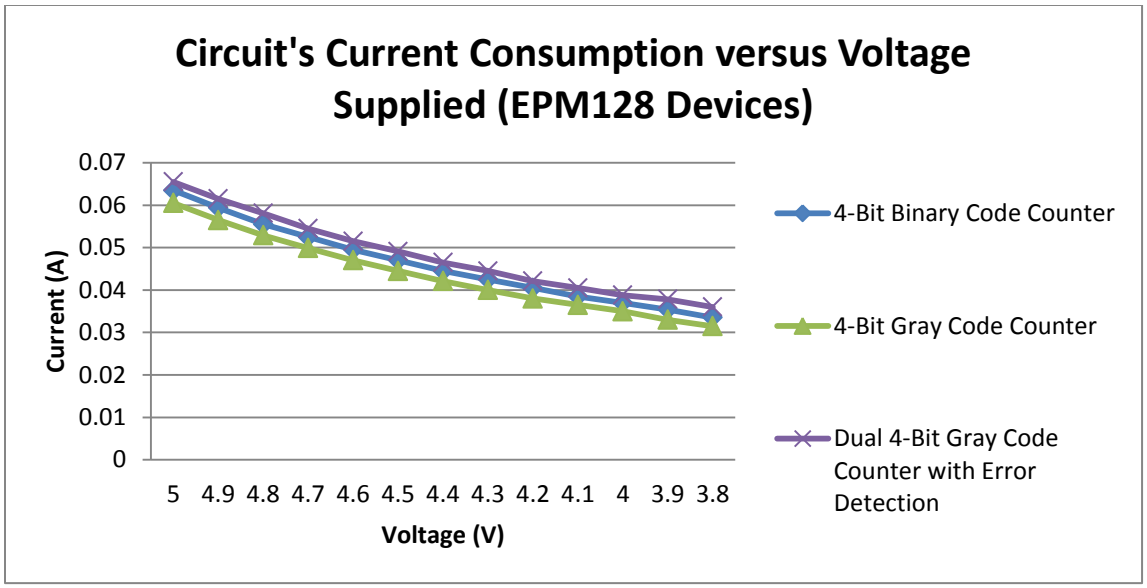

Figure 9: Circuit's Current Consumption versus Voltage Supplied (EPM128 Devices)

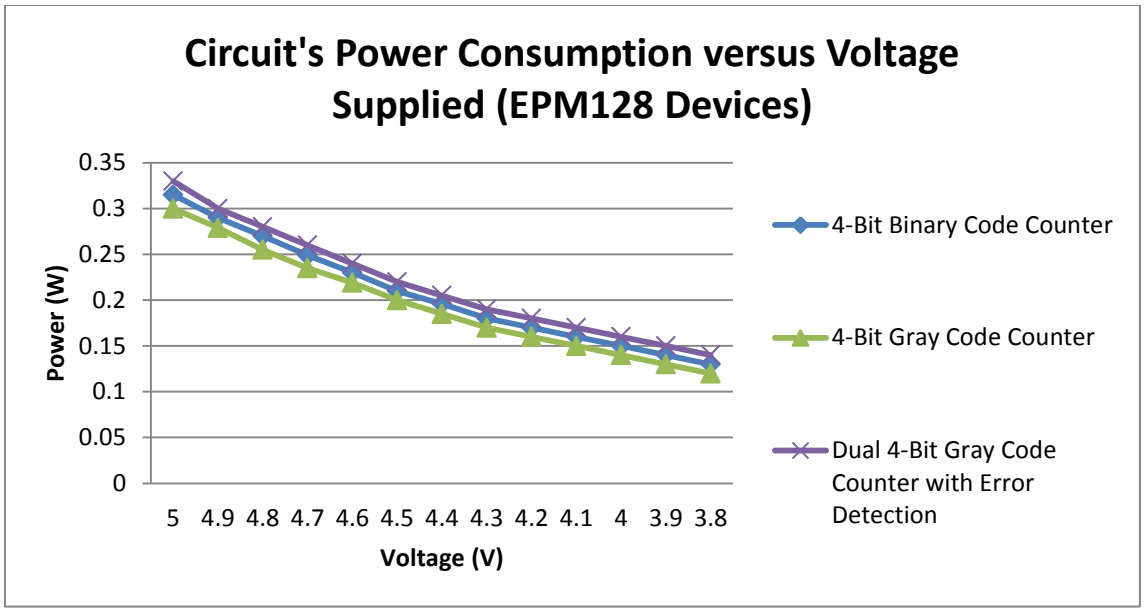

Figure 10: Circuit's Power Consumption versus Voltage Supplied (EPM128 Devices)

The two plots in Figure 11 and Figure 12 below show the power consumption of the dual rail gray code counter with error detection at various voltages versus the binary

and gray code counters at 5 V. As can be seen, at a point, not too far below 5 V, the dual rail counter consumes approximately the same power as its single counter counterpart.

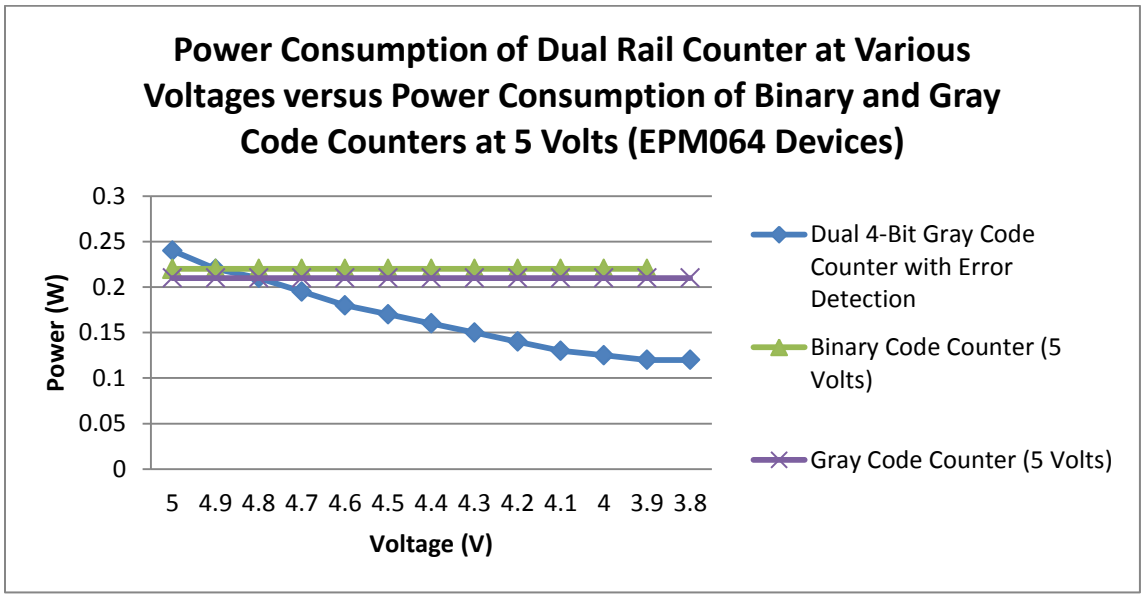

Figure 11: Power Consumption of Dual Rail Counter at Various Voltages versus Power Consumption of Binary and Gray Code Counters at 5 V (EPM064 Devices)

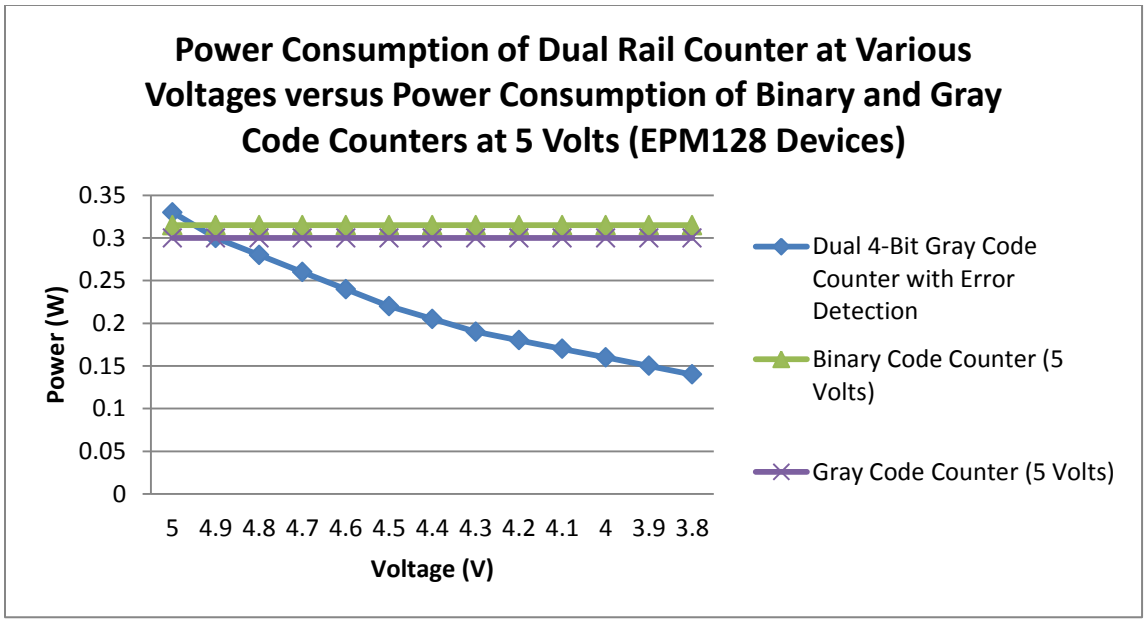

Figure 12: Power Consumption of Dual Rail Counter at Various Voltages versus Power Consumption of Binary and Gray Code Counters at 5 V (EPM128 Devices)

Chapter 7: Automated Approach:

This experiment outlined a general approach for testing the power consumption of fault-tolerant architectures. This approach can be automated to provide a fast, accurate and repeatable way of testing different devices and different digital circuits. Much of the design work for such automation has been done and will be briefly discussed.

Figure 13 shows a block diagram of the automation.

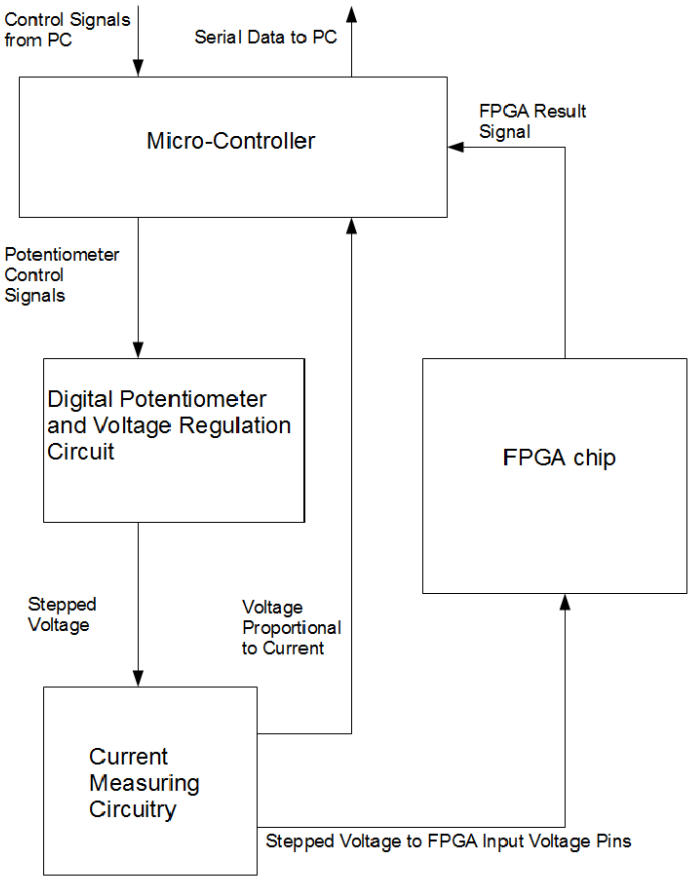

Figure 13: Block Diagram of the Automated Approach

The voltage is controlled using a digital potentiometer and voltage regulator. The potentiometer fills the role of R_2 in Figure 14 below, which uses a LM317 variable voltage regulator to control V_{out}. If R_1 is chosen to be 240 Ohms then a 5k digital potentiometer with 256 steps can generate the needed voltages. The output voltage is calculated from [8]

(Equation 2) $V_{out} = 1.25(R_1/R_2) * I_{adj} * R_2$

Where I_{adj} is held to under 100uA and is small enough to be ignored even with large values of R_2 [8]. Tests were done and this provided adequate control of the voltage. Details on wiring and using the digital potentiometer were found on its datasheet [9].

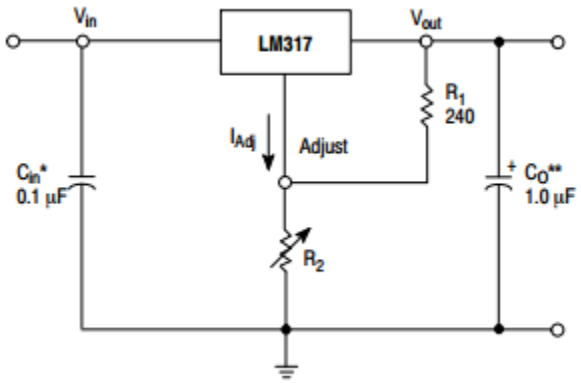

Figure 14: LM317 Circuit Diagram [8]

Measuring the current is accomplished using a shunt resistor. Tests used a 5.1 Ohm, 10 W resistor and gave results with 5 mA of the voltage measured by a Fluke 115 multi-meter. The microcontroller measured the voltage drop across the resistor to calculate the current. The foremost problems encountered using this method were the possibility of high voltages being measured by the microcontroller, which would damage it, and the possibility of the microcontroller consuming too much current and giving inaccurate results. These problems are solved using two inverting amplifiers with large resistors to half the voltage that the microcontroller measures [10]. A schematic is shown in Figure 15 below.

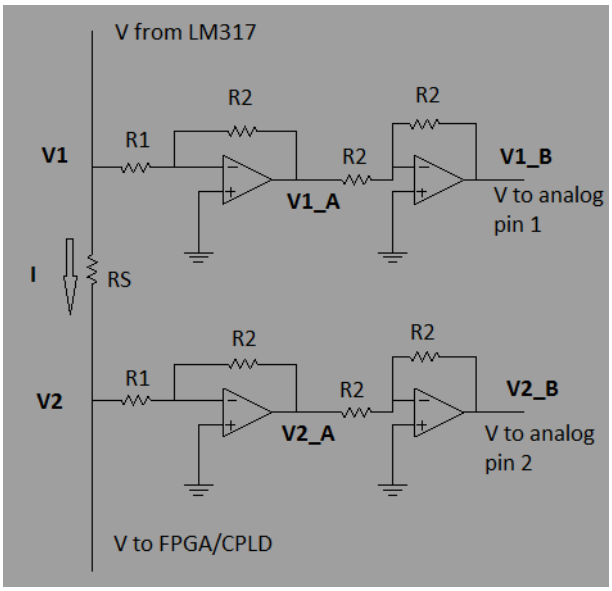

Figure 15: Current Measurement Circuit Diagram

The values selected for R_1 is 200 KOhms and R_2 is selected to be 100 KOhms and are large enough to minimize the current drawn by the microcontroller. Tests were done using this approach with acceptable results. Details on wiring and using the op-amp components were found on its datasheet [11]. This method is used over commercial products because current measurement integrated circuits are expensive and none could be found that specialized in measuring current in the milliamps region.

These are the major building blocks. The microcontroller needs to have enough pins to control the FPGA, measure the current, generate the clock and monitor for errors.

Chapter 8: Conclusion and Future Work

As can be seen from the results previously discussed, it is true that there are advantages to choosing one digital circuit over another. Additionally, it was shown that fault tolerant digital circuits, if operated at a lower voltage, would consume less power than their non-fault tolerant counterparts operating at nominal voltage.

This experiment only covered the preliminary and proof-of-concept work. Future work will investigate the fault-tolerant circuits more heavily and will focus on maintaining the functionality of the device even at lower operating voltages. Additionally, it will monitor the number of errors occurring versus the change in voltage to establish the functionality of the digital circuit, both with and without fault-tolerance, at various operating voltages.

In this experiment, devices that were easily mounted to breadboards and cheap were used; however, these devices are 5 V devices and small changes in voltage will have large impacts on its power consumption. More modern devices are manufactured to operate at lower voltages, some as low as 0.9 V [12]. Though these newer devices can be relatively cheap, they cannot be cheaply or easily mounted on a breadboard for easy pin access. Thus, future work will be more dedicated to these lower voltage devices and

investigating if the same results that were found for MAX 7000S CPLDs can be applied to CPLDs and FPGAs in general.

Lastly, future work will move towards minimizing the drawbacks of fault-tolerant architectures which include size and weight considerations and attempt to establish guidelines for choosing a fault-tolerant architecture over a non-fault-tolerant one.

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