Institutionen för systemteknik
Department of Electrical Engineering

Examensarbete

Implementation of a Low-Cost Analog-to-Digital Converter for Audio Applications Using an FPGA

Examensarbete utfört i Elektroniksystem
vid Tekniska högskolan vid Linköpings universitet
av

Johan Hellman

LiTH-ISY-EX--13/4711--SE

Linköping 2013

Linköpings universitet
TEKNISKA HÖGSKOLAN

Department of Electrical Engineering
Linköpings universitet
SE-581 83 Linköping, Sweden

Linköpings tekniska högskola
Linköpings universitet
581 83 Linköping

Implementation of a Low-Cost Analog-to-Digital Converter for Audio Applications Using an FPGA

Examensarbete utfört i Elektroniksystem
vid Tekniska högskolan vid Linköpings universitet
av

Johan Hellman

LiTH-ISY-EX--13/4711--SE

Handledare: **Erik Lindahl**
Actiwave AB

Examinator: **Kent Palmkvist**
ISY, Linköpings universitet

Linköping, 9 september 2013

Avdelning, Institution
Division, Department

Elektroniksystem
Department of Electrical Engineering
SE-581 83 Linköping

Datum
Date

2013-09-09

Språk
Language

☐ Svenska/Swedish
☒ Engelska/English
☐ _____

Rapporttyp
Report category

☐ Licentiatavhandling
☒ Examensarbete
☐ C-uppsats
☐ D-uppsats
☐ Övrig rapport
☐ _____

ISBN
—

ISRN
LiTH-ISY-EX--13/4711--SE

Serietitel och serienummer
Title of series, numbering

ISSN
—

URL för elektronisk version
http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-96009

Titel
Title

Implementering av en analog till digital omvandlare med låg kostnad för ljudapplikationer med hjälp av en FPGA

Implementation of a Low-Cost Analog-to-Digital Converter for Audio Applications Using an FPGA

Författare
Author

Johan Hellman

Sammanfattning
Abstract

The aim of this master's thesis is to implement an ADC (Analog-to-Digital Converter) for audio applications using external components together with an FPGA (Field-Programmable Gate Array). The focus is on making the ADC low-cost and it is desirable to achieve 16-bit resolution at 48 KS/s. Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.

This thesis presents two solutions: (1) a Σ-Δ (Sigma-Delta) converter with a first order passive loop-filter and (2) a Σ-Δ converter with a second order active loop-filter. The solutions have been designed on a PCB (Printed Curcuit Board) with a Xilinx Spartan-6 FPGA. Both solutions take advantage of the LVDS (Low-Voltage-Differential-Signaling) input buffers in the FPGA.

(1) achieves a peak SNDR (Signal-to-noise-and-distortion-ratio) of 62.3 dB (ENOB (Effective number of bits) 10.06 bits) and (2) achieves a peak SNDR of 80.3 dB (ENOB 13.04). (1) is very low-cost ($0.06) but is not suitable for high-precision audio applications. (2) costs $0.53 for mono audio and $0.71 for stereo audio and is comparable with the solution used today: an external ADC (PCM1807).

Nyckelord
Keywords

ADC, Sigma-Delta, FPGA, LVDS

Abstract

The aim of this master's thesis is to implement an ADC (Analog-to-Digital Converter) for audio applications using external components together with an FPGA (Field-Programmable Gate Array). The focus is on making the ADC low-cost and it is desirable to achieve 16-bit resolution at 48 KS/s. Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.

This thesis presents two solutions: (1) a Σ-Δ (Sigma-Delta) converter with a first order passive loop-filter and (2) a Σ-Δ converter with a second order active loop-filter. The solutions have been designed on a PCB (Printed Curcuit Board) with a Xilinx Spartan-6 FPGA. Both solutions take advantage of the LVDS (Low-Voltage-Differential-Signaling) input buffers in the FPGA.

(1) achieves a peak SNDR (Signal-to-noise-and-distortion-ratio) of 62.3 dB (ENOB (Effective number of bits) 10.06 bits) and (2) achieves a peak SNDR of 80.3 dB (ENOB 13.04). (1) is very low-cost ($0.06) but is not suitable for high-precision audio applications. (2) costs $0.53 for mono audio and $0.71 for stereo audio and is comparable with the solution used today: an external ADC (PCM1807).

Acknowledgments

First, I wish to thank Tina Kallio for her support during the thesis work. She has given me guidance and perspective in stressful moments.

I would also like to thank Dr. J Jacob Wikner for the help with Σ-Δ converters and Op-amps, and Dai Zhang, who helped me with FFT and providing me a FFT script.

Thanks to my examiner Kent Palmkvist for making this thesis possible.

At last (but not least), I would like to express my gratitude to Actiwave AB for this thesis and letting me do the work at their office in Stockholm. Especially thanks to my supervisor at Actiwave AB, Erik Lindahl, for all his help and support.

Stockholm, September 2013
Johan Hellman

Contents

Notation **ix**

1 Introduction **1**
1.1 Problem formulation 1
1.2 Related work 2
1.3 Thesis outline 2

2 System Overview **5**
2.1 The Complete System 5
2.2 The Xilinx Spartan-6 FPGA 6
2.2.1 LVDS 6
2.3 The Analog Audio Input Signal 7
2.4 Analog to Digital Converters Suited for Audio Applications 8

3 Theory **9**
3.1 Analog to Digital Conversion 9
3.1.1 Sampling 10
3.1.2 Quantization 11
3.1.3 Performance Metrics 11
3.2 Understanding Σ-Δ ADC 13
3.2.1 An Oversampling ADC 13
3.2.2 Noise Shaping 15
3.2.3 Higher Order Σ-Δ Modulators 17
3.2.4 Continuous-time Σ-Δ ADC 18
3.2.5 Inherent Anti-Aliasing Filter in CT Σ-Δ ADC 21
3.3 Non-idealities in CT Σ-Δ Modulator 22
3.3.1 Circuit Noise 22
3.3.2 Excess Loop Delay 23
3.3.3 Clock Jitter 23
3.3.4 Unequal Rise/Fall Time of DAC 24
3.3.5 Operational Amplifier Non-Idealities 24
3.4 Digital Filtering and Decimation 26
3.4.1 CIC filters 27

4 Test Setup **29**
4.1 Test Setup . . . 29
4.2 Control of Test Setup Quality . . . 30

5 Implementation of a Passive Σ-Δ Converter **33**
5.1 System Overview . . . 33
5.2 The Passive Σ-Δ Modulator . . . 34
5.2.1 Realization of the Passive Σ-Δ Converter . . . 36
5.2.2 Simulation Results . . . 37
5.2.3 Non-idealities in the Passive Σ-Δ modulator . . . 38
5.3 The CIC filter . . . 39
5.4 The FIR filter . . . 40
5.5 Results . . . 41
5.5.1 FPGA resources . . . 43
5.6 Discussion . . . 43

6 Implementation of a Second Order Σ-Δ Converter **45**
6.1 System Overview . . . 45
6.2 The 2^{nd} Order CT Σ-Δ Modulator . . . 46
6.2.1 Realization of the 2^{nd} order CT Σ-Δ modulator . . . 48
6.2.2 Simulation Results . . . 50
6.2.3 Non-idealities in the Δ-Σ modulator . . . 51
6.3 CIC filter . . . 52
6.4 FIR filter . . . 53
6.5 Results . . . 53
6.5.1 FPGA resources . . . 55
6.6 Discussion . . . 56

7 Conclusions and Future Work **57**
7.1 Conclusions . . . 57
7.2 Future Work . . . 59

List of Figures **61**

List of Tables **64**

Bibliography **65**

Notation

Notations

Notation	Denotation
A/D	Analog-to-digital
ADC	Analog-to-digital converter
ASIC	Application specific integrated curcuit
CIC	Cascaded-integrated-comb
CM	Common mode
CMT	Clock Management Tile
CT	Continuous time
DAC	Digital-to-analog converter
DCM	Digital clock manager
DSP	Digital signal processing
DT	Discrete time
DUT	Device under test
ELD	Excess loop delay
ENOB	Effective number of bits
FFT	Fast Fourier transform
FIR	Finite impulse response
FPGA	Field-programmable gate array
GBW	Gain-Bandwidth product
HDL	Hardware Description Language
HRZ	Half delay return to zero
I/O	Input/Output
ISI	Inter-symbol inteference
LUT	Look-up table
LVDS	Low voltage differential signaling
NRZ	Non-return to zero
NTF	Noise transfer function
OP-amp	Operational amplifier
OSR	Oversampling ratio

Notations

Notation	Denotation
PC	Personal computer
PCB	Printed curcuit board
PLL	Phase-locked loops
PSD	Power spectrum density
RAM	Random access memory
RMS	Root-mean-squared
RZ	Return to zero
S/s	Samples per second
Σ-Δ	Sigma-Delta
SCR	Switched capacitor resistor
SFDR	Spurious-free dynamic range
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
S/PDIF	Sony/Philips Digital Interconnect Format
SR	Slew rate
STF	Signal transfer function
SQNR	Signal-to-quantization-noise ratio
THD	Total harmonic distortion

1 Introduction

FPGA (Field-Programmable Gate Array) based solutions in consumer electronics have gained popularity due to low cost and high performance. The time-to-market is also shorter and the financial risk is lower compared to ASIC (Application Specific Integrated Circuit). One component that is missing in a low-cost FPGA is the ability to convert an analog signal to its digital counterpart.

An FPGA is an integrated curcuit, which have a large number of logic resources that can be configured to implement complex digital algorithms. The configuration can be done after manufacturing and is specified using a HDL (Hardware description language). This thesis will take advantage of the strength of the FPGA.

The aim of this thesis is to implement an ADC (Analog-to-Digital Converter) for audio applications using an FPGA together with external components. See figure 2.1 for an illustration of the complete system. Two solutions are presented: (1) a Σ-Δ converter with a first order passive loop-filter and (2) a Σ-Δ conveter with a second order active loop-filter. In both solutions, the FPGA will mainly be used to implement digital filters.

1.1 Problem formulation

This master thesis is done at Actiwave AB, a Swedish company which uses algorithms to make better sound quality in loudspeakers. The aim is to implement an ADC for audio applications using external components and an FPGA as illustrated in figure 2.1. Today, Actiwave AB uses an external ADC for conversion employing a 24-bit 99 dB SNR (93 dB SNDR) audio ADC (PCM1807) from Texas Instruments [21]. The main objective is to try eliminate the external ADC and replace it with external components and use the power of the FPGA. The goal is

therefore to make it low-cost and it is desirable to achieve CD quality, i.e. 16-bit resolution at 44.1 KS/s. In this thesis I will use 48 KS/s and the goal is to achieve 16-bit resolution. The term "low-cost", in this thesis, is only focusing on the external components. The goal is to keep the total cost of the external components at a minimum. However, the FPGA resources used should also be kept at a minimum.

Since large FPGA's have numerous I/O-pins, there are usually some unused pins and logic available in the FPGA that can be used for other purposes. This is taken advantage of, to make the ADC as low-cost as possible.

1.2 Related work

Analog to digital conversion is not a new topic; it has been along since the very start of mixed signal electronics. There have been several related work regarding ADC and FPGA's, e.g. Lattice [13] uses the LVDS buffer on the FPGA together with an RC-network to implement a simple Σ-Δ ADC. In 2004, Fabio Sousa et al. [19] presented a paper that also describes the implementation of Sigma-Delta that takes the advantage of the LVDS input buffers. In 2011, Axel Zimmerman et al. [27] presented a combined solution for ADC and DAC using an FPGA. The ADC is also employing the LVDS input buffer as a comparator.

However, none of the above presented papers have a focus on low-cost and they have not used any active components outside the FPGA.

1.3 Thesis outline

The outline of this master thesis is as follows:

- Chapter 2 describes a system overview, the Xilinx Spartan-6 FPGA and what type of ADC architecture that is suited for audio applications.
- In Chapter 3 the theory of analog to digital conversion is described and in particular the Σ-Δ ADC along with digital filtering.
- Chapter 5 describes the implementation of a first order Σ-Δ ADC using only passive components as a loop-filter.
- In Chapter 6 the implementation of the second order Σ-Δ ADC using an active filter as loop-filter is described.
- Chapter 7 presents the conclusions and what can be done in the future.

See Table 1.1 for an illustration of the outline of the thesis.

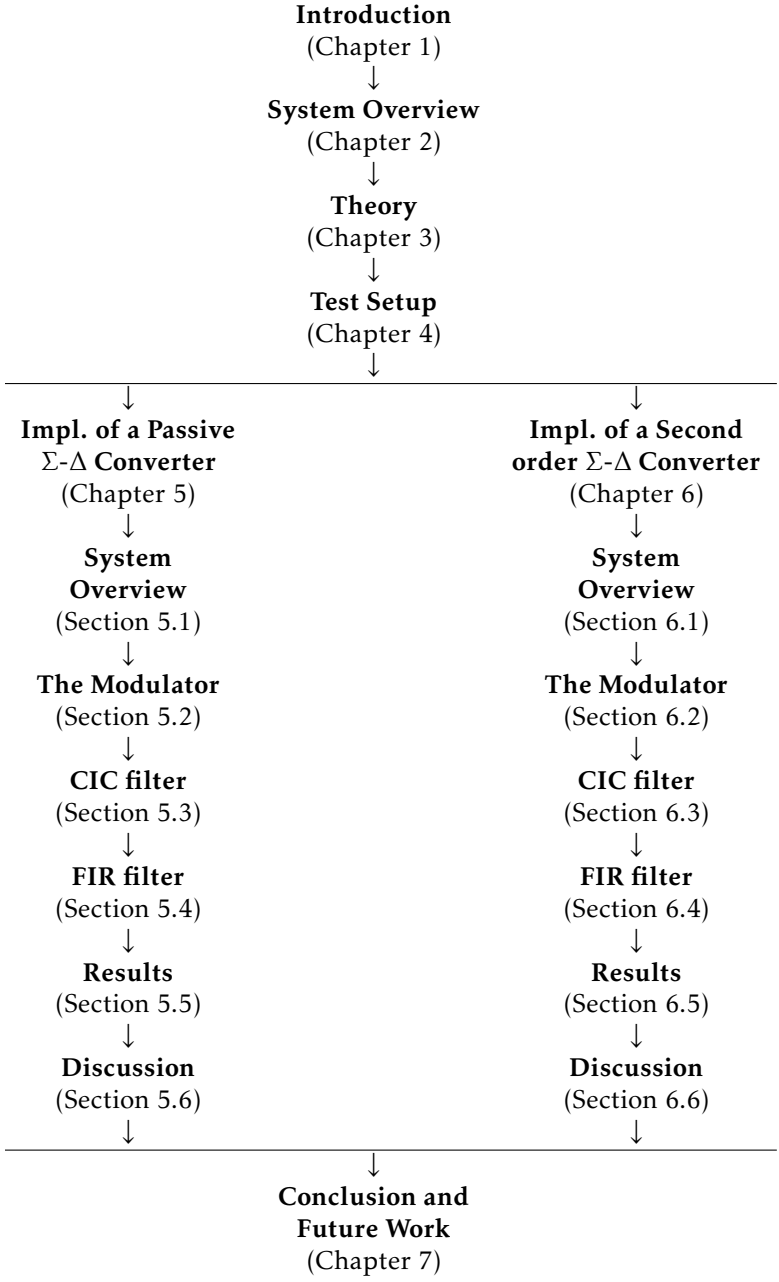


Table 1.1: *The outline of the thesis.*

2

System Overview

In this chapter, there will be a descirbed overview of the system along with the building blocks, such as the FPGA and LVDS input buffer. A discussion about the kind of ADC architecture that is suited for audio applications is also presented.

2.1 The Complete System

The ADC is implemented on a PCB (Printed Curcuit Board) containing a Xilinx XC6SLX9 (Spartan-6) FPGA in a TQG144 package and external components. See Figure 2.1 for the overview of the system. The external components could be anything, but in this thesis there will be a focus on low-cost. Therefore the total cost of the external components should be kept at a minimum.

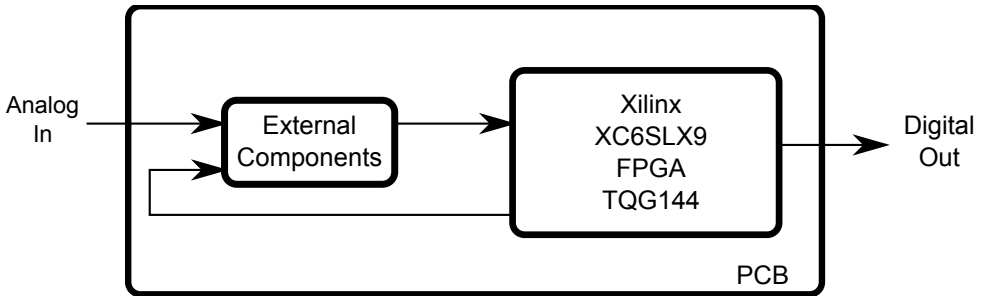


Figure 2.1: *The complete system.*

2.2 The Xilinx Spartan-6 FPGA

The FPGA contains resources according to Table 2.1 [25]. Each DSP48A1 slice contains an 18 × 18 bits multiplier, and adder and an accumulator. Every CMT (Clock Management Tile) is containing two DCMs (Digital Clock Managers) and one PLL (Phase-Locked Loops). The FPGA is using 3.3V single supply.

Block	Resource	Amount
	Logic Cells	9152
Configurable	**Slices**	1430
Logic Blocks	**Flip-Flops**	11440
(CLBs)	**Max Distributed RAM (Kb)**	90
Block RAM	**18 Kb**	32
Other	**DSP48A1 Slices**	16
	CMTs	2
	Total I/O Banks	4
	User I/O	102

Table 2.1: *Xilinx Spartan-6 XC6LX9 FPGA Features (TQG144 package).*

2.2.1 LVDS

The Spartan-6 FPGA is supporting the LVDS (Low Voltage Differential Signaling) standard. LVDS is a serial data communication channel transmitted over a differential pair allowing high speed and low power compared to single ended communication [18]. Figure 2.2 shows a simplified schematic of the LVDS driver and reciever. The driver sends a 3.5mA current through the 100Ω resistor, resulting in a 350mV swing. By changing the direction of the current results in a opposite polarity at the reciever [20]. The LVDS reciever is basically a high-speed comparator, allowing speed up to hundreds of megabits/s [18]. Since a lot of A/D converters are centered around one of several comparators, the LVDS buffer is a good component for this thesis.

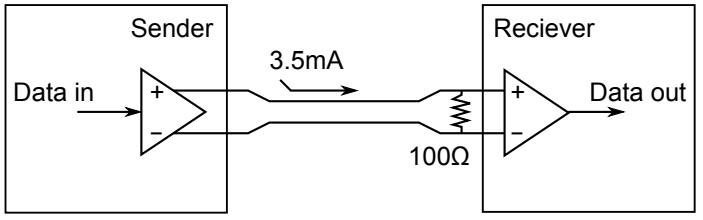


Figure 2.2: *Simplified LVDS schematic [18].*

Table 2.2 shows the LVDS input buffer specification of the Xilinx Spartan-6 [26]. One thing should be noted, the LVDS input buffer specification in Table 2.2 only specifies the LVDS input buffer so it complies with the LVDS standard. The LVDS

input buffer itself *could* work with larger V_{ID} and V_{ICM} ranges within the supply range.

V_{IN} Differential (V_{ID})		V_{IN} Common Mode (V_{ICM})	
Min [mV]	**Max [mV]**	**Max [V]**	**Min [V]**
100	600	0.3	2.35

Table 2.2: *LVDS I/O Standard Input Levels Xilinx Spartan-6.*

Some comparators have hysteresis [1], which prevents the comparator to switch states rapidly in a noisy environment. Figure 2.3 illustrates the transfer function of a comparator with hysteresis. Because the LVDS buffer is essentially a comparator, it may have hysteresis. According to [19], the hysteresis of the LVDS buffer in an Altera FPGA have a hysteresis less than 30mV. I will assume that the hysteresis of the LVDS buffer in Xilinx FPGA have the same order of magnitude.

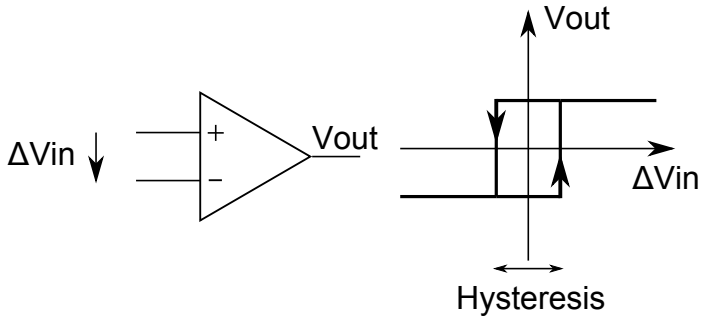


Figure 2.3: *Hysteresis of a comparator [1].*

2.3 The Analog Audio Input Signal

The input signal has to be characterized, in order to design the ADC suited for the particular input signal. The analog audio input signal, in this thesis, is assumed to have the specification according to Table 2.3.

Specification	Value
Amplitude (max)	$1.65V$ ($3.3V_{pp}$)
Bandwidth	$20Hz$ –$20KHz$

Table 2.3: *Analog audio input signal specification.*

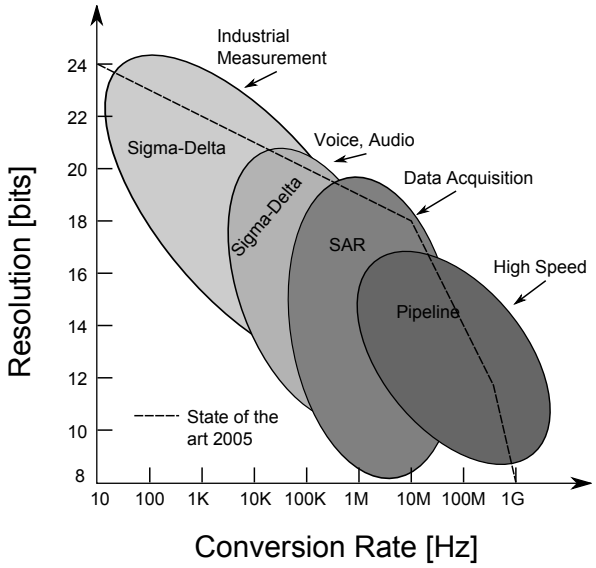


Figure 2.4: *Different ADC architectures and applications [11].*

2.4 Analog to Digital Converters Suited for Audio Applications

There are different kind of architectures of A/D-converters and there is often a tradeoff between resolution and the maximum signal bandwidth that can be converted. For example, Flash ADC are well suited for wide signal bandwidth, but with a moderate resolution. Audio applications have a limited signal bandwidth, due to the human ear which can only hear signals from 20Hz to 20KHz. ADI [11] classifies ADC applications into four market segments. These segments and their associated typical architectures is presented in Figure 2.4. According to this classification, Σ-Δ (Sigma-Delta) ADC is a good choice for audio applications.

The Σ-Δ ADC is an oversampling converter with quantization noise shaping. By using this technique, along with digital filtering, the Σ-Δ ADC can achieve resolution up to 24 bits. Therefore, they are very popular among high-precision audio applications [10]. Δ-Σ ADC is a feedback system with a filter in it's loop, placed before quantization. This filter can be either a discrete time (DT) or a continuous time (CT) filter, hence there are two classes of Σ-Δ ADC: Discrete time and Continuous time Σ-Δ ADC's. Discrete time Σ-Δ ADC are oftenly based on SC (Switched-Capacitor) filters, which is often a integrated curcuit and hard to get "off the shelf". Therefore my work will focus on Continuous Time Σ-Δ ADC. The operation of the Σ-Δ ADC will be described in Section 3.2.

3
Theory

In this chapter the fundamental operation of an ADC is described. Furthermore, it describes the basic operation of a Σ-Δ converter and in particualar the CT Σ-Δ converter. Since the Σ-Δ converter is a oversampling converter, there is a chapter about digital filtering and decimation (downsampling).

3.1 Analog to Digital Conversion

The main objective of an ADC is to convert an analog signal into its digital counterpart, so it can be further processed by digital circuits. An analog signal is in its nature continuous in both time and amplitude, while a digital signal is discrete in both time and amplitude. This process can be divided into two sections: Sampling (described in Section 3.1.1) and Quantization (described in Section 3.1.2). See Figure 3.1 for an illustration of the ADC system.

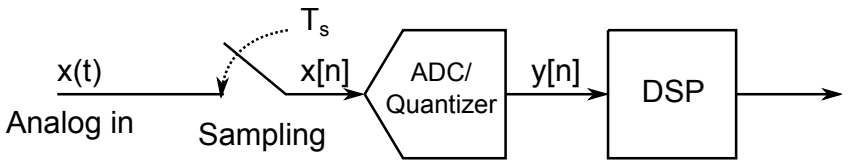


Figure 3.1: *From analog input signal, $x(t)$, to output, $y[n]$, which is later processed by e.g. a DSP [23].*

3.1.1 Sampling

Sampling is a process that convert a continuous time signal into a discrete time signal. The signal, $x(t)$, is sampled at a uniformly spaced time intervals, T_s (see Figure 3.2) [2]:

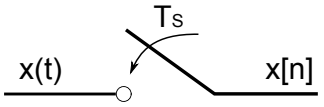


Figure 3.2: *The sampling process.*

$$x[n] = x(nT_s) \tag{3.1}$$

where $x[n]$ is the sampled signal. This can be seen as multiplying the signal with dirac pulses at nT_s [5]:

$$x_p(t) = x(t)p(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s) \tag{3.2}$$

where

$$p(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s) \tag{3.3}$$

and

$$\delta(t) = \begin{cases} 1, & t = 0 \\ 0, & t \neq 1 \end{cases} \tag{3.4}$$

The Fourier transform of the sampled function $x_p(t)$ is [5]:

$$X_p(\omega) = \frac{1}{2\pi} X(\omega) * P(\omega) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X(\omega - k\omega_s), \tag{3.5}$$

$$\omega_s = 2\pi f_s = \frac{2\pi}{T_s}.$$

One can see that the frequency components in $x(t)$ is reapeated every multiple of ω_s. To prevent aliasing and to fully reconstruct the signal, the Nyquist theorem has to be fulfilled [5]:

$$f_s > 2f_B, \tag{3.6}$$

where f_B is the bandwidth of the analog input signal. An anti-aliasing filter is usually placed before the sampling [2], to prevent this from happening. This is shown in Figure 3.3.

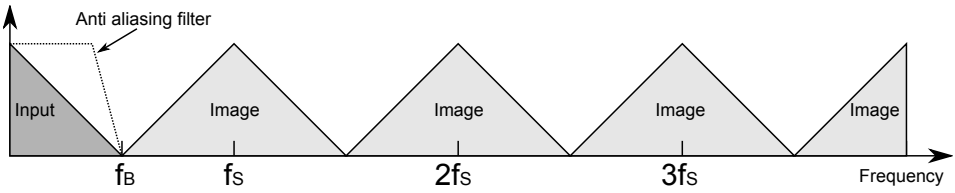


Figure 3.3: *x_p in the frequency domain [5].*

The Nyquist theorem sets a boundary for the sampling frequency. A/D-convertes that operates close to the boundary is called Nyquist-rate convertes and converters that operate at a much higher frequency is called oversampling ADCs. Oversampling ADCs are explained in Section 3.2.1.

3.1.2 Quantization

The analog signal must also be mapped to discrete levels. This is done by the quantization process. The wordlength, in number of bits N, decides the resolution of the ADC and the number of leves is 2^N. This is shown in Figure 3.4a with $N = 3$. The finite wordlength of the ADC results in a quantization error, Δ, which is bound between $-\frac{q}{2} < \Delta < +\frac{q}{2}$ where q is one LSB. The Δ-function is illustrated in Figure 3.4b. This quantization error is assumed to be white noise and uncorrelated with the input signal and is referred to as quantization noise. The total quantization noise power is (mean-squared) [5]:

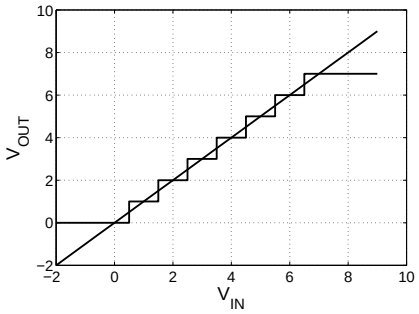
$$e_q^2 = \frac{1}{q} \int_{-q/2}^{+q/2} \Delta^2 \, d\Delta = \frac{q^2}{12}, \tag{3.7}$$

which is measured from DC to $f_s/2$. The power spectral density (PSD) for the quantization noise is [5]:

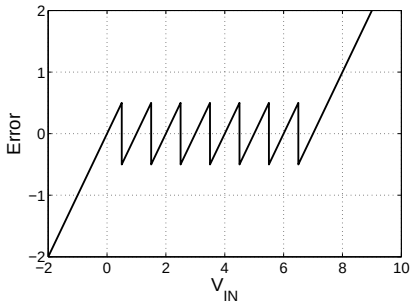
$$S_{e_q}(f) = \frac{e_q^2}{f_s/2}. \tag{3.8}$$

3.1.3 Performance Metrics

Performance metrics are used to characterize the ADC. The metrics can be divided in two categories: static and dynamic. Static metrics are analyzed in the time domain, while dynamic metrics are analyzed in the frequency domain [5]. In this thesis there will be focus on the dynamic metrics only. Below follows a presentation of the dynamic metrics used in this work.



(a) No quantization (straight line) and quantized signal.



(b) Error signal, $Error = Vout_{ideal} - Vout_{quantized}$.

Figure 3.4: *Illustration of quantization.*

SNR

SNR (Signal-to-Noise-Ratio) is defined as the ratio between the signal power and the noise power (excluding DC component) [5]:

$$SNR = 10log_{10}\left(\frac{S_{RMS}^2}{E_{RMS}^2}\right) \qquad [dB] \tag{3.9}$$

SQNR

SQNR (Signal-to-Quantization-Noise-Ratio) is, compared to SNR, only focusing on the noise generated by the quantizer (quantization noise) [5]:

$$SQNR = 10log_{10}\left(\frac{S_{RMS}^2}{E_{Q,RMS}^2}\right) \qquad [dB] \tag{3.10}$$

SNDR

SNDR (Signal-to-Noise-and-Distortion-Ratio) is, in contrast to SNR, also including the power of the distortion (excluding DC component) [5]:

$$SNDR = 10log_{10}\left(\frac{S_{RMS}^2}{E_{RMS}^2 + E_D^2}\right) \qquad [dB] \tag{3.11}$$

SNDR is sometimes referred to as SINAD or THD+N.

THD

THD (Total Harmonic Distortion) is defined as the ratio between the signal power and the power of all the harmonic distiortion [5]:

$$THD = 10log_{10}\left(\frac{S_{RMS}^2}{E_D^2}\right) \qquad [dB] \tag{3.12}$$

ENOB

ENOB (Effective-Number-of-Bits) is a measure of how many bits are above the noise floor. The ENOB formula is derived from the theoretical SNR of a N-bit ADC ($SNR = 6.02N + 1.76[dB]$), where SNR and N is substituted by SNDR and ENOB, respectively [5]:

$$ENOB = \frac{SNDR[dB] - 1.76}{6.02} \qquad [bits] \tag{3.13}$$

SFDR

SFDR (Spurious-Free-Dynamic-Range) is a defined as the ratio between the signal power and the power of the worst spurious signal [5]. This is illustrated in Figure 3.5, where dBFS stands for dB relative to the full-scale (FS) and dBc stands for dB relative to the carrier (c).

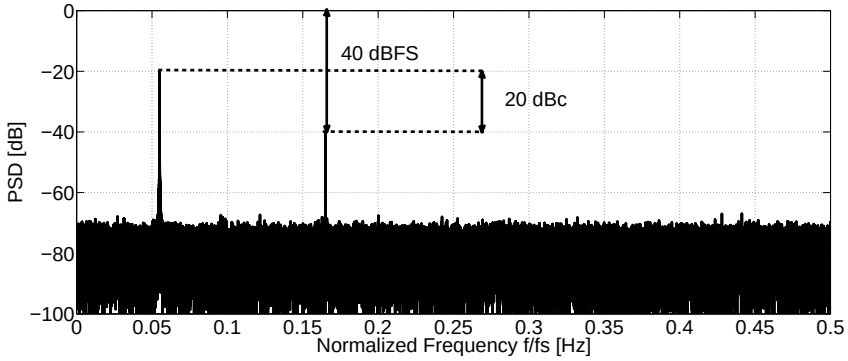


Figure 3.5: *Illustration of SFDR.*

3.2 Understanding Σ-Δ ADC

This section describes the basic operation of Σ-Δ converters.

3.2.1 An Oversampling ADC

Σ-Δ ADC is an oversampled A/D-converter which converts the signal in a much higher sampling frequency. The oversampling ratio (OSR) defined as [10]:

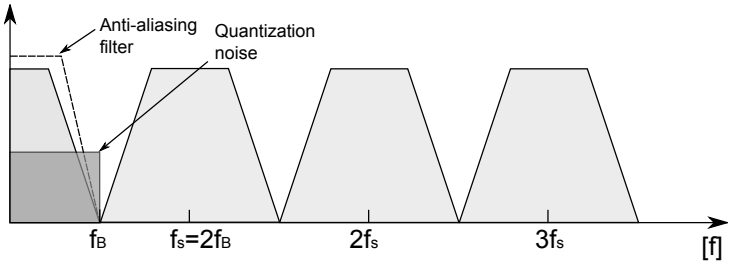
$$OSR = \frac{f_s}{2f_B}. \tag{3.14}$$

The benfits of the oversampled ADC is [10]:

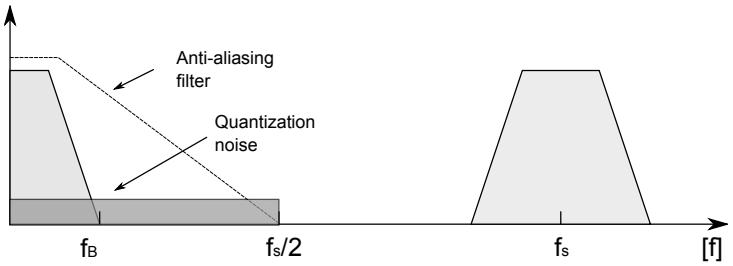
1. The quantization noise is spread over a wider frequency range. The total quantization noise remains the same, but the in-band noise is reduced which leads to a higher SQNR.

2. The anti-aliasing filter is relaxed.

This is shown in Figure 3.6.



(a) *Nyquist-rate ADC (OSR = 1).*



(b) *Oversampling ADC (OSR= 3).*

Figure 3.6: *Spectral proporties for Nyquist-rate and oversampling ADC [10].*

The in-band noise power for the oversampling ADC is derived as:

$$E_{q,OS} = \int_0^{f_B} S_{e_q,OS}(f)\,df = \int_0^{f_B} \frac{q^2}{12 f_s/2}\,df = \int_0^{f_B} \frac{q^2}{12 f_B OSR}\,df = \frac{q^2}{12 OSR}. \quad (3.15)$$

When applying a full-scale (FS) sine wave:

$$x(t) = \frac{q 2^N}{2} \sin(2\pi f t), \quad (3.16)$$

with the power (rms):

$$P_{sin} = \frac{q^2 2^{2N}}{8}, \quad (3.17)$$

the maximum SQNR for the oversampling ADC becomes:

$$SQNR_{OS} = 10log_{10}(\frac{P_{sin}}{E_q}) = 6.02N + 1.76 + 10log_{10}(OSR). \qquad [dB] \qquad (3.18)$$

For a comparison, a Nyquist-rate ADC with an $OSR = 1$, the maximum SQNR becomes:

$$SQNR_{Nyquist} = 6.02N + 1.76. \qquad [dB] \qquad (3.19)$$

The SQNR increases 3dB for every doubling of the OSR.

The oversampling ADC is usually followed by a digital low-pass filter which removes the out-of-band noise. The digital low-pass filter is followed by a decimator to get downsampled to the Nyquist-rate.

3.2.2 Noise Shaping

Σ-Δ ADCs also have the advantage of noise shaping. To illustrate this, Figure 3.7 shows a Σ-Δ modulator. It contains a loop filter, an ADC and a DAC. The sampling is done before the modulator, hence it's a discrete time Σ-Δ modulator [10].

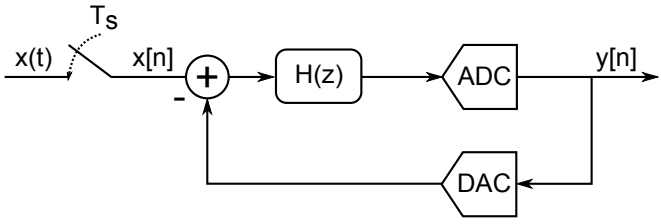


Figure 3.7: *A first order Σ-Δ discrete time modulator.*

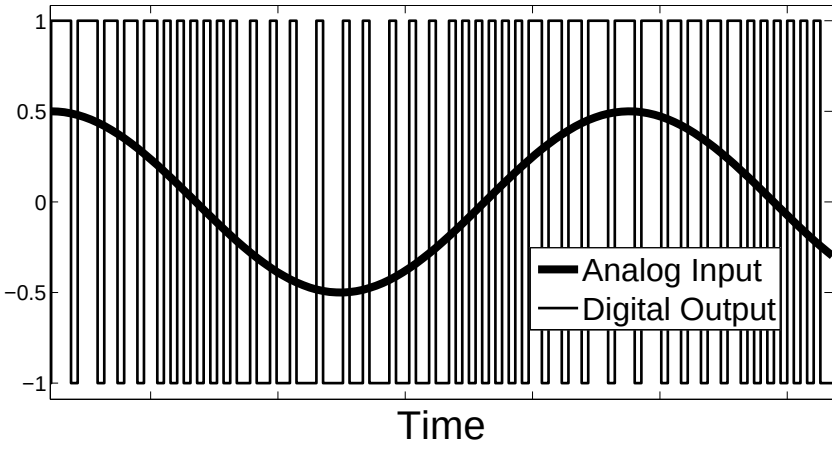


Figure 3.8: *Output waveform of a Σ-Δ converter with 1-bit quantizer (ADC).*

The output, y[n], of a 1-bit quantizer (ADC) is shown in Figure 3.8. A linearization of the Σ-Δ in the z-domain is shown in Figure 3.9. The ADC is replaced with an additive quantizaion noise, $E(z)$.

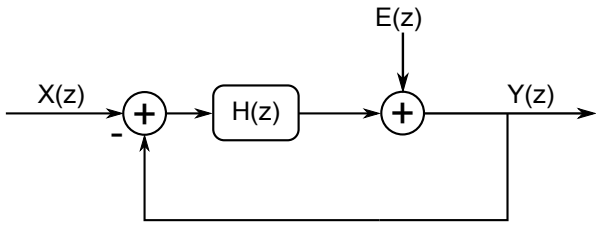


Figure 3.9: *A linearization of a first order Σ-Δ discrete time modulator in the z-domain.*

The transfer function becomes:

$$Y(z) = \frac{H(z)}{1 + H(z)} X(z) + \frac{1}{1 + H(z)} E(z) = STF(z)X(z) + NTF(z)E(z), \tag{3.20}$$

where STF and NTF stands for Signal Transfer Function and Noise Transfer Function, respectively. If the loop filter is:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}, \tag{3.21}$$

which is an accumulator/integrator, the STF and NTF becomes:

$$STF(z) = z^{-1}, \tag{3.22}$$

$$NTF(z) = 1 - z^{-1}. \tag{3.23}$$

According to Equation 3.22, the STF is a delay element. Equation 3.23 states that the NTF has a pole at $z = 0$ and a zero at $z = 1$ which corresponds to a high-pass filter. This means that the quantization noise is shaped. Again, the total quantization noise remains the same, but it gets pushed to higher frequencies. This means that the in-band quantization noise becomes lower, and thus, the SQNR becomes larger. This is illustrated in Figure 3.10.

The total in-band noise power for the first order Σ-Δ ADC is:

$$E_{q,\Sigma-\Delta} = \int_0^{f_B} S_{e_q,OS}(f)|NTF(z)|^2 \, df = \int_0^{f_B} \frac{q^2}{12 f_B OSR} |1 - e^{-j2\pi f/f_s}|^2 \, df \tag{3.24}$$

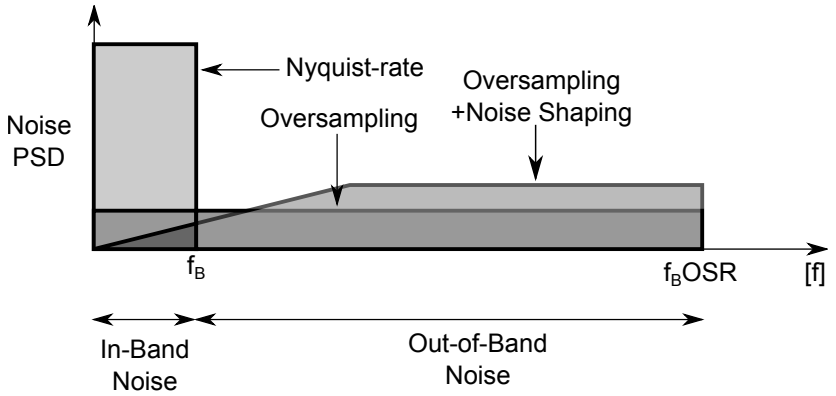


Figure 3.10: *Noise PSD for Nyquist-rate, oversampling and oversampling+noise-shaping (Σ-Δ) ADC's [10].*

If the OSR is high, this can be approximated by [10]:

$$E_{q,\Sigma-\Delta} \approx \int_0^{f_B} \frac{q^2}{12 f_B OSR} (2\sin(\pi f/f_s))^2 \, df = \frac{\pi^2 q^2}{36 OSR^3} \tag{3.25}$$

The SQNR for the first order Σ-Δ ADC becomes:

$$\begin{aligned} SQNR_{\Sigma-\Delta} &= 10log_{10}(\frac{P_{sin}}{E_{q,\Sigma-\Delta}}) = 10log_{10}(\frac{2^{2N}36OSR^3}{8\pi^2}) = \\ &= -3.41 + 6.02N + 30log_{10}(OSR) \qquad [dB] \end{aligned} \tag{3.26}$$

Hence, according to Equation 3.26 the SQNR imporves by 9 dB by doubling the OSR.

3.2.3 Higher Order Σ-Δ Modulators

By introducing more integrators into the loop filter, the modulator's order get increased. If an L^{th} order Σ-Δ modulator is designed, the NTF becomes [10]:

$$NTF_L(z) = (1 - z^{-1})^L. \tag{3.27}$$

This means that the in-band quantization noise gets more attenuated, and thus, increasing the SQNR. The maximum SQNR for a L^{th} order Σ-Δ modulator is [12]:

$$\begin{aligned} SQNR_L = 1.76 + 6.02N + (2L+1)10log_{10}(OSR) + \\ +10log_{10}(2L+1) - (2L)10log_{10}(\pi). \qquad [dB] \end{aligned} \tag{3.28}$$

Figure 3.11 shows the maxiumum SQNR for different Σ-Δ orders and OSR with a 1-bit quantizer.

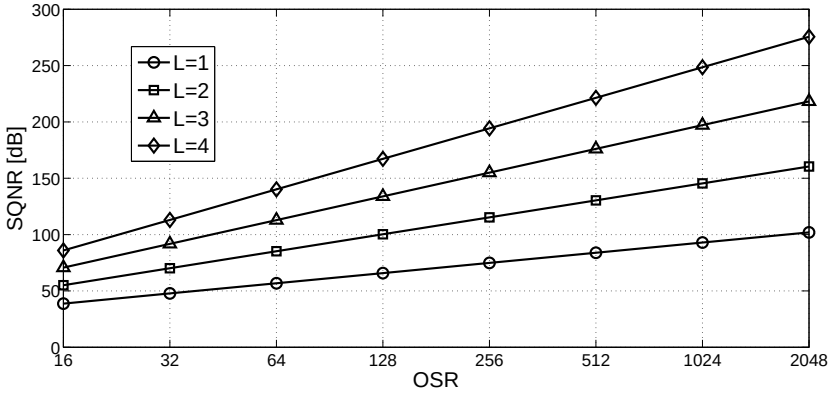


Figure 3.11: *Maximum SQNR for different Σ-Δ orders and OSR with a 1-bit quantizer*

For example, a 1-bit 2^{nd} order Σ-Δ with an OSR of 256 have an equivalent SQNR as a 18.8-bit Nyquist-rate ADC.

3.2.4 Continuous-time Σ-Δ ADC

By replacing the discrete-time (DT) loop filter by a continuous-time loop filter and perform the sampling inside the loop, one gets a continuous-time (CT) Σ-Δ modulator. See Figure 3.12.

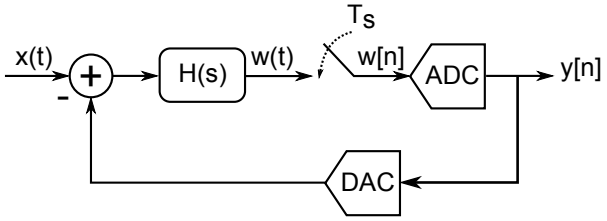


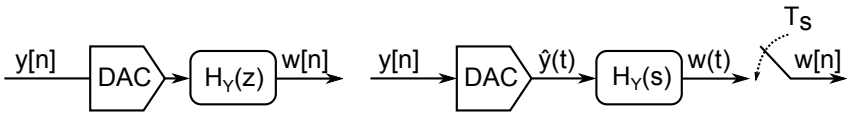
Figure 3.12: *Continuous-time Σ-Δ modulator.*

To design a CT Σ-Δ modulator, it is common to first design a DT Σ-Δ modulator and then find an equivalent CT Σ-Δ modulator [5]. The open-loop of the DT Σ-Δ modulator and CT Σ-Δ modulator is shown in Figure 3.13 [10].

The transfer function from $y[n]$ to $w[n]$ should be equivalent at each sampling instant for both the DT and CT case [10]. To find the equivalent loop filter (from $y[n]$ to $w[n]$), $H_Y(s)$, one can use the formula:

$$Z^{-1}\{H_Y(z)\} = L^{-1}\{H_{DAC}(s)H_Y(s)\}|_{t=nT_s}. \tag{3.29}$$

H_{DAC} is the transfer function of the DAC. The three main DAC pulses are non-return to zero (NRZ), return to zero (RZ) and half-delayed return to zero (HRZ).



(a) Open loop of DT Σ-Δ. *(b) Open loop of CT Σ-Δ.*

Figure 3.13: *Open loop of DT and CT Σ-Δ [10].*

The transfer function for these are:

$$H_{DAC}(s) = \frac{e^{-\alpha s} - e^{-\beta s}}{s}, \tag{3.30}$$

which is illustrated in Figure 3.14.

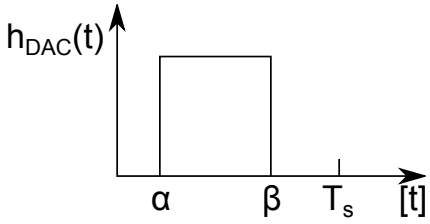


Figure 3.14: *H_{DAC} impulse response for NRZ, RZ and HRZ.*

α and β are constants according to Table 3.1 [10].

	α	β
NRZ	0	T_s
RZ	0	$0.5T_s$
HRZ	$0.5T_s$	T_s

Table 3.1: *α and β values for NRZ, RZ and HRZ DAC's.*

General Method of designing a Second order Discrete Time Σ-Δ Modulator and its Continuous Time Equivalent

A second order DT Σ-Δ modulator has an NTF:

$$NTF(z) = (1 - z^{-1})^2. \tag{3.31}$$

According to Equation 3.20 the loop filter becomes:

$$H(z) = \frac{1}{NTF(z)} - 1 = \frac{1}{(1 - z^{-1})^2} - 1 = \frac{z^{-1}}{(1 - z^{-1})} + \frac{z^{-1}}{(1 - z^{-1})^2}. \tag{3.32}$$

This is shown in Figure 3.15.

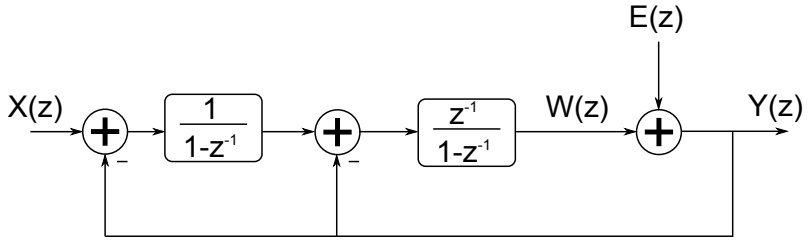


Figure 3.15: *A 2nd order DT Σ-Δ modulator in a feedback topology [10].*

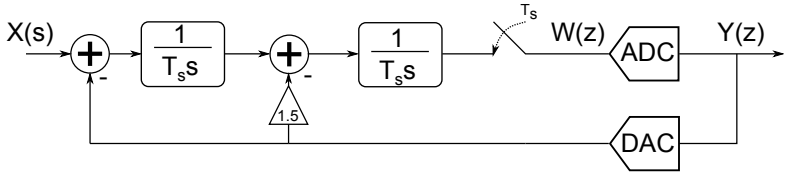
$H_Y(z)$ becomes:

$$H_Y(z) = \frac{W(z)}{Y(z)} = \frac{-2z+1}{(z-1)^2} \tag{3.33}$$

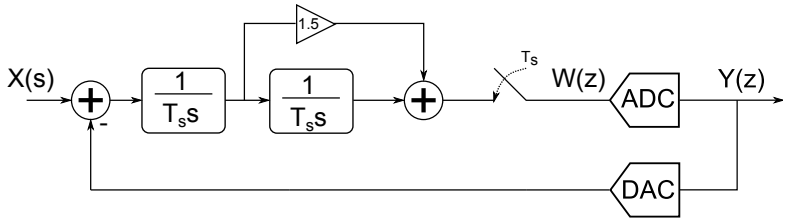
By using Equation 3.29 with NRZ DAC pulse, the CT equivalent becomes [10]:

$$H_Y(s) = \frac{-1.5T_s s - 1}{(T_s s)^2}. \tag{3.34}$$

This is illustrated in Figure 3.16a in feedback topology and in Figure 3.16b in feedforward topology.



(a) *Feedback topology.*



(b) *Feedforward topology.*

Figure 3.16: *A 2nd order CT Σ-Δ modulator.*

3.2.5 Inherent Anti-Aliasing Filter in CT Σ-Δ ADC

One benefit of the CT Σ-Δ is that it inherits an anti-aliasing filter. This eliminates an anti-aliasing filter in front of the CT Σ-Δ converter (which is necessary in the DT case). To illustrate this, a modified version of Figure 3.12 is illustrated in Figure 3.17 as in [17].

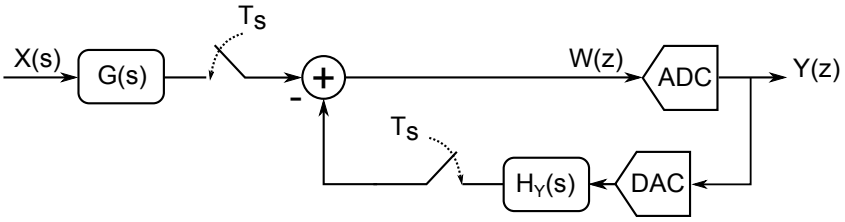


Figure 3.17: *A modified 2^{nd} order CT Σ-Δ converter.*

Where,

$$G(s) = \frac{1.5T_s s + 1}{(T_s s)^2} \tag{3.35}$$

and equivalent DT loop filter, $H_Y(z)$, from $Y(z)$ to $W(z)$ becomes, using Equation 3.29. The NTF becomes [17]:

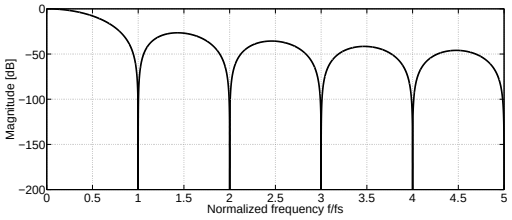
$$NTF(z) = \frac{1}{1 + H_Y(z)}. \tag{3.36}$$

The STF becomes [17]:

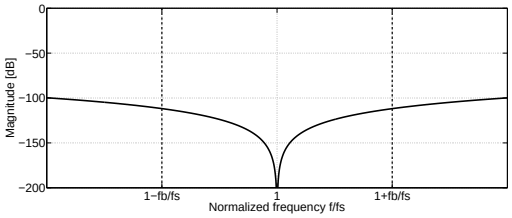
$$STF(s) = H(s)NTF(e^{sT_s}) = \frac{G(s)}{1 + H_Y(e^{sT_s})} \tag{3.37}$$

For a NRZ DAC, the STF magnitude response is illustrated in Figure 3.18a.

The signals that can be aliased into the in-band are located within $kf_s \pm f_B$, where k is an integer [17]. This is illustrated in Figure 3.18b, where $k = 1$. One can see that the aliasing bands are attenuated more than 100dB for a second order CT Σ-Δ modulator, in this example. Therefore, the CT Σ-Δ inherits the anti-aliasing filter.



(a) *Overview.*



(b) *Close up.*

Figure 3.18: *A 2nd order CT Σ-Δ STF.*

3.3 Non-idealities in CT Σ-Δ Modulator

3.3.1 Circuit Noise

There are different kind of noise sources present in a CT Σ-Δ modulator. Figure 3.19 shows a simplified illustration of noise sources and their location in a 1^{st} order CT Σ-Δ modulator.

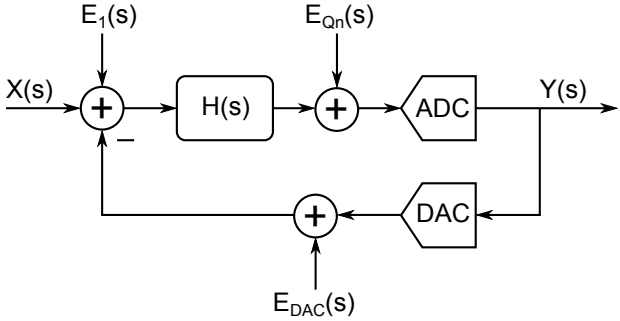


Figure 3.19: *Noise sources* $\left(E_1(s), E_{Qn}(s) and E_{DAC}(s)\right)$ *in a* 1^{st} *order CT Σ-Δ modulator [5].*

$E_1(s)$ is modeling the noise at the input of the modulator as well as the noise at the input of the loop filter, $H(s)$. $E_{Qn}(s)$ is the noise generated at the input of the quantizer and the noise present in the DAC is modeled as $E_{DAC}(s)$. The transfer function becomes (simplified):

$$Y(s) = \frac{X(s)H(s)}{1+H(s)} + \frac{E_1(s)H(s)}{1+H(s)} - \frac{E_{DAC}(s)H(s)}{1+H(s)} + \frac{E_{Qn}(s)}{1+H(s)} = \\ = STF(s)[X(s) + E_1(s) - H_{DAC}(s)] + NTF(s)E_{Qn}(s) \tag{3.38}$$

According to Equation 3.38 the DAC noise, the input noise and the filter noise will appear unattenuated at the output in the passband. The noise at the input of the quantizer, however, will appear at the output shaped like the quantization noise. E_{Qn} can then be neglected, if the NTF's attenuation in the passband is high enough. This shows that the location of the noise source is critical regarding the contribution it got at the output of the modulator.

3.3.2 Excess Loop Delay

Excess loop delay (ELD) is the effect of the delay from the sampling instant of the quantizer to the output of the DAC [5]. This can't be avoided, because of the non-zero switching time in e.g. transistors. The output of the of a NRZ DAC with a time delay t_d is illustrated in Figure 3.20.

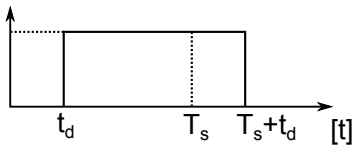


Figure 3.20: *Output of a NRZ DAC suffering from excess loop delay, with time delay t_d.*

The ELD effect is dependent on the shape of the DAC [5]. A DAC shape that is within the sampling period (such as RZ DAC with $t_d < 0.5T_s$), results in a coefficient deviation in the loop-filter [5]. For a DAC shape that extends into the next sampling period (such as NRZ and HRZ DAC's with $t_d > 0$) results in order increment of the loop-filter [5]. It is shown by [5, 10] that NRZ DAC suffers more of ELD compared to RZ. There is almost no degradtion of the CT Σ-Δ modulator if a RZ DAC is used and $t_d < 0.5T_s$ [10].

3.3.3 Clock Jitter

Clock jitter is an effect caused by the timing uncertainty of the clock, due to non-idealities. This effect is gaussian and effects the modulator as additional noise [10]. The clock jitter effects both the quantizer and the DAC [5] but, however, the jitter noise introduced in the quantizer is attenuated like the quantization noise. The jitter noise introduced in the DAC is not shaped, thus it degrades the modulator. The clock jitter can be seen as variation of the pulse width of the DAC, which corresponds to variation of the amount of feedback charge [15]. The DAC is only affected by the clock jitter when it's switching, therefore the RZ and HRZ DACs are affected more by clock jitter compared to NRZ DAC [10]. Another way to reduce the influence of clock jitter is to use a multibit DAC [15].

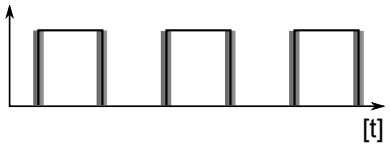


Figure 3.21: *Illustration of a jittered clock, where the shadows represents the clock uncertainty area.*

3.3.4 Unequal Rise/Fall Time of DAC

Unequal rise and fall times of the DAC is caused by mismatch of the output current of the DAC [16]. It causes code dependency and this phenomenon is called ISI (Inter-Symbol Inteference) [15]. For example: the avarage of the codes $c_1 = [1, 0, 1, 0]$ and $c_2 = [1, 1, 0, 0]$ should be equal. But with unequal rise and fall times, this is not true. The DAC becomes non linear and will cause distortion tones and additional noise at the output of the ADC [16]. A solution to prevent ISI is to use a differential DAC or employ RZ of HRZ DAC instead of NRZ DAC [15].

3.3.5 Operational Amplifier Non-Idealities

The integrators in the loop-filter is usually made of RC-integrators or g_mC-integrators [15]. In this section the impact of non-idealities in operational amplifiers (OP-amps) in RC-integrators will be described. Figure 3.22 shows the schematic of an RC-integrator. Since loop-filter non idealities are not supressed (as shown in Figure 3.19), non idealities in the integrators will degrade the modulators performance [15].

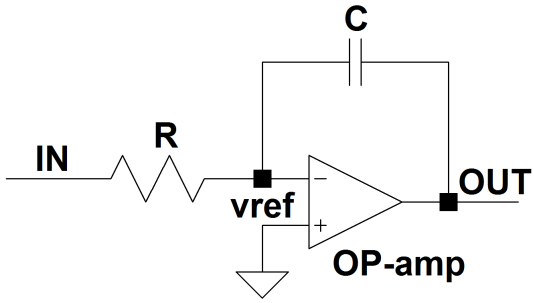


Figure 3.22: *The RC-integrator [24].*

Finite DC Gain

An ideal RC-integrator with infinite DC gain have a transfer function of [10]:

$$I_{RC}(s) = -\frac{1}{RCs}, \tag{3.39}$$

but, due to finite DC gain (A_0) of practical Op-amps, the real transfer function becomes [10]:

$$I_{RC}(s) = -\frac{1}{RCs}\frac{1}{1+(1+\frac{1}{RCs})\frac{1}{A_0}}. \tag{3.40}$$

Figure 3.23 shows an example the impact of NTF with loop-filter consisting of Op-amp with finite DC gain. This effect of finite DC gain on integrators is often called "leaky integration" [10].

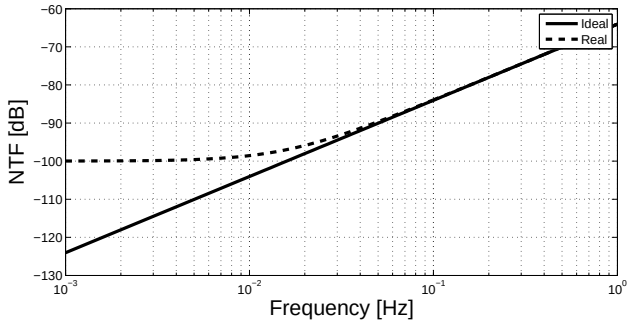


Figure 3.23: *Magnitude response of an ideal NTF and NTF with an Op-amp with finite DC gain (100K or 100 dB).*

Finite Gain-Bandwidth

An ideal OP-amp has infinte bandwidth. Real OP-amps has a both finite bandwidth and gain. For a single pole (placed at w_p) OP-amp the transfer function is [10]:

$$A(s) = \frac{A_0}{\frac{s}{w_p}+1} = \frac{GBW}{s+\frac{GBW}{A_0}}, \quad GBW = w_p A_0. \tag{3.41}$$

where GBW is referred to as gain-bandwidth product. The GBW is approximately where the OP-amp hits unity.

The transfer function for a RC-integrator with finite GBW becomes:

$$I_{RC}(s) = -\frac{A(s)}{RCsA(s)+RCs+1}. \tag{3.42}$$

The NTF (simplified) for different GBW is illustrated as an example in Figure 3.24. The Gain is set to 100K, with $RC = 10^{-7}$.

[15] states that:

$$GBW > 2\pi f_s, \quad [rad/s] \tag{3.43}$$

for single-loop CT Σ-Δ converters without severe performance degradtion. Here f_s is the sampling frequency of the system. The GBW is oftenly expressed in Hz, so therefore:

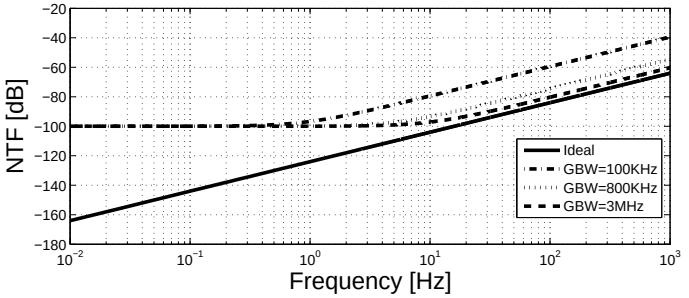


Figure 3.24: *NTF for different GBW.*

$$GBW > f_s \quad [Hz]. \tag{3.44}$$

Finite Slew Rate

An other non-ideality in Op-amp (and RC-integrator) is the finite slew rate (SR). Slew rate is due to limited output current, which is intended to charge the capacitor in the RC-integrator. The SR in CT Σ-Δ is relaxed compared to DT Σ-Δ, but insufficient SR is causes distortion and additive noise [15]. The easiest way to determine sufficient SR is by simulation, since different Σ-Δ modulators, DAC shapes, etc., influence the SR required and makes it difficult to calculate. Therefore, SR simulation results will be presented in Section 6.2.1.

3.4 Digital Filtering and Decimation

The oversampled data coming from the Σ-Δ modulator need to be filtered and decimated (lowering the sampling rate) to remove the out-of-band noise and to be converted down to the Nyquist rate. See Figure 3.25 for an illustration of post processing of data from Σ-Δ modulator by filtering and decimation.

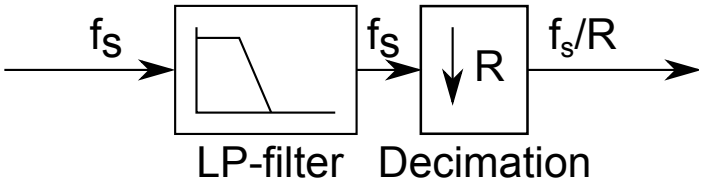


Figure 3.25: *Low-pass filtering and decimation by a factor R.*

Because of the high data rate from the Σ-Δ modulator, the low-pass filter in Figure 3.25 need to operate in fast. Since digital filters often consists of multipliers, this means that the multipliers in the filter need to be very fast and the filter tend to be very long [4]. Eugene B. Hogenauer introduces a class of digital linear phase

FIR filters for decimation in his paper [6] which doesn't require any multipliers. This class of filters are called CIC (Cascaded Integrator Comb) filters.

3.4.1 CIC filters

An illustration of a CIC filter is shown in Figure 3.26.

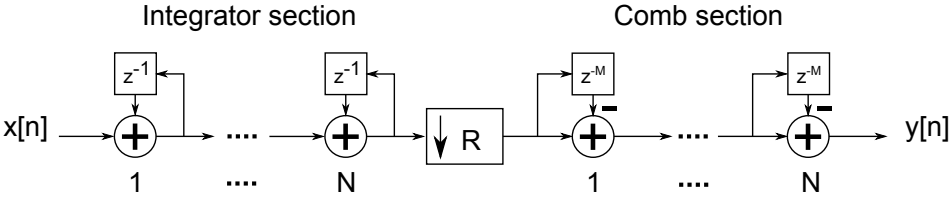


Figure 3.26: *Illustration of a CIC filter.*

The integrator section consists of N number of integrators operating at f_s. The Comb section consists of N number of comb filters with differential delay M operating at the lower frequency f_s/R (where R is the decimation factor). The total filter respons becomes [6]:

$$H(z) = H_I^N(z)H_C^N(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} = [\sum_{k=0}^{RM-1} z^{-k}]^N. \tag{3.45}$$

The magnitude response can be expressed as [6]:

$$|H(f)| = \left| \frac{\sin(\pi M f)}{\sin(\frac{\pi f}{R})} \right|^N. \tag{3.46}$$

The differential delay, M, is chosen to be usually 1 or 2 [6]. See Figure 3.27 for the frequency response relative to the low (decimated) sampling frequency of the CIC filter for different filter orders.

One can see that the a zero is placed at every multiple of the low (decimated) frequency. A region around every multiple of the decimated frequency is folded back into the passband, causing aliasing [6]. The region is $2f_B$ wide, where f_B is the passband frequency relative to the low sampling rate. The maximum aliasing error is usually at the lower edge of the first aliasing band $1-f_B$ [6]. In Figure 3.27 this is approximatly $17.1dB$, $34.3dB$, $51.4dB$, $68.5dB$ and $85.6dB$ for $N = 1 \ldots 5$, respectively. When designing the CIC filter, this has to be taken into account as well as the passband droop at f_B.

To overcome the poor passband droop and the aliasing band characteristics, one can use CIC filters to make transition from high to low sampling rates, with a decimation factor R_1, and then use conventional filters to shape the frequency

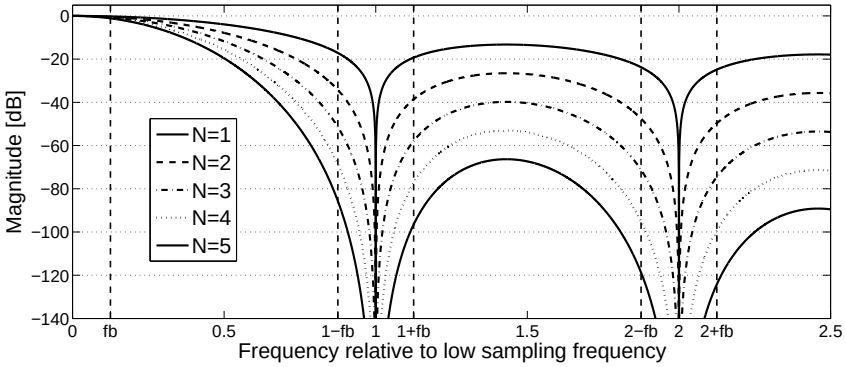


Figure 3.27: *Magnitude respons for different filter order vs. frequency relative to the low (decimated) sampling frequency, where R = 256 and M = 1. f_B is* 1/8 *relative to the low sampling frequency.*

response and decimate by a factor R_2. This is illustrated in Figure 3.28. The total decimation factor is $R = R_1 R_2$.

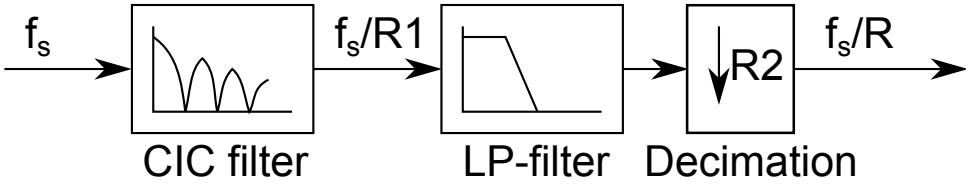


Figure 3.28: *CIC filter decimation by a factor R_1 and conventional decimation filter by a factor R_2, where $R = R1 \times R2$.*

Hogenauer [6] states that the gain of the CIC filter is simply:

$$G = (RM)^N, \tag{3.47}$$

where R is the decimation factor, M is the differential delay in the Comb sections and N is the order of the CIC filter. To be sure that the registers don't overflow, the register width has to be at least [6]:

$$B_{OUT} = N log_2(RM) + B_{IN} - 1, \tag{3.48}$$

where B_{IN} is the number of bits in the input data stream, where the LSB is considered to be bit zero. For an 1-bit input data stream with $R = 64$, $M = 1$ and $N = 5$, the register widths have to be at least 31 bits long.

4

Test Setup

This chapter is describing how the converters are tested. The converters consists of external components and an FPGA, which are mounted on a PCB. There will also be a section about the test setup quality (Section 4.2).

4.1 Test Setup

The test setup is illustrated in Figure 4.1. The PC generates a sine wave which is sent to an external sound card, the M-Audio Fast Track Pro. The sound card is then genereting an analog signal of the sine wave which is sent to the DUT (Device Under Test). The DUT is the converter under test, which is a PCB with the FPGA and external components. The result of the A/D-convertion, generated by the DUT, is then fed back to the sound card using S/PDIF with 24 bits resolution, which is then recorded by the PC. The collected data is analyzed in Matlab.

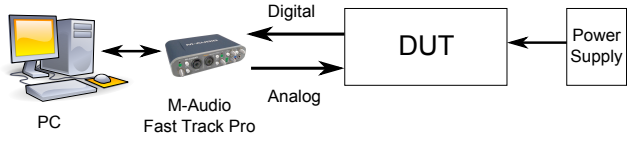


Figure 4.1: *Test setup for testing the converter.*

The sound card (M-Audio Fast Track Pro) claims to be a 103dB SNR and 86 dB SNDR DAC [14].

4.2 Control of Test Setup Quality

To control if the sound card have the claimed SNR and SNDR, this section will present results of the sound card only. This is done by using the sound card in loop-back, i.e. feeding an analog output and recording it with the analog input of the sound card (ADC). The built in ADC claims to have a 101 dB SNR and 86 dB SNDR [14]. An FFT plot of the recorded signal is shown in Figure 4.2.

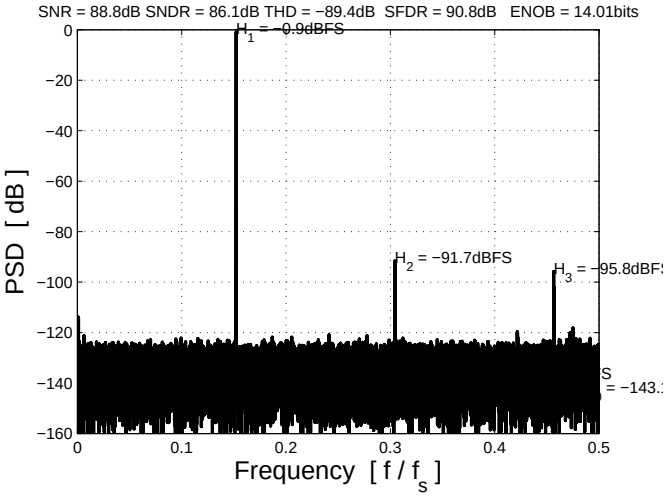


Figure 4.2: *65536 point FFT of the output of the M-Audio Fast Track Pro, using a -1dBFS and ∼7.3KHz input signal. The SNDR is verified (86 dB), but the SNR is much lower than the stated 103 dB.*

SNDR/SNR vs. input frequency is shown in Figure 4.3.

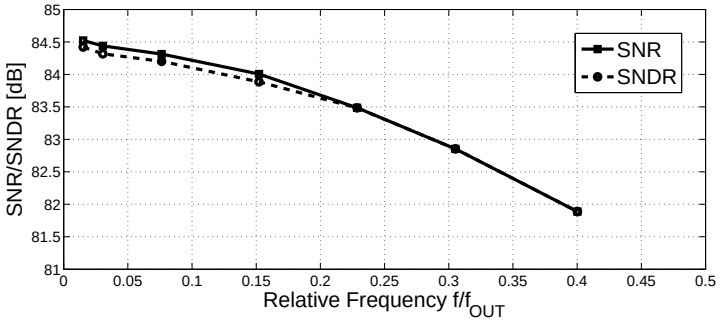


Figure 4.3: *SNR/SNDR vs. frequency of M-Audio Fast Track Pro, using a -6dBFS input signal.*

SNDR/SNR vs. input amplitude is shown in Figure 4.4.

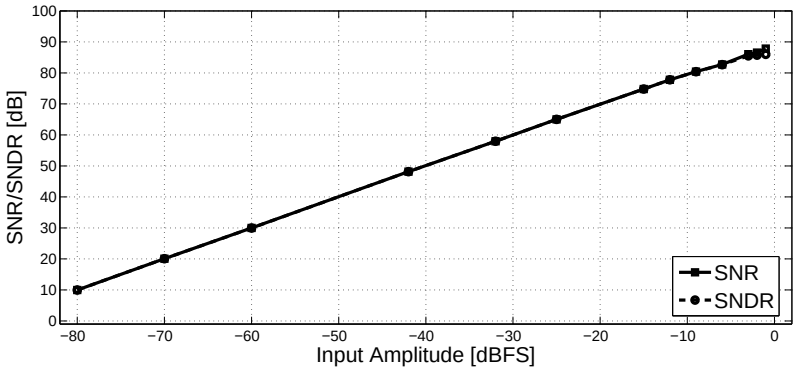


Figure 4.4: *SNR/SNDR vs. input amplitude of M-Audio Fast Track Pro, using a ∼7.3KHz input signal. The claimed 86 dB SNDR is reached, but not the claimed 103 dB SNR.*

The 86 dB SNDR of the M-Audio DAC implies an ENOB of about 14 bits. Because of that the test can't verify that the DUT has a ENOB better than 14 bits, by using the M-Audio Fast Track Pro. The claimed 103dB SNR cannot be seen in Figure 4.2, Figure 4.3 and Figure 4.4 using this test setup.

5

Implementation of a Passive Σ-Δ Converter

This chapter will describe the implementation of a low-cost passive Σ-Δ converter. First there will be a section about the system overview (Section 5.1). Thereafter there will be a section about the implementation of the modulator itself (Section 5.2), a section about the CIC filter (Section 5.3) and a section about the FIR filter (Section 5.4). Section 5.5 presents the results. In the last section (Section 5.6) there will be a discussion of the results of the passive Σ-Δ converter.

5.1 System Overview

The system is illustrated in Figure 5.1.

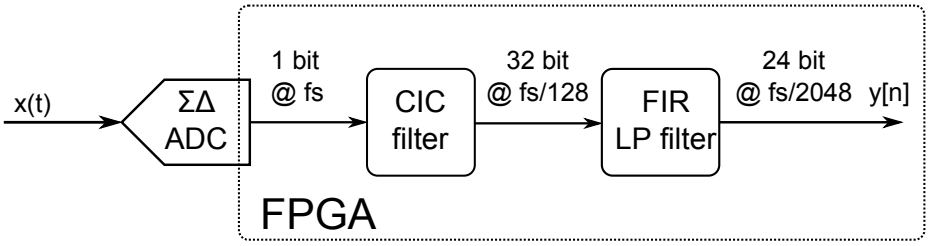


Figure 5.1: *System overview of the passive Σ-Δ ADC.*

The Σ-Δ modulator is described in Section 5.2, the CIC filter is described in Section 5.3 and the FIR filter is described in Section 5.4.

Specification	Symbol	Value
Sampling frequency	f_s	98.304MHz
Oversampling ratio	OSR	2048
Output sampling rate	f_{OUT}	48KS/s
Supply voltage	Vdd	3.3V single supply
Input bandwidth	f_B	20KHz
Input voltage amplitude (max)	A_{in}	1.65 V

Table 5.1: *Specification for the passive Σ-Δ ADC.*

5.2 The Passive Σ-Δ Modulator

In order to cut the cost of a Σ-Δ ADC, the loop-filter consists only of passive components. The loop-filter of a typical (active) Σ-Δ is employing integrators with high gain (e.g. RC-integrators). One can make an integrator of passive components with e.g. a RC-filter, a so called "lossy integrator" with no gain. The linearization of the passive Σ-Δ is shown in Figure 5.2. The gain G is the gain of the quantizer/comparator [3], which in Figure 3.9 is assumed to be small and negligible.

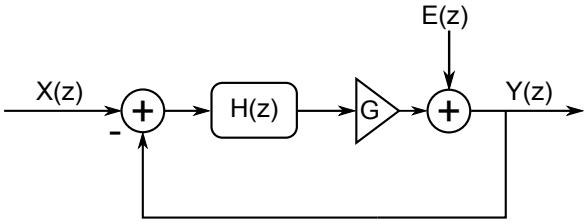


Figure 5.2: *Linearization of the passive Σ-Δ ADC.*

The transfer function becomes:

$$Y(z) = \frac{GH(z)}{1 + GH(z)}X(z) + \frac{1}{1 + GH(z)}E(z) \tag{5.1}$$

The gain factor G is assumed to be constant. [3] estimates the value of G by nulling the input, x. The 1-bit output, y[n], will alternate (ideally) between 0 and 1 at a rate of $f_s/2$. This signal is then passed to the (low-pass) loop filter by a DAC. If the sampling frequency is high enough the signal is attenuated by a factor $|H(f = f_s/2)|$, and this G is roughly:

$$G \approx \frac{1}{|H(f = f_s/2)|}. \tag{5.2}$$

A first order RC-filter with transfer function:

$$H(s) = \frac{1}{RCs + 1} = \frac{1}{\frac{s}{w_p} + 1}. \tag{5.3}$$

By changing the location of the pole, w_p, the gain factor G gets changed. In Figure 5.3 the NTF of two passive loop-filters with different pole placements are shown. The ideal first order NTF (with an active loop-filter) are also shown for comparison. One can see that, by lowering the w_p, the NTF gets higher attenuation at low frequencies. This is also stated in [3]. Therefore the cut-off frequency in the loop-filter will be as low as possible. The limit is the upper bound of the input frequency, i.e. 20KHz. Therefore this system's pole will be placed close to that frequency.

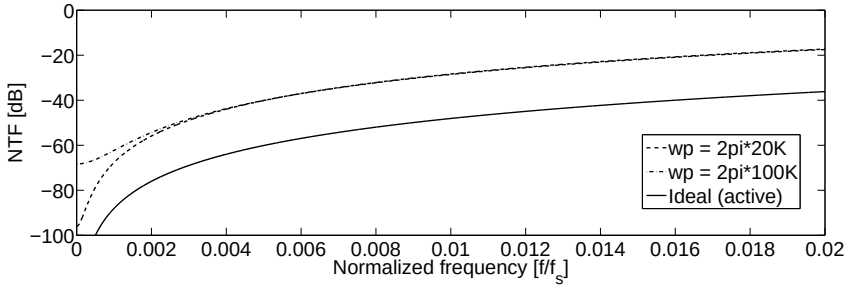


Figure 5.3: *NTF with passive loop-filter with different w_p compared with an active loop-filter.*

The total system of the passive Σ-Δ converter is illustrated in Figure 5.4.

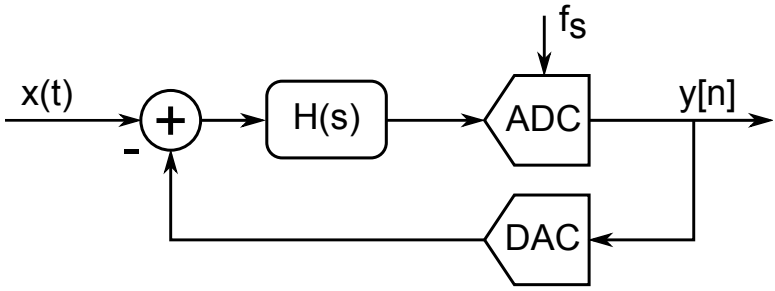


Figure 5.4: *The passive Σ-Δ converter.*

The loop-filter, $H(s)$, is a simple RC filter with transfer function:

$$H(s) = \frac{1}{RCs + 1}, \tag{5.4}$$

where RC is chosen to be as:

$$RC = \frac{1}{w_p} = \frac{1}{2\pi 20KHz}. \tag{5.5}$$

The ADC in Figure 5.4 is chosen to be a 1-bit quantizer, employing the LVDS buffer in the FPGA, sampled at $f_s = 98.304MHz$.

The DAC is chosen to be a 1 bit DAC, which only uses one pin on the FPGA. Figure 5.5 illustrates the 1-bit DAC. Here, the output of the FPGA is chosen to be a tri-state buffer and therefore the output of the DAC can either be Vdd, GND or T. This tri-state buffer can be used to create NRZ, RZ and HRZ DAC pulses. T stands for tri-state and is a high output impedence state (no current can flow out of the FPGA). NRZ pulses is either "high" or "low" for the whole sample period, i.e., it doesn't employ the T-state. On the other hand, the T-state can be used to implement RZ and HRZ pulses which is "off" for half of the sample period. One thing to take into account is the parasitic capacitance assosiated with the pad, Cp. This capacitance is max 10pF [26]. This implies that the time constant, $R_{DAC}Cp$, has to be as low as possible, in order to get the same shape as illustrated in Figure 3.14.

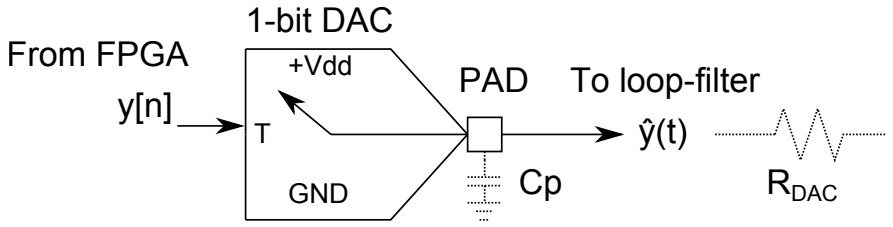


Figure 5.5: *Simple illustration of an 1-bit DAC.*

The chosen 1-bit DAC will use NRZ pulses because of the simplicity and "minimal" impact of the parasitic capacitance.

The converter is therefore only using three pins on the FPGA: two for the LVDS buffer and one for the NRZ DAC.

5.2.1 Realization of the Passive Σ-Δ Converter

Figure 5.6 illustrates the realization of the Σ-Δ converter. The 1-bit digital out will be further processed (filtered and decimated) by the CIC and FIR filter. The reference signal (vref) is mid-range, i.e. $Vdd/2 = 1.65V$.

The chosen component values are presented in Table 5.2.

Component	Value
R_{IN}	$6.8K\Omega$
R_{DAC}	$6.8K\Omega$
C	$1nF$
R	$6.8K\Omega$
C_{IN}	$1\mu F$

Table 5.2: *Component values for the passive Σ-Δ modulator.*

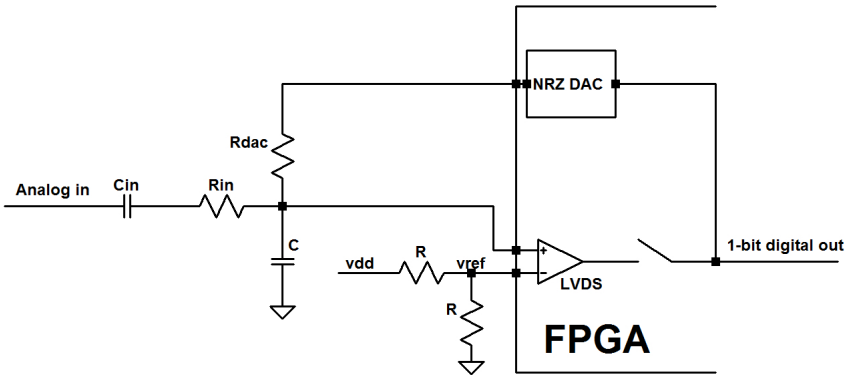


Figure 5.6: *Realization of the passive Σ-Δ converter [13].*

5.2.2 Simulation Results

The simulation was done using Simulink/Matlab with the passive modulator illustrated in Figure 5.4. The filtering and decimation used in this simulation are "ideal", in order to characterize the Σ-Δ modulator only. Figure 5.7 shows an FFT plot of the output of the modulator.

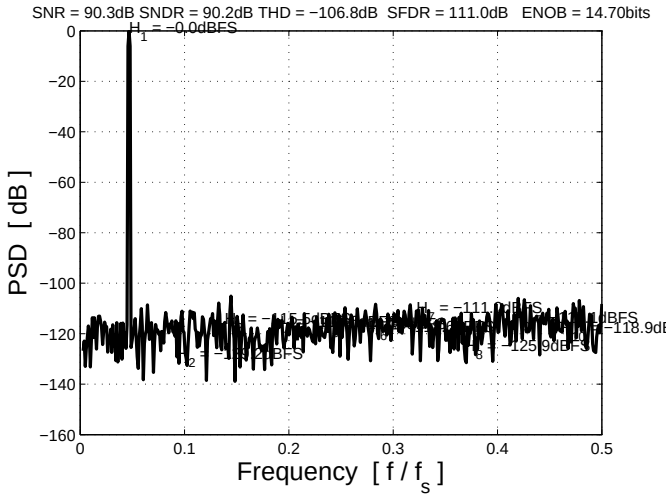


Figure 5.7: *1024 point FFT plot of the output of the passive Σ-Δ modualtor. The input signal is 2KHz and has an amplitude of 1V.*

Figure 5.8 shows the SNDR/SNR vs. input frequency.

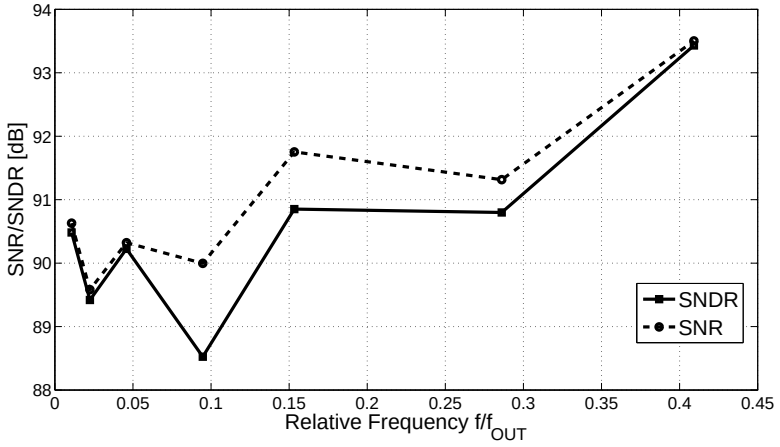
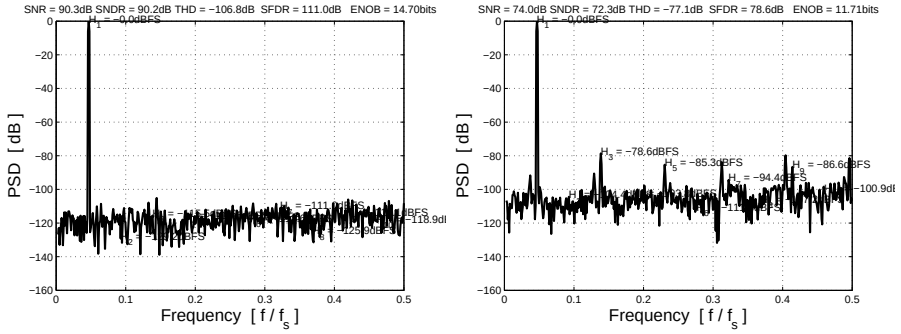


Figure 5.8: *SNDR and SNR vs. Input Frequency. Using a 1V input signal.*

5.2.3 Non-idealities in the Passive Σ-Δ modulator

Hysteresis

Because the noise transfer function (NTF) of the passive Σ-Δ doesn't have high attenuation in the passband, the hysteresis of the comparator can't be neglected. See Section 2.2.1 for the defenition of hysteresis of a comparator. See Figure 5.9 for simulation results of the passive Σ-Δ modulator(illustrated in Figure 5.6) using "ideal" filtering and decimation.



(a) *0mV hysteresis.* ***(b)*** *30 mV hysteresis.*

Figure 5.9: *Hysteresis effect of the comparator in the passive Σ-Δ modulator with "ideal" filtering and decimation. Using 1024 point FFT, with Hanning window and ∼2KHz input signal with amplitude of 1V.*

One can see that the noise floor increases and distortion is generated due to the

hysteresis of the LVDS buffer. See Figure 5.10 for simulation results of the passive Σ-Δ, varying the comparator's hysteresis. The plot shows SNDR vs. Hysteresis.

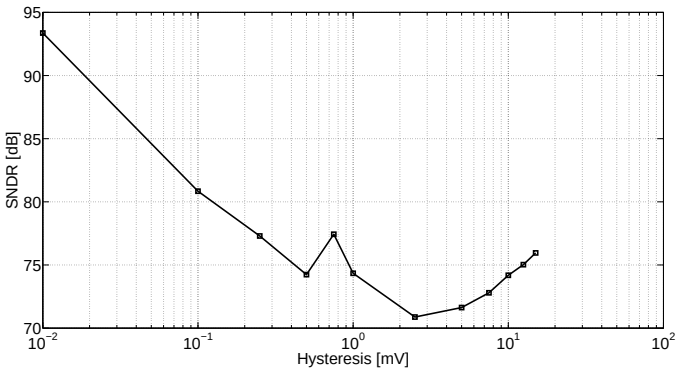


Figure 5.10: *SNDR vs. Hysteresis. Using a 1V input signal of 2KHz.*

DAC Non-idealities

According to Section 3.3, the NRZ DAC suffers from clock jitter, excess loop delay (ELD) and ISI inter alia. This will cause more noise and distortion at the modulator output.

Other Non-idealities

Other non-idealities will degrade the modulator. Figure 3.19 in Section 3.3.1 shows the a simplified model of noise sources. $E_1(s)$ is modeling the noise at the input at the modulator (such as input signal noise) and noise generated in the loop-filter (such as resistor noise).

5.3 The CIC filter

The CIC filter is specified in Table 5.3. This gives a magnitude response, illustrated in Figure 5.11.

Parameter	Symbol	Value
Order	N	4
Decimation factor	R	128
Differential delay	M	1

Table 5.3: *Parameters of the CIC filter for the passive Σ-Δ converter.*

The attenuation in the aliasing bands are more than 120 dB and the passband droop is only 0.05 dB. The output word length has to be at least (according to Equation 3.48) 28 bits long. The attenuation in the aliasing bands have to be more than 98 dB (= 16 bits) to ensure that there is no degradation in the band of intrest, i.e the passband.

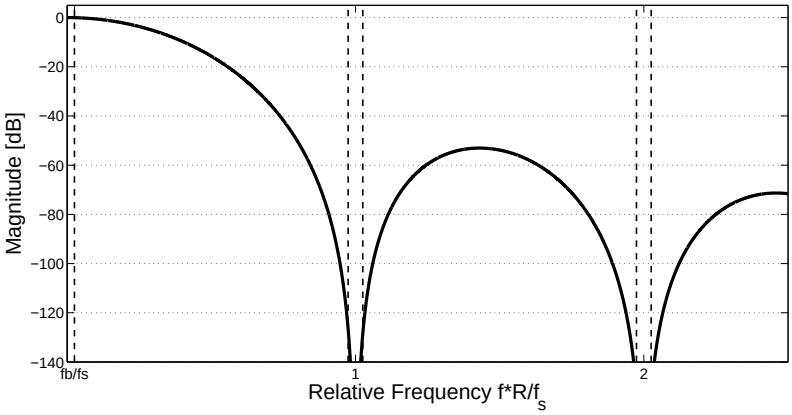


Figure 5.11: *CIC filter response for the passive Σ-Δ converter.*

5.4 The FIR filter

The FIR filter is generated using Matlab. The specification used is shown in Table 6.5. The attenuation in the stopband have to be more than 98 dB (= 16 bits) to ensure that there is no degradation in the band of intrest, i.e the passband.

Parameter	Symbol	Value
Ripple in passband	A_{pass}	1 dB
Attenuation in stopband	A_{stop}	100 dB
Passband edge frequency	F_{pass}	20KHz
Stopband edge frequency	F_{stop}	24KHz
Decimation	R	16
Operating frequency	f_{FIR}	768KHz

Table 5.4: *FIR filter specification for the passive Σ-Δ converter.*

The resulting FIR filter is illustrated in Figure 5.12. The filter is of order 603.

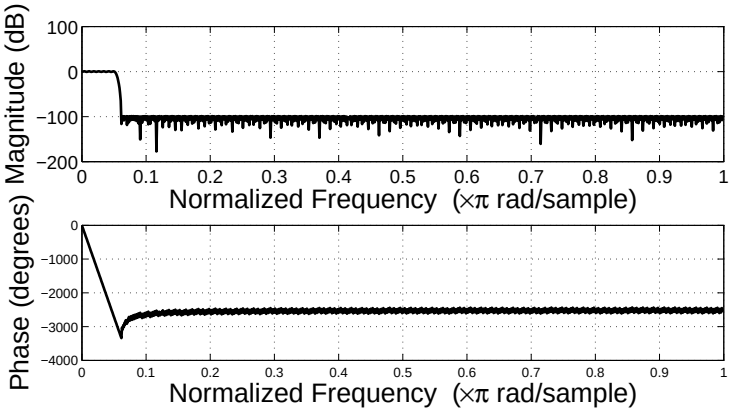


Figure 5.12: *FIR filter response for the passive Σ-Δ converter.*

5.5 Results

This section presents the results of the passive Σ-Δ modulator, using the modulator illustrated in Figure 5.1. The test setup is described in Chapter 4.

Figure 5.13 shows the FFT plot of the output of the passive Σ-Δ modulator.

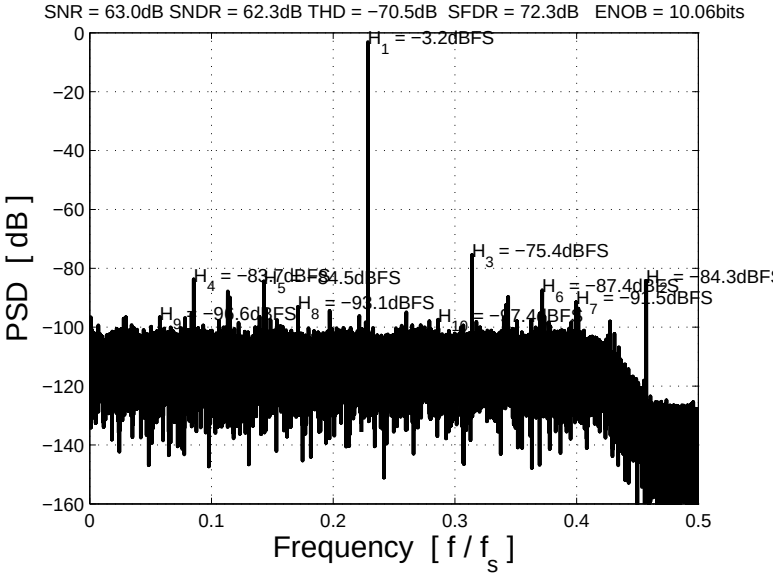


Figure 5.13: *65536 point FFT plot of a 10 KHz -3dBFS input signal.*

Figure 5.14 shows the SNDR/SNR vs. input frequency of the output of the pas-

sive Σ-Δ modulator.

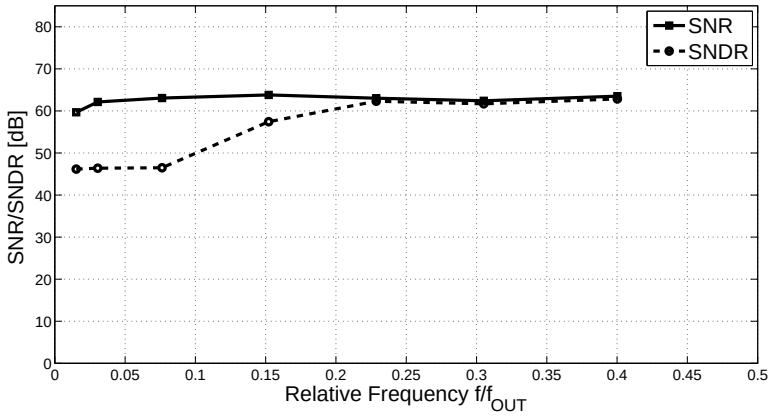


Figure 5.14: *SNR and SNDR vs. Frequency using a -3dBFS input signal.*

Figure 5.15 shows the SNDR/SNR vs. input amplitude of the output of the passive Σ-Δ modulator.

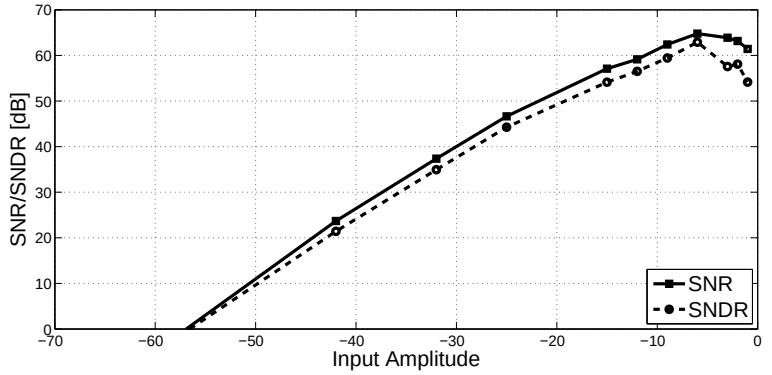


Figure 5.15: *SNR and SNDR vs. input amplitude using a 7.3KHz input signal.*

5.5.1 FPGA resources

Table 5.5 shows the FPGA resources used. The "other" row includes e.g. a S/PDIF driver and the sampling register. Three pins on the FPGA are used for the Σ-Δ converter.

	Slice Regs	LUTs	Block RAM	DSP	DCM/PLL
FIR	312	213	5	3	0
CIC	194	91	0	5	0
Other	93	104	0	0	1
Total	599	408	5	8	1
FPGA utilization	5%	7%	7%	50%	50%

Table 5.5: *FPGA resources used in the passive first order Σ-Δ Converter.*

5.6 Discussion

In this section the results in Section 5.5 is discussed.

Figure 5.13, 5.14 and 5.15, show a peak SNDR of about 62.3dB, which is equivalent to about 10 bits. This is far from the theoretical SNDR of up to 93 dB (∼15 bits), shown in Figure 5.7 and 5.8. The degradation comes mainly from the poor attenuation in the band of intrest (20Hz - 20KHz) in the NTF, shown in Figure 5.3. Because of that, the hysteresis of the LVDS input buffer is of main concern. The hysteresis effecting the modulator is shown in Figure 5.9b and 5.10, which causes additional noise and distortion.

Other noise sources such as clock jitter, ELD, ISI, power supply noise, cuircuit noise inter alia, will degrade the modulator and add up to the total SNDR/SNR.

In Table 5.5, the used resources for the passive Σ-Δ converter is listed. One can see that the FIR filter and the CIC filter are occupying the most "area" in the FPGA. This area can be optimized by, e.g., changing the specification and parameters of the filters.

6

Implementation of a Second Order Σ-Δ Converter

This chapter will describe the implementation of a second order Σ-Δ converter. First there will be a section about the system overview (Section 6.1). Thereafter there will be a section about the implementation of the modulator itself (Section 6.2), a section about the CIC filter (Section 6.3) and a section about the FIR filter (Section 6.4). Section 6.5 presents the results. In the last section (Section 6.6) there will be a discussion of the results of the second order Σ-Δ converter.

6.1 System Overview

The complete system of the second order Σ-Δ converter is illustrated in Figure 6.1.

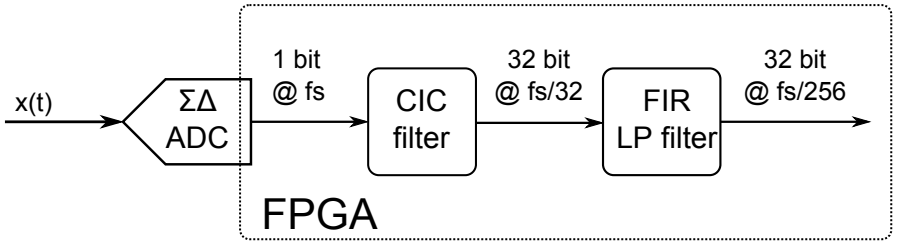


Figure 6.1: *System overview of the second order Σ-Δ converter.*

The Σ-Δ modulator is described in Section 6.2. The CIC filter and the FIR filter is described in Section 6.3 and 6.4, respectively. The system specification is shown in Table 6.1.

Specification	Symbol	Value
Sampling frequency	f_s	12.288MHz
Oversampling ratio	OSR	256
Output sampling rate	f_{OUT}	48KS/s
Supply voltage	Vdd	3.3V single supply
Input bandwidth	f_B	20KHz
Input voltage amplitude (max)	A_{in}	1.65 V

Table 6.1: *Specification for the second order Σ-Δ ADC.*

6.2 The 2^{nd} Order CT Σ-Δ Modulator

A second order DT Σ-Δ modulator has a NTF:

$$NTF(z) = (1 - z^{-1})^2 \tag{6.1}$$

and according to Equation 3.33 the loop-filter becomes:

$$H_Y(z) = -\frac{2z + 1}{(z - 1)^2}. \tag{6.2}$$

By using Equation 3.29, the CT equivalent becomes:

$$H_Y(s) = -\frac{a_1 T_s + 1}{k_1 T_s^2 s^2}, \tag{6.3}$$

which is illustrated in Figure 6.2. The coefficients a_1 and k_1 depends on the DAC (assuming rectangular DAC pulses).

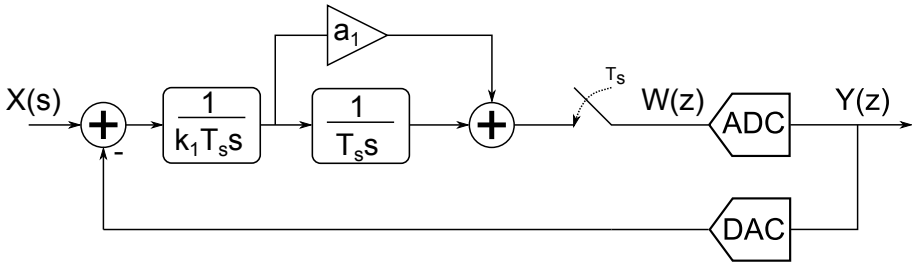


Figure 6.2: *A 2nd order CT Σ-Δ feed-forward modulator.*

The ADC is a 1-bit quantizer using the LVDS buffer (as a comparator) in the FPGA. The DAC is chosen to be a 1-bit DAC emplyoing NRZ pulses. The choice of the NRZ DAC is discussed in Section 5.2. The DAC will only use one output pin on the FPGA. By using NRZ DAC, the coefficients k_1 and a_1 becomes 1 and 1.5, respectively.

The modulator will therefore only use 3 pins (2 for the LVDS, 1 for the DAC) on the FPGA. The OSR of the modulator is chosen to be 256 (2^8). This gives a ideal

SQNR, derived from Equation 3.28, of:

$$SQNR = 1.76 + 6.02 + 50log_{10}(256) + 10log_{10}(5) - 4log_{10}(\pi) \approx 115[dB]. \quad (6.4)$$

That is equal to a 18.8 bits Nyquist-rate ADC.

One has be sure that the voltage swing within the loop-filter is between the voltage rails (i.e. 3.3V and GND). This is done by simulation in Simulink. The voltage of the input of the quantizer is shown in Figure 6.3.

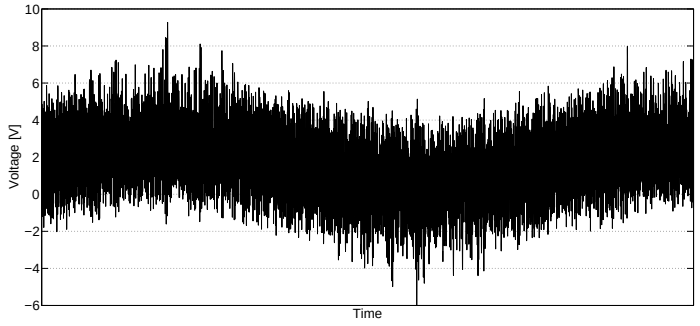


Figure 6.3: *Matlab simulation of the input to the quantizer with* $a_1 = 1.5$ *and* $k_1 = 1$.

This doesn't comply with the LVDS specifications in Table 2.2 and because the modulator will use 3.3V single supply, it will cause clipping. By changing the values of a_1 and k_1, the voltage swing at the input of the quantizer can be lowered. In Figure 6.4, $a_1 = 2.5$ and $k_1 = 156$ which improves the voltage swing significant.

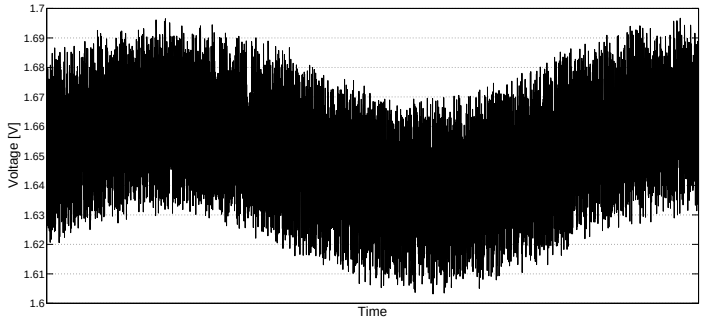


Figure 6.4: *Matlab simulation of the input to the quantizer with* $a_1 = 2.5$ *and* $k_1 = 156$.

6.2.1 Realization of the 2^{nd} order CT Σ-Δ modulator

The realization of the modulator is shown in Figure 6.5. The loop-filter is a single amplifier section, derived from [24], chapter 6.5. This loop-filter only use one OP amplifier, which is better than two in a low-cost perspective.

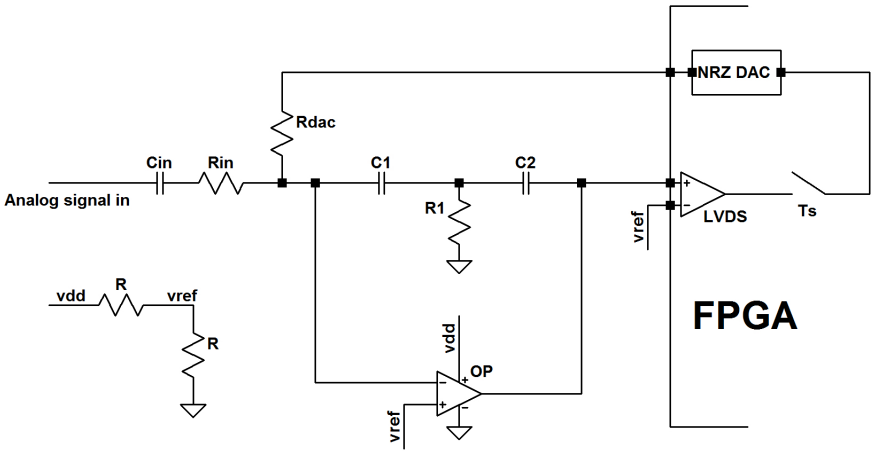


Figure 6.5: *Realization of the 2^{nd} order CT Σ-Δ modulator.*

The reference voltage is mid-range, i.e. $V_{dd}/2 = 1.65V$ and is generated by a voltage divider with two resistors. The transfer function from the DAC to the input of the LVDS buffer is:

$$H_Y(s) = -\frac{R_1(C_1 + C_2)s + 1}{R_{DAC}R_1C_1C_2s^2} = -\frac{a_1T_ss + 1}{k_1T_s^2s^2}, \tag{6.5}$$

where

$$R_1(C_1 + C_2) = a_1T_s \tag{6.6}$$

$$R_{DAC}R_1C_1C_2 = k_1T_s^2 \tag{6.7}$$

Table 6.2 shows the chosen component values. The chosen component values corresponds to $a_1 \approx 2.5$ and $k_1 \approx 156$.

Component	Value
C1	100pF
C2	100pF
R1	1KΩ
R_{DAC}	100KΩ
R_{IN}	100KΩ
R	4.7KΩ
C_{IN}	1μF

Table 6.2: *Component values for the loop filter in the second order Σ-Δ modulator.*

Operational Amplifier selection

According to Section 3.3.5, OP-amp non idealities has to be taken into account. According to Equation 3.44, the GBW has to have $GBW > f_s$, to prevent severe degradtion in performance.

The slew rate limit is simulated using LTspice, which is a SPICE simulator produced by Linear Technology. The circuit, which is illustrated in Figure 6.5, is simulated with different values of SR of the OP-amp. The 1-bit digital data output is further processed in Simulink, where an "ideal" low-pass filtering and decimation is used to analyze the impact of the SR. Figure 6.6 shows the simulation of the ENOB vs. SR. The SR in the figure is normalized by a factor $V_{REF}f_s$, where $V_{REF} = 1.65$ and f_s is the sampling frequency according to Table 6.1.

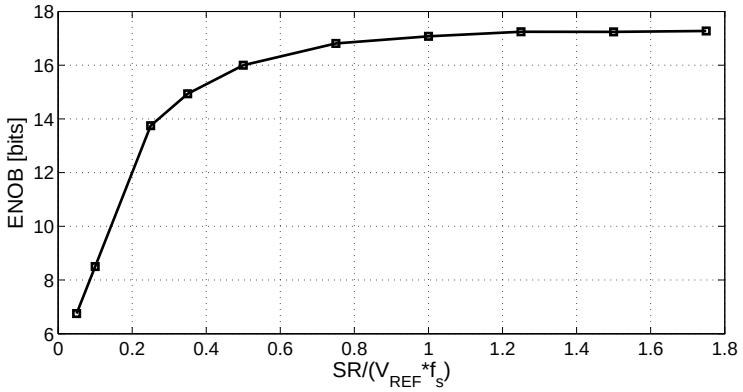


Figure 6.6: *Simulation of the SR in the Op-amp in the second order Σ-Δ modulator.*

If

$$\frac{SR}{V_{REF}f_s} > 0.75 \rightarrow SR > 0.75V_{REF}f_s \approx 15V/\mu V, \tag{6.8}$$

there is almost no degradtion of the modulator.

Table 6.3 summarizes the OP-amp specification.

Specification	Symbol	Value
DC Gain	A_0	100K (100dB)
Gain Bandwith Product (min)	GBW	12.288 MHz
Slew Rate (min)	SR	15 $V/\mu V$

Table 6.3: *OP-amp specifications.*

The Op-amp is chosen to be LMV793, which is a low-noise operational amplifier with 88MHz GBW, 32/24 $V/\mu V$ SR and approximately 100dB DC Gain [22]. The chosen Op-amp met the specification in Table 6.3.

6.2.2 Simulation Results

The simulation was done using LTspice and Simulink/Matlab. LTspice simulated the Σ-Δ modulator, while Simulink/Matlab simulated an "ideal" filter and decimation. Figure 6.7 shows an FFT plot of the second order converter and Figure 6.8 shows SNR/SNDR vs. frequency of the output of the converter.

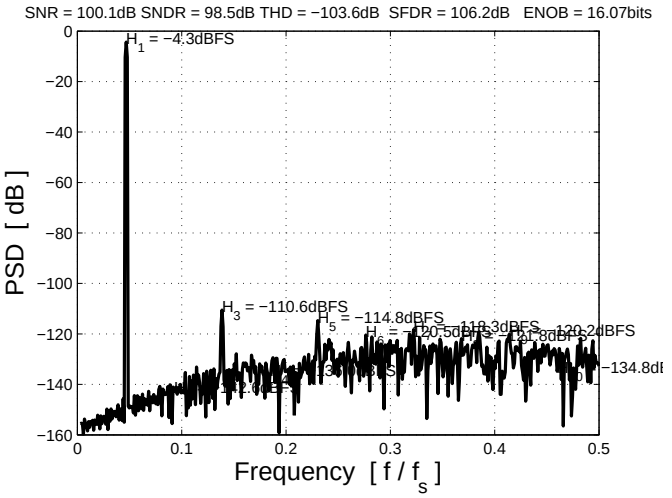


Figure 6.7: *Simulation result of the second order Σ-Δ modulator using 1024 points FFT, 1V input amplitude (-4.3 dBFS).*

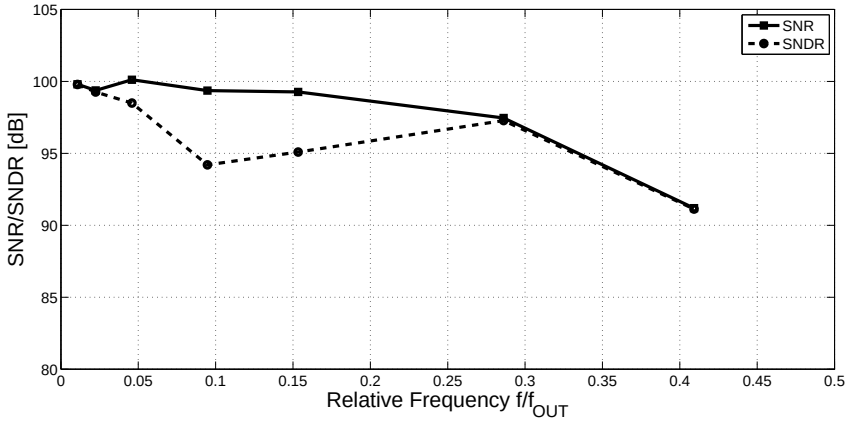


Figure 6.8: *Simulation result of the second order Σ-Δ modulator, SNR/SNDR vs. Frequency.*

6.2.3 Non-idealities in the Δ-Σ modulator

According to Section 3.3 there are several non-idealities associated with a CT Σ-Δ converter. Because the choice of a NRZ DAC, the converter can be sensetive to clock jitter, ELD and ISI. There are also cuircuit noise (e.g. OP-amp noise, resistor noise) present in the loop-filter that might degrade the converter.

6.3 CIC filter

The CIC filter is specified in Table 6.4. This gives a magnitude response illustrated in Figure 6.9.

Parameter	Symbol	Value
Order	N	5
Decimation factor	R	32
Differential delay	M	1

Table 6.4: *CIC filter parameters for the second order Σ-Δ converter.*

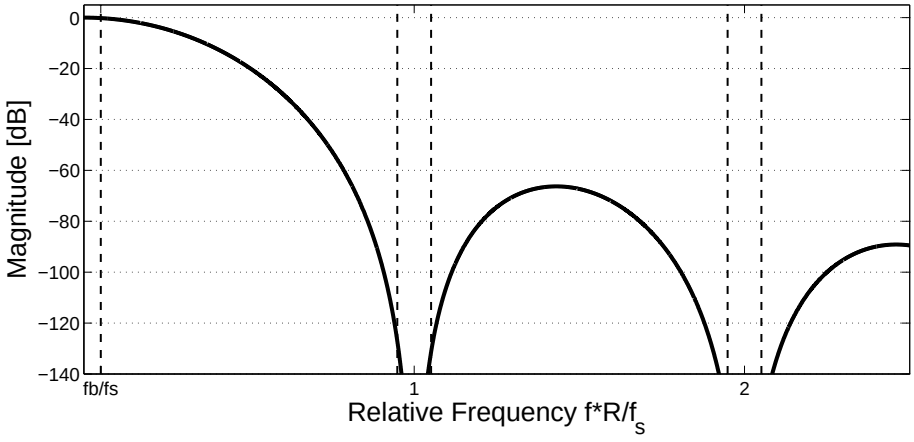


Figure 6.9: *CIC filter response of the second order Σ-Δ converter.*

The attenuation in the aliasing bands are more than 120 dB and the passband droop is only 0.2 dB. The output word length has to be at least (according to Equation 3.48) 25 bits long. The attenuation in the aliasing bands have to be more than 98 dB (= 16 bits) to ensure that there is no degradation in the band of intrest, i.e the passband.

6.4 FIR filter

The FIR filter is generated using Matlab. The specification used is shown in Table 6.5. The attenuation in the stopband have to be more than 98 dB (= 16 bits) to ensure that there is no degradation in the band of intrest, i.e the passband.

Parameter	Symbol	Value
Ripple in passband	A_{pass}	1 dB
Attenuation in stopband	A_{stop}	100 dB
Passband edge frequency	F_{pass}	20KHz
Stopband edge frequency	F_{stop}	24KHz
Decimation	R	8
Operating frequency	f_{FIR}	384KHz

Table 6.5: *FIR filter specification for the second order Σ-Δ converter.*

The resulting FIR filter is illustrated in Figure 6.10. The filter has an order of 302.

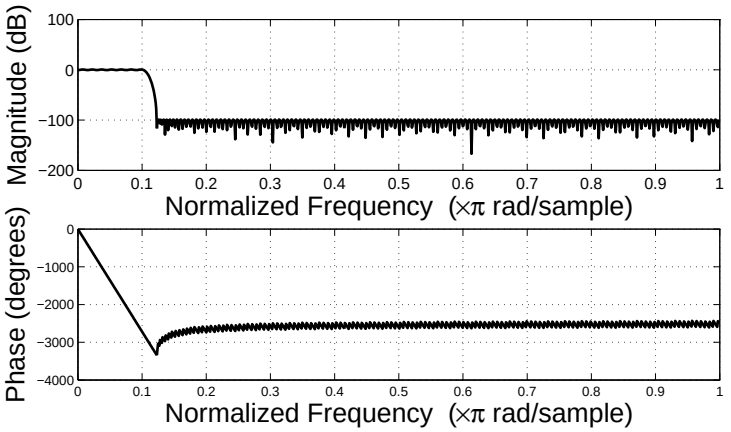


Figure 6.10: *FIR filter response of the second order Σ-Δ converter.*

6.5 Results

This section presents the results of the 2^{nd} order Σ-Δ converter, using the converter illustrated in Figure 6.1. The test setup is described in Chapter 4.

Figure 6.11 shows an FFT plot of the output of the Σ-Δ modulator.

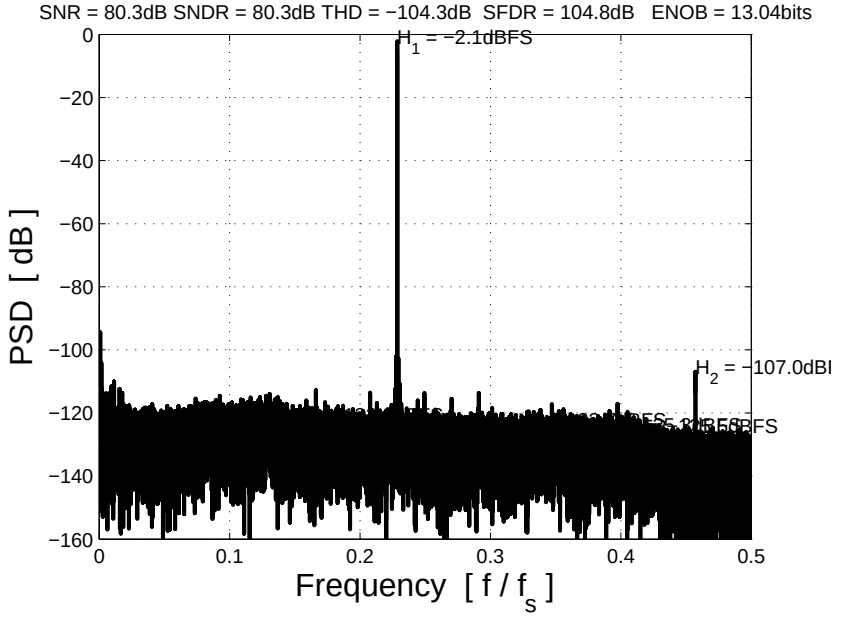


Figure 6.11: *FFT plot of an input frequency of 10KHz -3dBFS using 65536 points FFT.*

Figure 6.12 shows the SNDR/SNR vs. input frequency of the output of the Σ-Δ modulator.

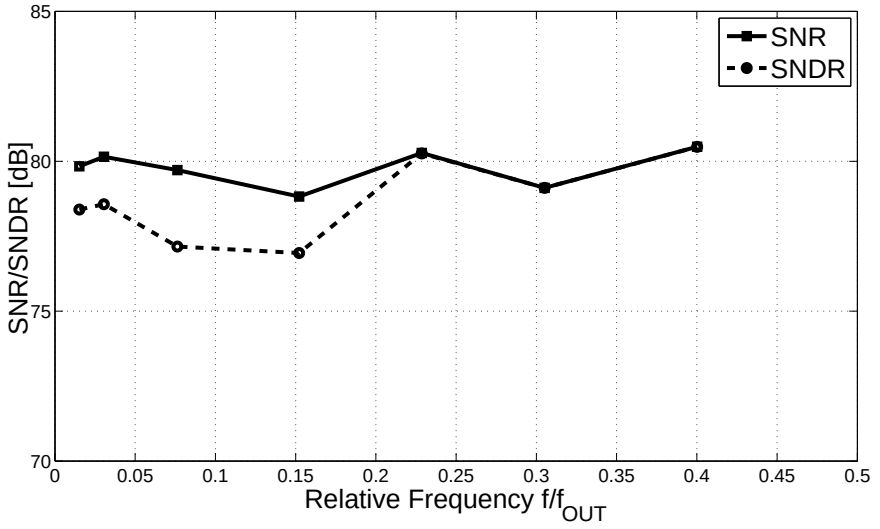


Figure 6.12: *SNR and SNDR vs. frequency using an -3dBFS input signal.*

Figure 6.13 shows the SNDR/SNR vs. input amplitude of the output of the Σ-Δ modulator.

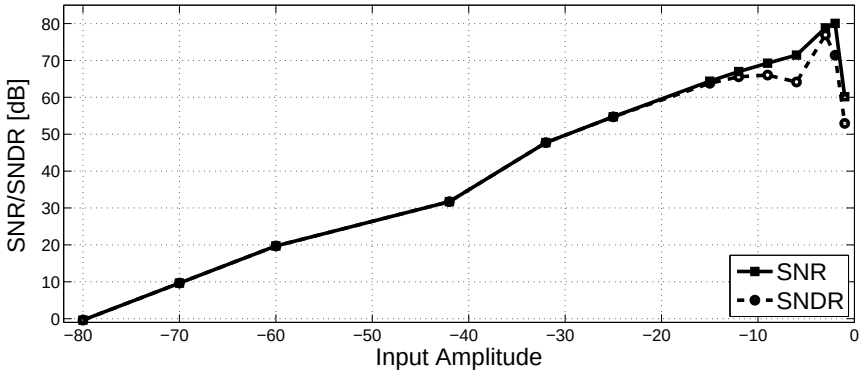


Figure 6.13: *SNR and SNDR vs. input amplitude, using a 7.3KHz input frequency.*

6.5.1 FPGA resources

Table 6.6 shows the FPGA resources used. The "other" row includes e.g. a S/PDIF driver and the sampling register. Three pins on the FPGA are used for the second order active loop-filter Σ-Δ converter.

	Slice Regs	LUTs	Block RAM	DSP	DCM/PLL
FIR	305	200	3	3	0
CIC	209	122	0	2	0
Other	97	108	0	0	1
Total	611	430	3	5	1
FPGA utilization	5%	7%	4%	31%	50%

Table 6.6: *FPGA resources used in the second order Σ-Δ Converter.*

6.6 Discussion

The results in Section 6.5 will be discussed here.

According to Figure 6.11 and Figure 6.13 the peak SNDR is about 80.3dB for the second order Σ-Δ converter, i.e.:

$$SNDR_{peak} = 10log_{10}\left(\frac{S^2}{E_{n,d}^2 + E_{in,n,d}^2}\right) = 80.3dB, \quad (ENOB = 13.04\,bits). \tag{6.9}$$

Where S is the input signal power, $E_{n,d}$ is the noise and the distortion power generated in the converter. $E_{in,n,d}$ is noise and distortion in the input signal. According to Figure 4.2 and Figure 4.4, the peak SNDR for the M-audio test equipment is about 86.1 dB. Therefore the input signal has an SNDR of:

$$SNDR_{in,peak} = 10log_{10}\left(\frac{S^2}{E_{in,n,d}^2}\right) = 86.1dB, \quad (ENOB = 14.01\,bits). \tag{6.10}$$

The second order Σ-Δ modulator is about 6dB (equivalent to about 1 bit) worse than the input signal. The ideal SNDR peak is, by combining Equation 6.9 and Equation 6.10:

$$SNDR_{in,peak} = 10log_{10}\left(\frac{S^2}{E_{n,d}^2}\right) = 81.6dB, \quad (ENOB = 13.26\,bits). \tag{6.11}$$

According to Equation 6.11, the dominant noise and distortion comes from the modulator itself. The simulation result in Section 6.2.2, claims a theoretical ENOB of above 16 bits. The additional noise and distortion may come from clock jitter, ELD, ISI, power supply noise, cuircuit noise and operational amplifier non-idealities inter alia, as discussed in Section 3.3. Further investigation has to be done to find the dominant noise/distortion source to further improve the converter.

Table 6.6 in Section 6.5.1, the used resources for the second order Σ-Δ converter is listed. One can see that the FIR filter and the CIC filter are occupying the most "area" in the FPGA. This area can be optimized by, e.g., changing the specification and parameters of the filters.

7

Conclusions and Future Work

Conclusions and future work will be presented in this chapter.

7.1 Conclusions

Table 7.1 shows a comparison between the passive Σ-Δ converter (from Chapter 5), the second order Σ-Δ converter (from Chapter 6) and the converter that is used today in a product from Actiwave: PCM1807 from Texas Instruments. I have used the same test setup as in Figure 4.1 to test the PCM1807, except that it is powered from another power supply.

Since the PCM1807 is a dual channel ADC, the resources are divided by two in order to compare it with my two solutions. The prices of PCM1807 ($0.90) and LMV793 ($0.45) are taken from Texas Instruments website [9][7]. The price for the passive components (resistors and capacitors) are set to $0.01. The prices don't include the decoupling capacitors needed.

With proper deisgn and careful PCB layout with the PCM1807, the theoretical SNDR is typical 93dB (ENOB ~15.15) according to the datasheet of the PCM1807 [21]. But in order to compare the A/D converters, the same test setup is used (except for another power supply used for PCM1807).

According to Table 7.1, there can be conclusions:

1. The first order passive CT Σ-Δ is moderate in SNDR, but with low cost of external components and with relative large FPGA area. If there's a priority in low-cost the first order passive CT Σ-Δ is a good choice.

2. The second order CT Σ-Δ have the best SNDR, but with large FPGA area

Dynamic parameter	1^{st} **order passive CT** Σ-Δ	2^{nd} **order CT** Σ-Δ	**Actiwave AB with TI PCM1807**
SNR_{peak} **[dB]**	63	80.3	77.9
$SNDR_{peak}$ **[dB]**	62.3	80.3	77.8
$ENOB_{peak}$ **[bits]**	10.06	13.04	12.63
Resources/channel FPGA			
# I/O pins	3	3	4/2
# Slice regs	599	611	256/2
# LUTs	408	430	146/2
# Block RAMs	5	3	0/2
# DSP	8	5	0/2
# DCM/PLL	1	1	1/2
Resources/channel Components			
# Active components	0	1	1/2
# Passive components	6	8	2/2
Total price [$]	0.06	0.53	0.46

Table 7.1: *Comparison between the A/D converters. Since the PCM1807 is a dual channel ADC, its resources are divided by two.*

and highest cost per channel. With demands for good quality in SNDR the second order CT Σ-Δ is a good choice.

3. The PCM1807 have good SNDR, small FPGA area and fairly high cost of external components. If there's demand for small FPGA area and good quality in SNDR an external ADC (such as the PCM1807) is a good choice.

There seems to be a tradeoff between quality (e.g. SNDR), FPGA area and cost.

It is some difficulty to compare the two converters presented in this thesis with the PCM1807. For instance, PCM1807 need two voltages (3.3V and 5V) in order to function [21]. This add up to the total price for the Actiwave AB solution, which is not listed in Table 7.1.

The two converters presented in this thesis can easily be doubled in order to convert stereo audio (like the PCM1807). This doesn't necessary scale the resources of the FPGA and the total price by a factor of two. For instance, one can use LMV794 (which is two LMV793 in a single package) for the second order CT Σ-Δ converter in order to convert stereo audio. The price for LMV794 is \$0.63 [8] which implies a total price of \$0.71 for the second order CT Σ-Δ converter with dual channel. The corresponding total price for the PCM1807 (dual channel) is \$0.92.

The two converters presented in this thesis can be used for other purposes. For example, the passive Σ-Δ converter can easily be modified to be able to convert other analog signals, e.g. signals from sensors that perhaps only need 10 bits

ENOB and is very low-cost.

The recommendation for Actiwave AB is not to use the passive CT Σ-Δ converter for audio applications. Since Actiwave AB is working with high precision audio, this is not an option. But the passive CT Σ-Δ converter can be used for other applications, e.g. convert analog signals from sensors.

To cut cost, Actiwave AB could use the second order Σ-Δ converter in a dual channel configuration (with LMV794) instead of the PCM1807. However, the LVM794 has to be tested and further investigation of the second order CT Σ-Δ converter is necessary in order to achieve 16 bits ENOB.

7.2 Future Work

The things that can be done in the future are listed below:

- More testing has to be done in order to further characterize both the passive and the active Σ-Δ converter. The input (test) signal needs to have better quality than the converter itself.
- The digital filters in the FPGA can be further optimized. The FIR filters are quite long (order of 603 and 302 for the passive and the active Σ-Δ, respectively) and take up relative large FPGA area.
- For the passive Σ-Δ converter there can be more investigation on the passive filter. Perhaps a higher order filter or a RLC-filter can achieve better resolution.
- Further investigation on the DAC pulse shape can be done. There are several types of pulse shapes that are not rectangular (NRZ, RZ, HRZ) such as e.g. SCR (Switched-Capacitor-Resistor). Perhaps one can take advantage of the parasitic capacitance assosiated with the pad (described in Section 5.2) to implement a SCR DAC pulse.
- A differential solution for the second order active Σ-Δ converter, can possible be more immune to noise and non-idealities.
- Further investigation on what the dominant noise source can be done in order to achieve better quality on the converters.

List of Figures

2.1 The complete system. 5
2.2 Simplified LVDS schematic [18]. 6
2.3 Hysteresis of a comparator [1]. 7
2.4 Different ADC architectures and applications [11]. 8

3.1 From analog input signal, $x(t)$, to output, $y[n]$, which is later processed by e.g. a DSP [23]. 9
3.2 The sampling process. 10
3.3 x_p in the frequency domain [5]. 11
3.4 Illustration of quantization. 12
3.5 Illustration of SFDR. 13
3.6 Spectral proporties for Nyquist-rate and oversampling ADC [10]. . 14
3.7 A first order Σ-Δ discrete time modulator. 15
3.8 Output waveform of a Σ-Δ converter with 1-bit quantizer (ADC). . 15
3.9 A linearization of a first order Σ-Δ discrete time modulator in the z-domain. 16
3.10 Noise PSD for Nyquist-rate, oversampling and oversampling+noise-shaping (Σ-Δ) ADC's [10]. 17
3.11 Maximum SQNR for different Σ-Δ orders and OSR with a 1-bit quantizer 18
3.12 Continuous-time Σ-Δ modulator. 18
3.13 Open loop of DT and CT Σ-Δ [10]. 19
3.14 H_{DAC} impulse response for NRZ, RZ and HRZ. 19
3.15 A 2nd order DT Σ-Δ modulator in a feedback topology [10]. 20
3.16 A 2nd order CT Σ-Δ modulator. 20
3.17 A modified 2^{nd} order CT Σ-Δ converter. 21
3.18 A 2nd order CT Σ-Δ STF. 22
3.19 Noise sources $\left(E_1(s), E_{Qn}(s) and E_{DAC}(s)\right)$ in a 1^{st} order CT Σ-Δ modulator [5]. 22
3.20 Output of a NRZ DAC suffering from excess loop delay, with time delay t_d. 23
3.21 Illustration of a jittered clock, where the shadows represents the clock uncertainty area. 24
3.22 The RC-integrator [24]. 24

3.23 Magnitude response of an ideal NTF and NTF with an Op-amp with finite DC gain (100K or 100 dB). 25
3.24 NTF for different GBW. 26
3.25 Low-pass filtering and decimation by a factor R. 26
3.26 Illustration of a CIC filter. 27
3.27 Magnitude respons for different filter order vs. frequency relative to the low (decimated) sampling frequency, where R = 256 and M = 1. f_B is 1/8 relative to the low sampling frequency. 28
3.28 CIC filter decimation by a factor R_1 and conventional decimation filter by a factor R_2, where $R = R1 \times R2$. 28

4.1 Test setup for testing the converter. 29
4.2 65536 point FFT of the output of the M-Audio Fast Track Pro, using a -1dBFS and ~7.3KHz input signal. The SNDR is verified (86 dB), but the SNR is much lower than the stated 103 dB. 30
4.3 SNR/SNDR vs. frequency of M-Audio Fast Track Pro, using a -6dBFS input signal. 30
4.4 SNR/SNDR vs. input amplitude of M-Audio Fast Track Pro, using a ~7.3KHz input signal. The claimed 86 dB SNDR is reached, but not the claimed 103 dB SNR. 31

5.1 System overview of the passive Σ-Δ ADC. 33
5.2 Linearization of the passive Σ-Δ ADC. 34
5.3 NTF with passive loop-filter with different w_p compared with an active loop-filter. 35
5.4 The passive Σ-Δ converter. 35
5.5 Simple illustration of an 1-bit DAC. 36
5.6 Realization of the passive Σ-Δ converter [13]. 37
5.7 1024 point FFT plot of the output of the passive Σ-Δ modualtor. The input signal is 2KHz and has an amplitude of 1V. 37
5.8 SNDR and SNR vs. Input Frequency. Using a 1V input signal. . . . 38
5.9 Hysteresis effect of the comparator in the passive Σ-Δ modulator with "ideal" filtering and decimation. Using 1024 point FFT, with Hanning window and ~2KHz input signal with amplitude of 1V. 38
5.10 SNDR vs. Hysteresis. Using a 1V input signal of 2KHz. 39
5.11 CIC filter response for the passive Σ-Δ converter. 40
5.12 FIR filter response for the passive Σ-Δ converter. 41
5.13 65536 point FFT plot of a 10 KHz -3dBFS input signal. 41
5.14 SNR and SNDR vs. Frequency using a -3dBFS input signal. 42
5.15 SNR and SNDR vs. input amplitude using a 7.3KHz input signal. . 42

6.1 System overview of the second order Σ-Δ converter. 45
6.2 A 2nd order CT Σ-Δ feed-forward modulator. 46
6.3 Matlab simulation of the input to the quantizer with $a_1 = 1.5$ and $k_1 = 1$. 47

6.4 Matlab simulation of the input to the quantizer with $a_1 = 2.5$ and $k_1 = 156$. 47
6.5 Realization of the 2^{nd} order CT Σ-Δ modulator. 48
6.6 Simulation of the SR in the Op-amp in the second order Σ-Δ modulator. 49
6.7 Simulation result of the second order Σ-Δ modulator using 1024 points FFT, 1V input amplitude (-4.3 dBFS). 50
6.8 Simulation result of the second order Σ-Δ modulator, SNR/SNDR vs. Frequency. 51
6.9 CIC filter response of the second order Σ-Δ converter. 52
6.10 FIR filter response of the second order Σ-Δ converter. 53
6.11 FFT plot of an input frequency of 10KHz -3dBFS using 65536 points FFT. 54
6.12 SNR and SNDR vs. frequency using an -3dBFS input signal. 54
6.13 SNR and SNDR vs. input amplitude, using a 7.3KHz input frequency. 55

List of Tables

1.1 The outline of the thesis. 3

2.1 Xilinx Spartan-6 XC6LX9 FPGA Features (TQG144 package). . . . 6
2.2 LVDS I/O Standard Input Levels Xilinx Spartan-6. 7
2.3 Analog audio input signal specification. 7

3.1 α and β values for NRZ, RZ and HRZ DAC's. 19

5.1 Specification for the passive Σ-Δ ADC. 34
5.2 Component values for the passive Σ-Δ modulator. 36
5.3 Parameters of the CIC filter for the passive Σ-Δ converter. 39
5.4 FIR filter specification for the passive Σ-Δ converter. 40
5.5 FPGA resources used in the passive first order Σ-Δ Converter. . . . 43

6.1 Specification for the second order Σ-Δ ADC. 46
6.2 Component values for the loop filter in the second order Σ-Δ modulator. 49
6.3 OP-amp specifications. 50
6.4 CIC filter parameters for the second order Σ-Δ converter. 52
6.5 FIR filter specification for the second order Σ-Δ converter. 53
6.6 FPGA resources used in the second order Σ-Δ Converter. 55

7.1 Comparison between the A/D converters. Since the PCM1807 is a dual channel ADC, its resources are divided by two. 58

Bibliography

[1] Analog Devices. *Comparators*, September 2011. MT-083, Rev. A. Cited on pages 7 and 61.

[2] Pervez M. Aziz, Henrik V. Sorensen, and Jan Van Der Spiegel. An Overview of Sigma-Delta Converters: How a 1-bit ADC achieves more than 16-bit resolution. *IEEE Signal Processing Magazine*, 13:61, 1996. Cited on pages 10 and 11.

[3] Feng Chen and Bosco Leung. A 0.25-mW Low-Pass Passive Sigma-Delta Modulator with Built-In Mixer for a 10-MHz IF Input. *IEEE Journal of Solid-State Circuits*, 32(6):774–782, 1997. Cited on pages 34 and 35.

[4] Matthew P. Donadio. CIC Filter Introduction. July 2000. Cited on page 26.

[5] Julian M. Garcia. *Digitally Enhanced Continuous-Time Sigma-Delta Analogue-to-Digital Converters*. PhD thesis, KTH Royal Institute of Technology, 2012. ISBN: 978-91-7501-360-2. Cited on pages 10, 11, 12, 13, 18, 22, 23, and 61.

[6] Eugene B. Hogenauer. An Economical Class of Digital Filters for Decimation and Interpolation. *IEEE Transactions on Acoustics, Speech, and Signal Processing*, ASSP-29, No. 2, April 1981. Cited on pages 27 and 28.

[7] Texas Instruments. LMV793, July 9 2013. http://www.ti.com/product/lmv793. Cited on page 57.

[8] Texas Instruments. LMV794, July 9 2013. http://www.ti.com/product/lmv794. Cited on page 58.

[9] Texas Instruments. PCM1807, July 9 2013. http://www.ti.com/product/pcm1807. Cited on page 57.

[10] Zhang Jinghua. *Low-Voltage Low-Power Continuous-Time Delta-Sigma Modulator Designs*. PhD thesis, National University of Singapore, 2010. Cited on pages 8, 13, 14, 15, 17, 18, 19, 20, 23, 24, 25, and 61.

[11] Walt Kester. Which ADC Architecture Is Right for Your Application? *Analog Dialogue*, (39), June 2005. Cited on pages 8 and 61.

[12] Scott D. Kulchycki. Continuous-Time Sigma-Delta ADCs. *ADC12EU050*, January 2008. Cited on page 17.

[13] Lattice Semiconductor Corporation. *Simple Sigma-Delta ADC*, November 2010. RD1066. Cited on pages 2, 37, and 62.

[14] M-Audio/ Avid Technology, Inc. *Fast Track Pro User Guide*, 2010. Guide Part Number 9329-65014-00 REV A 05/10. Cited on pages 29 and 30.

[15] M. Ortmanns and F. Gerfers. *Continuous-Time Sigma-Delta A/D Conversion*. Springer, 2006. ISBN 10-3-540-28406-0. Cited on pages 23, 24, 25, and 26.

[16] Matthew Jeremiah Park. *A 4^{th} Order Continuous-Time Σ-Δ ADC with VCO-Based Integrator and Quantizer*. PhD thesis. Cited on page 24.

[17] Pavel Peev, Bart De Vuyst, Pieter Rombouts, and Anas A. Hamoui. An Anti-Aliasing Filter inspired by Continuous-Time Σ-Δ Modulation. Cited on page 21.

[18] Fabio Sousa, Volker Mauer, Neimar Duarte, Ricardo P. Jasinski, and Volnei A. Pedroni. Taking Advantage of LVDS Inpus Buffers To Implement Sigma-Delta A/D Converters in FPGAs. *IEEE International Symposium on Circuits and Systems*, 1, 2004. Cited on pages 6 and 61.

[19] Fabio Sousa, Volker Mauer, Neimar Duarte, Ricardo P. Jasinski, and Volnei A. Pedroni. Taking Advantage of LVDS Input Buffers to Implement Sigma-Delta A/D Converters in FPGAs. *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, 1:1088–1091, 2004. ISBN: 0-7803-8251-X. Cited on pages 2 and 7.

[20] Texas Instruments. *LVDS Owner's Manual Including High-Speed CML and Signal Conditioning*, Fourth edition. Cited on page 6.

[21] Texas Instruments. *PCM1807: Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo A/D Converter*, September 2005. SLES147. Cited on pages 1, 57, and 58.

[22] Texas Instruments. *LMV793/LMV794 88 MHz, Low Noise, 1.8V CMOS Input, Decompensated Operational Amplifiers*, 2007. Cited on page 50.

[23] Lars Wanhammar. *DSP Integrated Circuits*. Academic Press, 1999. ISBN 0-12-734530-2. Cited on pages 9 and 61.

[24] Lars Wanhammar. *Analog Filters Using MATLAB*. Springer, 2009. ISBN 978-0-387-92766-4. Cited on pages 24, 48, and 61.

[25] Xilinx. *Spartan-6 Family Overview*, v.2.0 edition, October 2011. DS160. Cited on page 6.

[26] Xilinx. *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*, v.3.0 edition, October 2011. DS162. Cited on pages 6 and 36.

[27] Axel Zimmermann, Endric Schubert, and Christian Grumbein. Integration of Analog-Digital and Digital-Analog Converters into FPGA-Based Microcontrollers. 2011. Cited on page 2.