Design of Heterogeneously-integrated Memory System with Storage Class Memories and NAND Flash Memories

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ABSTRACT
Heterogeneously-integrated memory system is configured with various types of storage class memories (SCMs) and NAND flash memories. SCMs are faster than NAND flash, and they are divided into memory and storage types with their characteristics. NAND flash memories are also classified by the number of stored bits per memory cell. These non-volatile memories have trade-offs among access speed, capacity and bit cost. Therefore, mix and match of various non-volatile memories are essential to simultaneously achieve the best speed and cost of the storage. This paper proposes a design methodology with unique interaction of device, circuit and system to achieve the appropriate configurations in the heterogeneously-integrated memory system for application.

CCS CONCEPTS
· Hardware → Non-volatile memory; Hardware-software codesign

KEYWORDS
Design methodology, Non-volatile memory system, Storage class memory, NAND flash memory

1 Heterogeneously-integrated Memory Systems with Non-volatile Memories
Heterogeneously-integrated non-volatile memory systems with storage class memories (SCMs) and NAND flash memories have been proposed [1, 2, 3]. Figs. 1(a) and 1(b) show write time of ReRAM [4] as a kind of SCMs and MLC NAND flash [2], respectively. The proposed memory system is put in practice by replacing one of NAND flash memories with SCM (Fig. 1(c)). However, SCMs and NAND flash memories have large access performance gap (Fig. 2). In the first place, memory-type SCMs (M-SCM), such as MRAM, have lower bit cost than DRAM, with higher access performance and smaller access size (512 Byte) than NAND flash. On the other hand, ReRAM, PRAM, and 3D XPoint are called storage-type SCM (S-SCM) [6]. In contrast, NAND flash memories have asymmetric as well as long read and write latencies. Multiple-level cell technologies such as MLC (multiple-level cell, 2 bits/cell) and TLC (triple-level cell, 3 bits/cell) achieve the larger capacity and lower bit cost with a drawback of the longer access time. Furthermore, NAND flash memories require garbage collection (GC) to reclaim free space (Fig. 3) [7] because of asymmetric access unit: read and write in page (16 KByte) and erase in block of multiple pages [8].

2 Design Methodology for Heterogeneously-integrated Memory System
This paper proposes step-by-step design methodology because optimizing four kinds memories such as M-SCM, S-SCM, MLC and TLC NAND flash at the same time is too complex. The previously proposed data management algorithms [2, 3, 9, 10], simply store frequently accessed hot data in fast M-SCM and S-SCM, and rarely accessed cold and frozen data in slow MLC and TLC NAND flash as shown in Fig. 4(a). Different memory combination is required to obtain the best performance because each application shows different workload characteristics. What's worse, the characteristics of non-volatile memories and applications are so complex that understanding the system-level performance of the heterogeneously-integrated memory systems is not straightforward.

This paper proposes the design methodology to optimize the complex heterogeneously-integrated memory systems with various non-volatile memories by means of the step-by-step design from 1-memory system to more hierarchical systems as shown in Fig. 4(b). The unique interaction of system, circuit and device are introduced. The device measurements results (Fig. 1) are input to transaction-level modeling based emulator [1] and the memory system performance is evaluated.

Figs. 5-8 describe the proposed design methodology, Step 1-4, and demonstrate its verification results with prxy_0 application [11]. MLC and TLC NAND flash capacities are optimized first. Then, M-SCM and S-SCM capacities are optimized. This approach is effective because there is a huge performance gap between S-SCM and MLC NAND flash (Fig. 2). Step 1 roughly determines the SCM and NAND flash capacity. Step 2 determines the detailed capacity allocation between MLC and TLC NAND flash. Step 3 determines the M-SCM and S-SCM capacities. Step 4 fine-tunes the capacity of M-SCM, S-SCM, MLC and TLC NAND flash.

First, in Step 1 (Fig. 5), the required SCM capacity is determined from input/output per second (IOPS) performance of M-SCM/MLC NAND flash hybrid system [9] by changing M-SCM capacity ratio. Because M-SCM stores frequent accessed data (Fig. 4(a)), prxy_0, which have frequent accessed hot data, requires larger M-SCM capacity and have IOPS jump with M-SCM capacity 1% and 10%.

Next, Step 2 (Fig. 6) determines how much capacity of MLC and TLC NAND flash memories are required from IOPS performance of Tri-hybrid system with M-SCM/MLC&TLC NAND flash [2]. Large TLC NAND flash capacity degrades IOPS performance (Fig. 6(a)) because W/E cycles of MLC NAND flash increase (Fig. 6(b)) and GC happens frequently. The key indicator is valid page destination of MLC NAND flash GC for frozen page screening: to MLC or to TLC NAND flash (Fig. 6(c)). Although TLC NAND flash has long memory access time, W/E cycles of TLC NAND flash does not show significant impact on the performance because TLC NAND flash stores rarely accessed frozen data. The frozen data eviction algorithm assures that data in TLC NAND flash are very infrequently accessed and W/E cycles of TLC NAND flash is much smaller than MLC NAND flash [12]. In Step 3, capacity of two types of SCMs are determined from IOPS performance of Heterogeneous Dual-SCM/MLC NAND flash memory system (Fig. 7(a)) [3]. To determine the memory capacity ratio between M-SCM and S-SCM, a constraint is applied that W/E cycles of M-SCM should be larger than that of S-SCM (Fig. 7(b)). Lastly, in Step 4 (Fig. 8), 3 types of memory systems are comprehensively compared in IOPS and IOPS/cost as figures of merit. The cost of system is defined as sum of (bit cost × capacity ratio) of the non-volatile memories. By considering memory cost, if TLC NAND flash is available, the best memory-combination is determined. For prxy_0 application, the Tri-hybrid system (S-SCM 10%, MLC NAND flash 78.8%, TLC NAND flash 11.2%) is the optimal. Yet, if developing TLC NAND flash is difficult and is not available, the Heterogeneous Dual-SCM/MLC NAND flash memory system (M-SCM 1%, S-SCM 9%, MLC NAND flash 90%) also achieve an excellent performance with reasonable costs. Note that energy consumption of the memory systems is inversely proportional to IOPS.

3 Conclusion
The design methodology for the heterogeneously-integrated non-volatile memory system is described (Figs. 5-8). By following the steps of the design methodology, the optimal non-volatile memory combination for application is determined and demonstrated.

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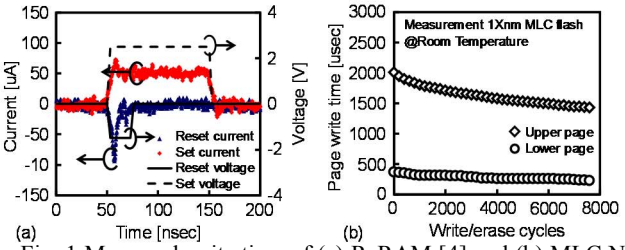

Fig. 1 Measured write time of (a) ReRAM [4] and (b) MLC NAND flash [2]. (c) Measured non-volatile memory system [5].

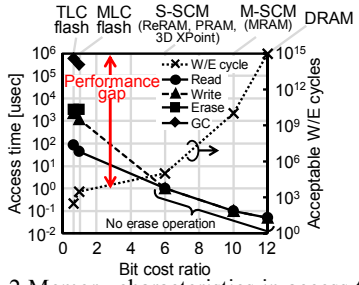

Fig. 2 Memory characteristics in access time, acceptable W/E cycles and bit cost [2].

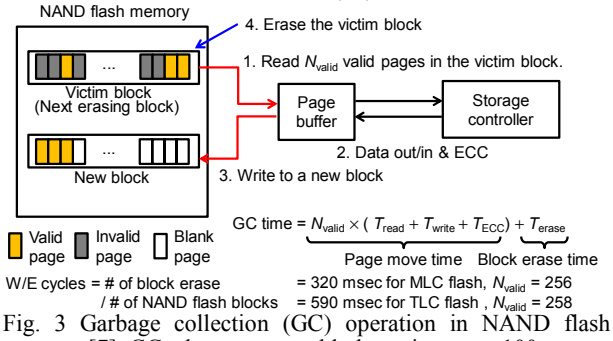

Fig. 3 Garbage collection (GC) operation in NAND flash memory [7]. GC takes unacceptably long time over 100 msec.

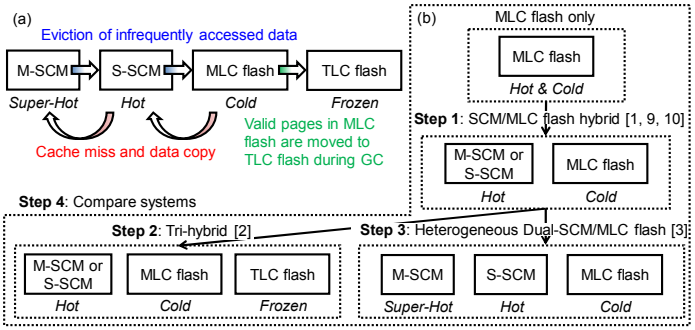

Fig. 4 (a) Data management algorithms that indicates relationship between memory and data characteristics. (b) Proposed step-by-step design methodology of heterogeneously-integrated non-volatile memories.

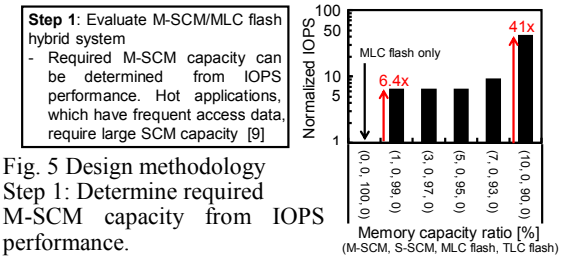

Fig. 5 Design methodology Step 1: Determine required M-SCM capacity from IOPS performance.

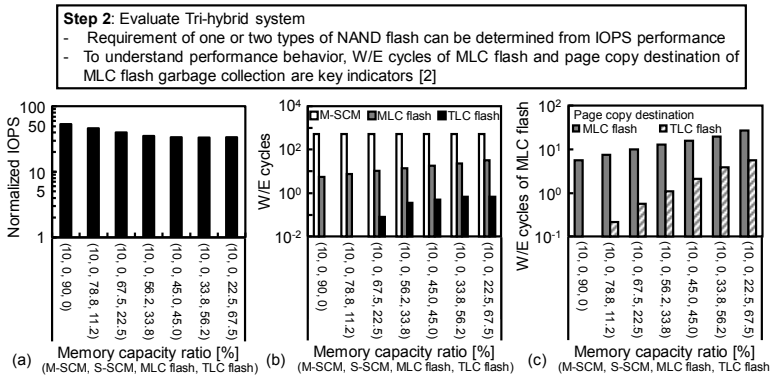

Fig. 6 Design methodology Step 2: Determine MLC/TLC NAND flash capacity ratio. (a) IOPS performance, (b) memory W/E cycles, and (c) Valid page destination of MLC NAND flash GC: MLC or TLC NAND flash.

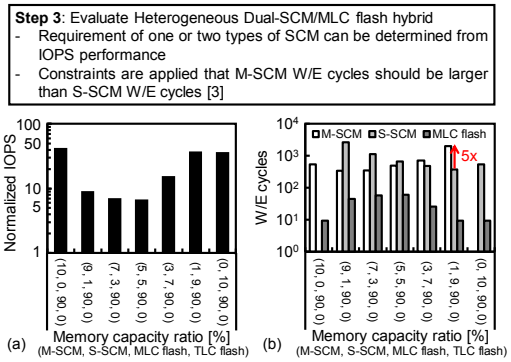

Fig. 7 Design methodology Step 3: Determine M-SCM and S-SCM capacity ratio. (a) IOPS performance and (b) memory W/E cycles.

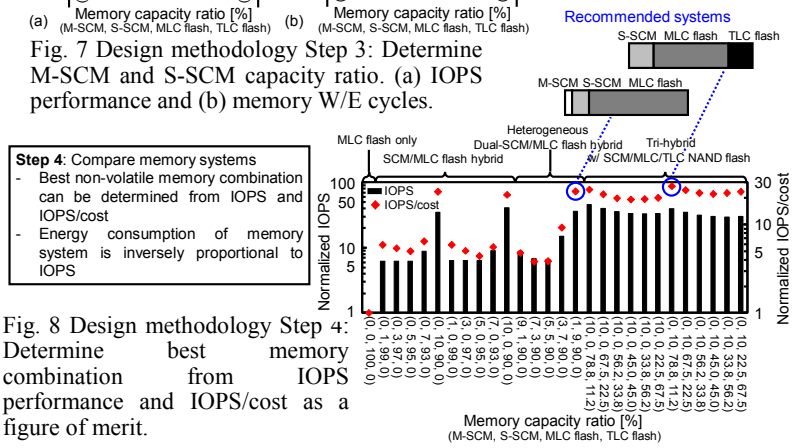

Fig. 8 Design methodology Step 4: Determine best memory combination from IOPS performance and IOPS/cost as a figure of merit.

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