Thesis Plan

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1 Outline

The current plan is to use the RPU core.

1. Test core to confirm functionality

2. Test for multicore potential

3. Think up tests and key metrics to judge from

4. Draw up schemes for hardware and software controllers for task scheduling

5. Find linux distro that will run on this shitshow

6. Figure out a comms protocol between the computer and the FPGA. I think there is a microUSB port that should do the trick.

7. Configure RPU for sprinting.