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BERNSTEIN GLOBAL VIEW

Mourning Moore's Law?

JUNE 2013

Tears, fears or cheers for Semiconductors?

Moore's Law has been the driving force behind virtually every technological advancement of the last 40+ years, as continually shrinking transistor size provides more performance, lower cost and power savings at every generation; but many fear that the Law is about to be broken

All may not be lost; while the pace of transistor shrink will undoubtedly slow, a solid fundamental case exists to carry shrink to 4-1.5nm by the end of next decade; however, the associated costs will rise considerably, with several potential outcomes for the industry

"Doomsday" scenarios are clear, as higher costs for consumers or semi players hinder demand or pressure margins; but there may be hope, with cost per chip salvaged through lower performance increase (and smaller dies) while power efficiency protects ASPs, and wafer additions slow

Rising complexity helps Litho & Metrology; slower wafer adds pressure other Semi-caps; Intel's business shift creates great uncertainty; we see Foundry margin compression; slower shrink improves Memory industry dynamics; rise of "mid-end" eventually shifts value from OSAT

SEE DISCLOSURE APPENDIX OF THIS REPORT FOR IMPORTANT DISCLOSURES AND ANALYST CERTIFICATIONS

Portfolio Manager's Summary

Even non-techies are familiar with Moore's Law, an observation that the number of transistors in a given silicon chip area doubles about every two years. And if one is not familiar with the Law itself, one is certainly familiar with the results; Moore's Law has been the driving force behind virtually every technological advancement of the last 40+ years. Continually shrinking the size of transistors provides more performance, lower cost, and power savings at every generation, a trifecta of benefits that has created unimaginable innovation and value for the world.

But many fear that this Law is about to be broken. Bernstein's Semis team undertakes a perilous look at how the future of Moore's Law may evolve, and ask whether industry players may finally be forced into "mourning Moore."

However, all may not be lost. While the pace of transistor shrink will undoubtedly slow, we believe a solid fundamental case exists to carry down to ~4 to 1.5nm critical dimensions, which (assuming the engineering challenges can be solved) provides a roadmap for shrink into the latter half of the next decade. The associated costs will rise considerably, with several potential outcomes for the industry. The "doomsday" scenarios are certainly clear. Higher costs passed to the end user could kill elasticity and structurally hinder end demand. And, should industry players be forced to bear cost increases in isolation, semiconductor margins would be massively pressured. Fortunately, there may be a path to industry salvation, particularly if the power-performance trade-off shifts. Cost savings ***per chip*** could be achieved through less performance increase (and hence, smaller dies), with pricing held via increased power efficiency. In this scenario industry economics could continue unabated, with higher-cost wafers offset by higher revenue per wafer, but with added wafer capacity slowing.

Overall, rising wafer costs are visibly good for Semi-cap, but slowing wafer additions mean the benefit is not to be shared equally. Litho and Metrology win, with spending driven primarily by complexity; others at least ultimately suffer, with spending driven mostly by wafer additions.

Intel is by far the king of semiconductor manufacturing, and it is likely the last in the industry to be forced into "Mourning Moore." However, as power efficiency, over time, trumps performance improvement, the resulting business model shift brings considerable uncertainty for it in the mid-term. For the foundries, the story is simple — we see margin compression on the way. Memory players may counter-intuitively benefit from "Mourning Moore," as higher costs force more rational supply growth and, consequently, better pricing.

And as for the back-end players, they have ***never*** benefitted from Moore's Law, but over the next few years, flip-chip adoption in mobile should drive value. Over the longer term, a migration to 2.5/3D packaging and the rise of the "mid-end" runs a risk of shifting value away from the OSATs, but not until the costs to implement the technology come down.

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Exhibit 1 Financial Overview

	US Semiconductors			European Semiconductors		Asian Semiconductors					Global Memory and Consumer Electronics					
	Intel	**Qualcomm**	**Broadcom**	**ASML**	**ARM**	**TSMC**	**UMC**	**SMIC**	**ASE**	**SPIL**	**Samsung**	**SanDisk**	**Micron**	**SK Hynix**	**Inotera**	**Nanya**
Ticker	**INTC**	**QCOM**	**BRCM**	**ASML.NA**	**ARM.LN**	**2330.TT**	**2303.TT**	**981.HK**	**2311.TT**	**2325.TT**	**005930.KS**	**SNDK**	**MU**	**000660.KS**	**3474.TT**	**2408.TT**
Rating	Underperform	Outperform	Outperform	Outperform	Underperform	Market-perform	Underperform	Underperform	Market-perform	Outperform	Outperform	Outperform	Outperform	Market-perform	Outperform	Underperform
Target Price	**18.0**	**80.0**	**41.0**	**70**	**550**	**107.0**	**8.7**	**0.55**	**27.0**	**42.0**	**2,500,000**	**75.00**	**14.00**	**35,000**	**14.00**	**1.20**
Currency	USD	USD	USD	EUR	GBp	TWD	TWD	HKD	TWD	TWD	KRW	USD	USD	KRW	NTD	NTD
Price on May 31st, 2013	23.9	64.1	36.5	64.26	988	109.5	13.2	0.6	25.8	35.1	1,538,000	59.02	11.68	32,200	12.75	6.05
Target P/E (2014E)	9.7	16.2	13.4	15.10	24.30	14.0	41.5	13.8	12.1	14.8	10.1	12.7	9.5	9.5	7.0	NM
Market Capitalization (millions)	119553	110426	20990	26899	14079	2838678	170966	20205	196132	109216	225,662,592	14,171	11,826	22,144,218	70,536	149,025
Sales (millions)											*Note: Sales for Samsung and SK Hynix are in KRW billions*					
FY 2012A	53341	19121	8006	4732	577	506249	115675	1702	193972	64655	201,104	5,053	8,234	10,161	35,296	32,479
FY 2013E	53816	24530	8634	5122	667	609410	123077	1987	208685	70201	239,887	5,734	8,708	12,641	42,862	40,603
FY 2014E	55880	27325	9527	7131	744	669151	128330	2092	224669	78890	256,689	6,787	15,020	13,772	48,665	50,781
EPS																
FY 2012	2.13	3.71	2.92	2.7	14.7	6.41	0.46	-0.02	1.76	1.83	153,929	2.38	(1.04)	(228)	(2.95)	(2.24)
FY 2013E	1.89	4.49	2.82	2.5	19.4	7.46	0.77	0.41	1.92	1.87	221,444	4.32	(0.24)	2,622	0.88	(0.17)
FY 2014E	1.85	4.93	3.07	4.6	22.6	7.65	0.21	0.54	2.23	2.83	248,287	5.91	1.48	3,696	2.00	(0.14)
P/E on SCB EPS Forecast																
FY 2012	11.2	17.3	12.5	23.9	67.0	17.1	28.4	N.M.	14.7	19.2	9.99	24.83	NM	NM	NM	NM
FY 2013E	12.6	14.3	12.9	25.5	50.9	14.7	17.2	1.5	13.4	18.8	6.95	13.65	NM	12.28	14.41	NM
FY 2014E	12.9	13.0	11.9	13.9	43.6	14.3	63.0	1.2	11.6	12.4	6.19	9.99	7.89	8.71	6.39	NM
P/S on SCB EPS Forecast																
FY 2012	2.29	5.88	2.64	5.62	24.09	5.61	1.48	11.87	1.01	1.69	1.12	2.80	1.44	2.18	2.00	4.59
FY 2013E	2.27	4.58	2.45	5.19	20.83	4.66	1.39	10.17	0.94	1.56	0.94	2.47	1.36	1.75	1.65	3.67
FY 2014E	2.19	4.11	2.22	3.73	18.68	4.24	1.33	9.66	0.87	1.38	0.88	2.09	0.79	1.61	1.45	2.93

Note: The stocks are benchmarked against the S&P 500, MSCI Asia Pacific ex Japan, MSCI Europe Local and MSCI Emerging Markets indexes, which had closing prices of 1630.74, 464.98, 1257.17 and 1016.02, respectively, on May 31, 2013.

Source: Capital IQ, Thomson, corporate reports and Bernstein estimates and analysis.

Significant Research Conclusions

Over the last year, we have had many questions from investors about the long-term prospects of the semiconductor industry. Our *Blackbook* considers how the semiconductor industry's main driving force — Moore's Law — is likely to evolve.

Moore's Law Is the Single Most Important Driver of Value Creation in Semiconductors (and Beyond)

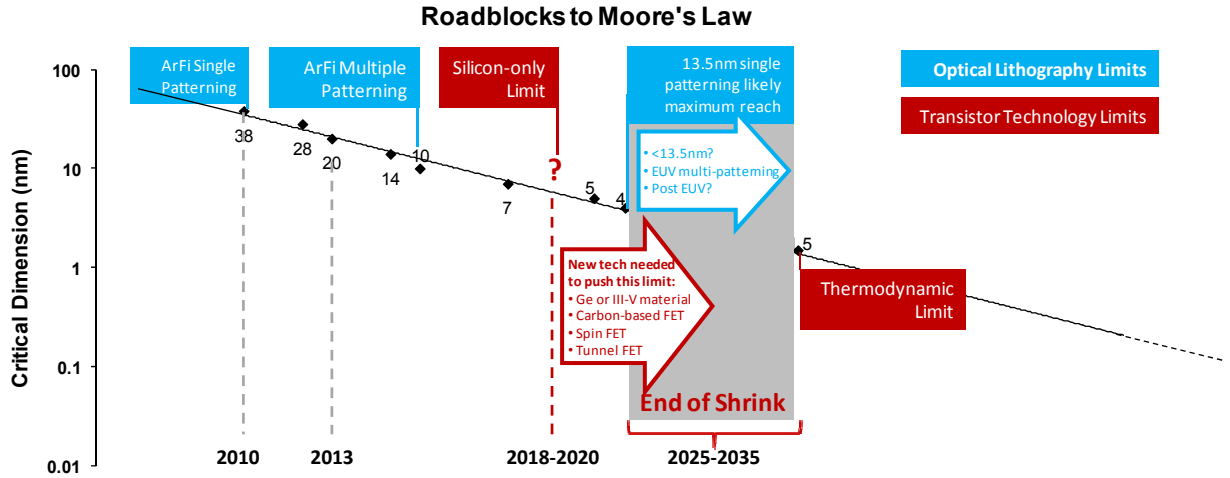
Moore's Law drives performance enhancement, which in turn drives replacement dynamics. It also drives cost efficiencies, which in turn drives elasticity-driven growth and last but not least technological challenges, all of which drives defensible competitive advantages and rights to make money across the value chain. A semiconductor industry without Moore's Law would look very boring.

However, Moore's Law Has an Absolute Physical Limit

The power required to switch a transistor from one state to another has a thermodynamic limit. Based on the Shannon-von Neumann-Landauer expression, 0.017 eV is required as a minimum energy level to change the state of a bit at room temperature, whatever its physical implementation. A switching power limit introduces a dimensioning limit. Linking this back to Heisenberg's uncertainty principle, we can conclude the minimum feature size of a transistor has to be above 1.5nm. This reduces the time horizon of Moore's Law to somewhere around 2030.

However, there are roadblocks on the way to 1.5nm (see Exhibit 2). Virtually no process step is exempt from challenges as we move to lower feature sizes. As transistors become smaller, leakage current becomes a greater problem. We will need new Lithography light sources with narrower wavelengths than EUV. Material challenges for interconnect layers will surface soon, similar to those described above for transistor layers, and the increase in power density poses a material challenge as well, as do metrology, test, defect detection and measurement of 3D structures. If none of these barriers appear insurmountable, their combination is clearly changing the economic side of Moore's Law and increasing the chances of roadmap slippage and slower node transitions.

Exhibit 2 **Moore's Law Has a Hard Stop at 1.5-4nm in 2025-35, With Many Roadblocks Ahead**



Source: Bernstein estimates and analysis.

What Are the Implications for the Industry Going Forward?

The end of Moore's Law is often viewed as the dusk of the industry. Our research suggests the mourning of the Law will actually last a long time and keep the industry going, but at a cost. We see three potential scenarios.

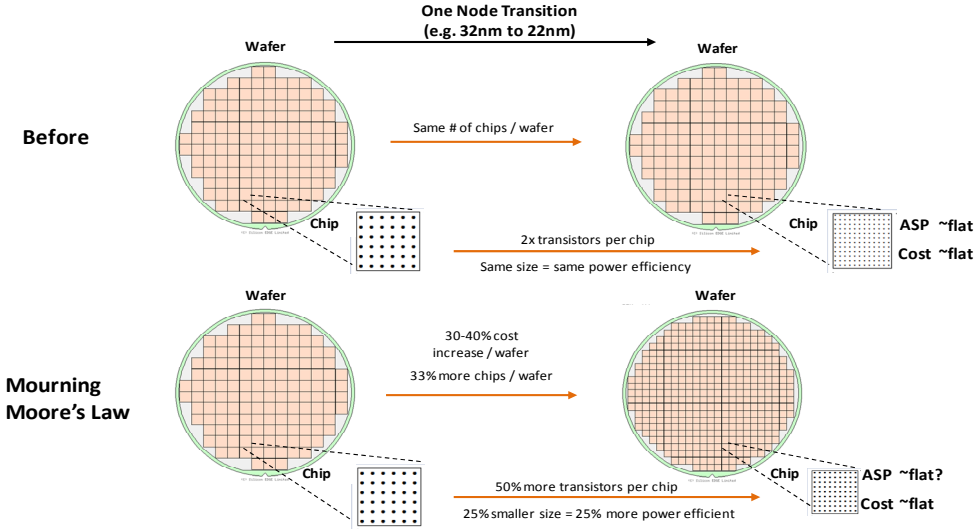
1. The mourning of Moore's Law affects end-demand: Elasticity matters on the demand side, and end-markets cannot absorb broad cost increases. With manufacturing costs increasing, unit shipment growth slows down, squeezing the industry for some time to come.

2. The mourning of Moore's Law squeezes margins: Manufacturers continue to deliver a steady improvement in performance, but at an increasing cost. Competition keeps the chase for incremental demand challenging, at best keeping chip ASPs on their historical trajectory, i.e., not enough to keep up with increasing costs. Margins pay the bill.

3. Power efficiency matters and saves the industry: As the decline in cost per transistor flattens, manufacturers slow the increase in transistor count per chip, delivering less incremental performance, but more power efficiency, as die sizes come down. This is valued by customers and keeps chip costs stable (even as wafer costs rise), and end-demand intact. As a result, units and revenues stay on steady historical trends, but wafer addition slows.

In all cases, we expect capex going forward to grow faster than it has in the past. However, there is no consensus in our team on which scenario is most likely to be realized, even if we agree that the first two scenarios put material pressure on the industry's economics. We believe the third scenario is a possible savior for the industry, if it can find a way to keep charging the same for slower transistor growth but greater power efficiency at every node transition (see Exhibit 3).

Exhibit 3 The Industry Could Preserve Its Economics If It Can Keep Charging the Same for Slower Transistor Growth But Greater Power Efficiency at Node Transitions



Source: Bernstein estimates and analysis.

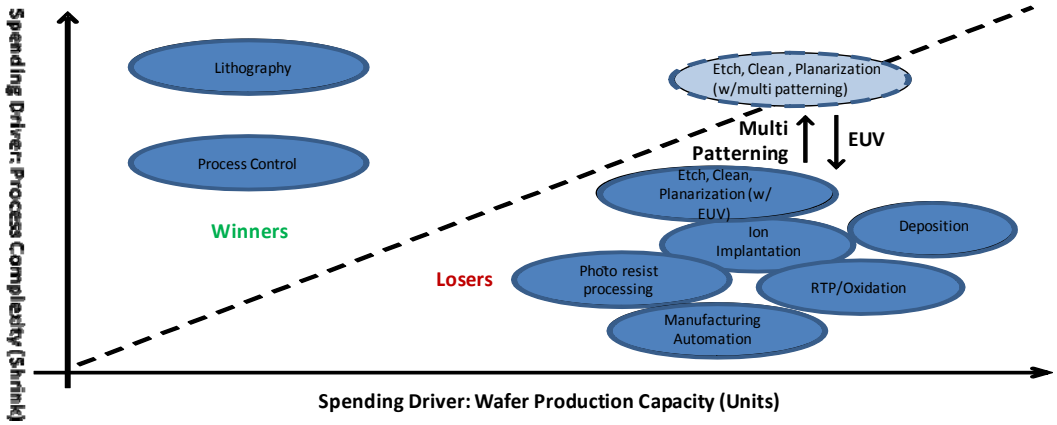
We Expect Equipment Spending to Continue to Rise…

In our most conservative scenario for equipment manufacturers (i.e., Scenario 3), as wafers get more expensive to produce, we expect the number of chips per wafer to increase, balancing out the increase in cost per wafer and keeping industry capex as a percentage of sales flat, versus a structural decline in the past. In more cautious scenarios, in which manufacturers can't reduce the average die size and either destroy end-demand, passing on cost increases to customers, or take a significant margin hit, capital intensity would increase significantly more over time.

...But This Doesn't Imply All Equipment Manufacturers Will Benefit

Winning segments are process steps at the origin of the increase in cost per wafer**:** Lithography, Process Control. **Losing segments** suffer from the decline in wafer additions we anticipate under the combined effect of increasing costs per wafer and the 450mm migration — Etch, Clean and Planarization, Deposition, RTP/Oxidation, Ion Implantation and Manufacturing Automation (see Exhibit 6).

Exhibit 4 Growth Drivers for Semi-Cap Equipment: Process Complexity and Wafer Additions



Source: Bernstein analysis.

We expect Lithography and Process Control to grow at a much faster rate than the overall semi-cap market: 8% p.a. and 7% p.a., respectively, in the long term, versus 4% p.a. for semi-cap equipment spending. As a reference point, these long-term growth rates in the past have been 4%, 3.6% and 2.1%, respectively. We expect all other process steps to experience only anemic growth — 1.4% p.a. going forward versus 1.6% p.a. in the past.

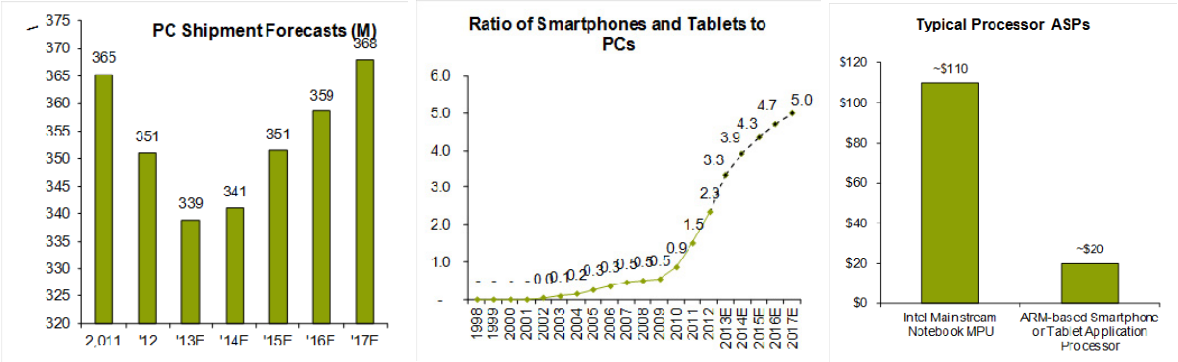
In our coverage, **ASML** is a structural winner and remains a top pick. We see **KLA Tencor, Hermes, NuFlare, Rudolph and Nanometrics** as "the winning group" and appear to stand to benefit the most from the mourning of Moore's Law. For most other semi-capital equipment players (**Tokyo Electron**, **Dainippon Screen, Kulicke & Soffa, BE Semiconductor, Hitachi Kokusai Electric and Mattson Technology, AMAT, LAM research**, **Advantest, Teradyne and LTX-Credence),** mourning Moore's Law equates to some secular headwind and we note that these companies trade at a wide range of multiples across several key valuation metrics.

Intel's Manufacturing Leadership May Allow It to Navigate an Industry Shifting from Performance to Power, But the Journey Is Likely to Be Perilous

As the increasing technical and engineering difficulties around shrink intensify and the economic drivers of Moore's Law abate (replaced by, at best, a race for power efficiency), scale and technology will remain the dominant factors for success. However, the IDMs may in fact be better positioned along these lines to win versus the pure-play foundry incumbents, with Intel in particular poised as a primary disruptor.

While Intel's new products look very good in regard to power efficiency, this shift is unfortunately accompanied by a change to the business model, as new ultra-mobile markets will not support the high ASPs that Intel generates in its core PC market today. Pricing that is ~one-fifth of Intel's current ASPs virtually insists that Intel invest for the prospect of huge share gains in order to drive any sort of upside, implying no way to take its foot off the gas. And, 450mm wafers will be required to preserve margins as growth is driven by armies of $20 chips. These imply elevated investments must continue even as the core business slows (see Exhibit 5).

Exhibit 5 **While the PC Isn't Necessarily Dead, Smartphones and Tablets Are an Increasing Percentage of "Computing" Unit Growth, With Much Lower ASPs**



Source: Gartner, Strategy Analytics and Bernstein estimates and analysis.

Intel Is Also Leveraging Its Lead to Disrupt Foundry Competitors; Could Apple Be a Wildcard?

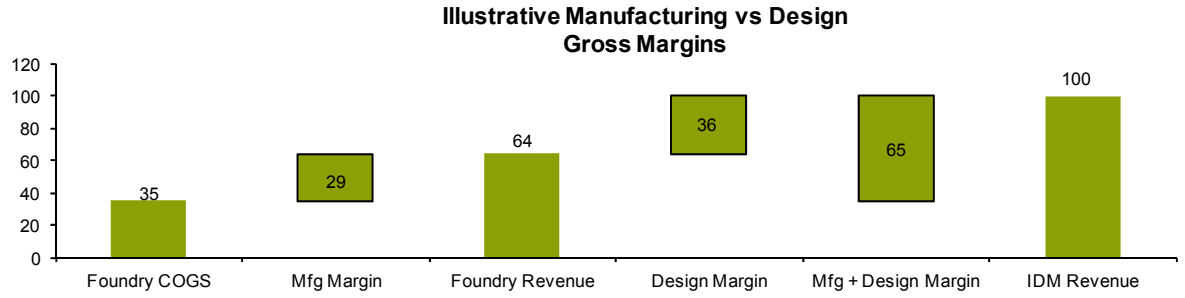
Intel is also attempting to leverage its manufacturing leadership into the foundry market. It is starting with low-volume (but high-value) customers, learning the foundry business model, as well as picking off high-value leading-edge customers (like high-end FPGAs) in an attempt to disrupt the competition (a benefit likely far bigger than earnings upside at this point).

Of course, the majority of pure-play foundry leading-edge volume today is mobile SoCs, which (unlike high-end FPGAs) do not come with quite as attractive economics for someone like Intel (see Exhibit 6). Additionally, the strategic issues are hugely intensified given Intel's own goals to grow strongly with its own products into the same markets.

Apple could, however, be a wildcard. In fact, Apple sits with a foot in both camps, both a potential strategic partner as well as a competitor, and strategic issues (from Intel's point of view), while not non-existent, may be less. However, the economics for Intel for such a large-volume foundry play appear, at least from capital intensity/ROIC basis, troubling, making the adverse capital intensity trends we see impacting the company even worse.

Nevertheless, the solidity of Intel's Moore's roadmap in fact makes it a very credible threat to competitors (namely, the existing foundry ecosystem) as it exploits "roadmap risk" at current incumbents. This could manifest itself through direct success in mobile (adversely affecting the trajectory of the foundries' current major customers), picking off high-value "strategic" targets (e.g., Altera, Cisco) or selectively attacking larger options (Apple), or casting the die on a much broader leading-edge foundry push should all other options fail.

Exhibit 6 **The Profit Pool of General Foundry Is Generally Shallower Than That of an IDM**



Source: Gartner, Strategy Analytics and Bernstein estimates and analysis.

Greatly Increasing Investment in the Wake of a Slowing Market May Pressure Cash Return, Long a Point of Stability for Intel's Stock

Elevated capital intensity, combined with challenging end-market growth, means that Intel's cash return, long simply taken as a given, could now be reaching a somewhat less secure point. Already, future buybacks at current levels can no longer be covered by the company's cash generation. And, while we do not forecast anything as severe as a cut to the dividend at this point, it is not quite as laughable an idea as it might have been a few years ago, and we do believe a plausible case can (at a minimum) be made for the pace of cash return increases to slow versus history.

Longer Term, Accelerating M(o)ore Investments May Be a Winning Strategy, But the Journey Is Likely to Be Painful

Longer term, accelerating investments may be a winning strategy, but the journey is likely to be painful. One can postulate an end-game (say, five years or more out) in which Intel still owns whatever is left of the PC market, and additionally deploys its process technology advantage to further capture value as the industry's focus shifts more to power efficiency. Thus, it could leverage its increasing technology gap to become a formidable player in new markets such as smartphones and tablets. However, massive capex and investment will be necessary to craft a company capable of dominating these markets, but which (in a bit of a chicken-or-egg manner) also requires market dominance (e.g., significant unit share) to fill the capacity the investments will put into place. We believe the path that Intel is on is likely the right one for the company given the nature of the battle and the weapons it brings to bear, but that the act of transformation is likely to be very painful for investors during a multi-year transition period.

Historically, the Rising Cost of Moore's Law Is a Friend to Foundries as It Pressures IDMs to Outsource to Foundries

Since its birth two to three decades ago, the foundry industry clearly has demonstrated the merits of its business model. In addition to the growth due to the fabless industry, the additional outsourcing of IDMs is also a very important contributor to a foundry's success. By sharing assets with a larger and more diversified customer base, foundries better use their expensive manufacturing assets and hence provide lower cost that very few IDMs can match. Although the foundries have faced the rising costs of advancing Moore's Law for a very long time, the rising cost burden actually helped them as most IDMs found it difficult to reach sufficient scale to be economical and turned to the foundries for help. Hence somewhat counter-intuitively, the cost pressure actually has been the foundry's friend.

The industry, in particular the leader TSMC, has also risen higher as the semiconductor growth shifts from PCs to mobile devices. The combination of foundries and fabless companies trumped IDMs as seen by the fact that by 2011, a quarter of the semiconductor value had shifted to the fabless companies.

However, the Cost Increase Now Has Escalated to a Point That It Can Become an Enemy to Foundries; the Secular Growth of Mobile Devices Also Invites Stronger Competitors, Including in Apple's Foundry Business

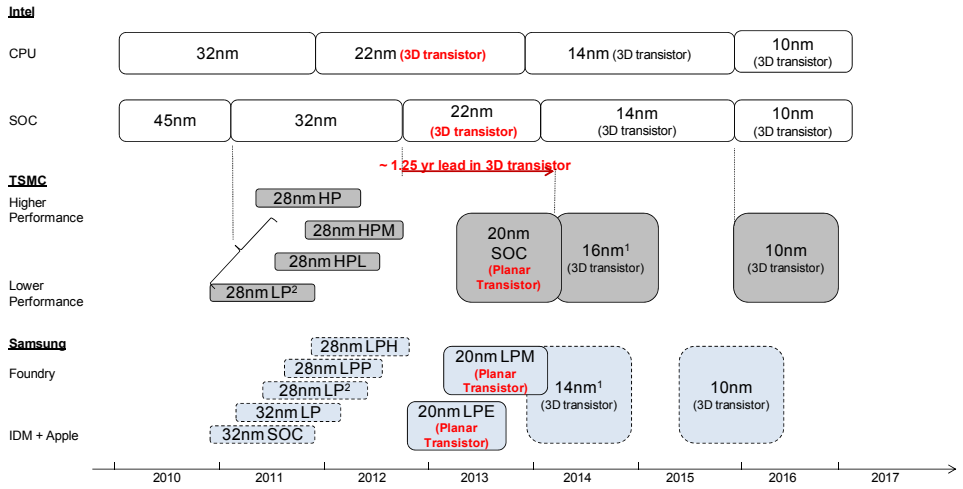
But now we see challenges to this trend. Once a friend to foundries, the cost increase now has risen to a point that the economics of Moore's Law faces a slow death. Even TSMC is feeling the pressure, and is forced to either absorb the rising costs, or transfer the burden to customers but run the risk of hindering the demand growth.

Meanwhile, facing the rapid shift to mobile devices, as discussed earlier, Intel is making large investments in process technology. If Intel continues on its current trajectory, it is expected to command a lead in process technology versus TSMC over the next two to three years (see Exhibit 7). Also as noted earlier, on the one hand, Intel is a credible contender for Apple's foundry business, on the other hand, success of Intel's own mobile SoCs could also be a threat for TSMC's customers. In either scenario Intel's success would be a negative to TSMC.

Samsung's Vertical Integration Allows It to Be More Self-Sufficient in Logic IC, Also Posing a Threat to TSMC's Customers and TSMC

As for Samsung, as the high cost of advanced technologies casts doubt on the growth prospects of the memory business, the company is moving into logic IC for growth opportunities with rising intensity. Samsung now has sufficient demand from its internal handset, tablet, and PC divisions to support a sizable logic IC business with competitive cost structure. Its capability in logic IC such as application processor, baseband, etc., is also improving quickly. Extrapolating from the current progress, we find Samsung likely would become much more self-sufficient in logic ICs in the next few years, leaving a smaller market available for TSMC's customers and TSMC.

Exhibit 7 Intel's Process Technology Is More Advanced Than TSMC's and Samsung's



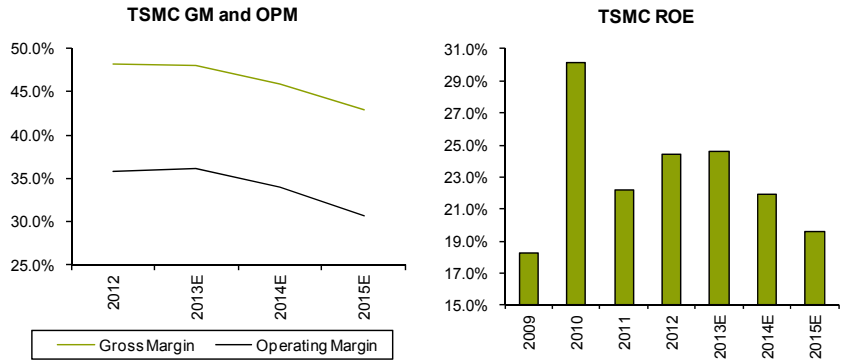
Note: Dotted line refers to SCB estimate. Solid line is company reported. 1. TSMC's 16nm, GlobalFoundries' 14XM and Samsung's 14nm are all "3D transistor version of 20nm." They are similar technologies and deliver comparable performance. 2. Poly/SiON flavor.

Source: Corporate data and Bernstein estimates and analysis.

We Therefore Expect Margin Compression at TSMC in the Next Few Years

As for TSMC, we continue to forecast margin deterioration because competitive pressures from Intel and Samsung hinder its ability to transfer the cost of leading technologies to customers (see Exhibit 8). Even if TSMC manages to pass on the cost increases to customers, the risk of demand loss from price-elasticity cannot be ignored. Considering its high valuation, we don't find favor in the risk/reward trade-off at current levels and therefore maintain a cautious stance on TSMC.

Exhibit 8 TSMC's Margins and ROE Are Expected to Deteriorate in 2014 and 2015



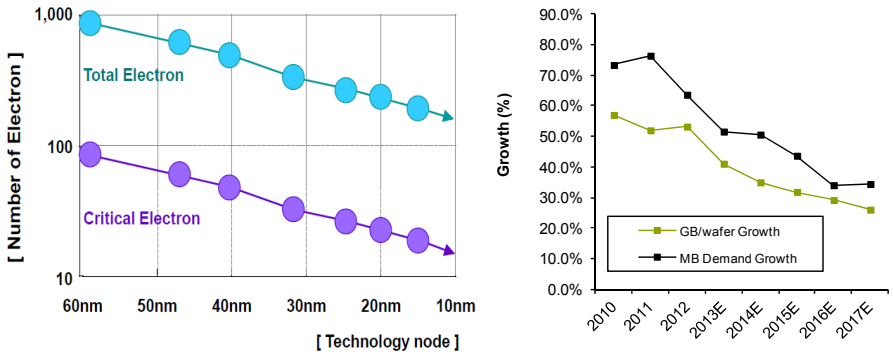
Source: Corporate data and Bernstein estimates and analysis.

NAND Will Soon Face Scalability Challenge at the 10-12nm Level; However, This Is Good for NAND Economics

For NAND, on the technology side and as NAND scaling continues, the number of critical electrons is expected to fall to only 10 at sub-1xnm design level, implying shortage of electrons to store multiple states in a cell. We estimate 78% of NAND is currently produced on 20nm-class.

As scaling continues and complexity increases, capex is also increasing. Furthermore, this increased complexity means cost declines are slowing. Without new wafers, the GB/wafer growth is not enough due to technology constraints, hence the need for an additional 475 KWPM wafer capacity by 2017 (see Exhibit 9). At today's prices, NAND makers do not make adequate returns (we estimate 3% ROIC at 23% 2012 NAND industry gross margins). NAND ASP would have to increase 31% from 1Q:13 level to get to 45% NAND gross margin (the level required to generate 12% ROIC).

Exhibit 9 **The Number of Critical Electrons Will Fall to Only 10 at Sub-1xnm Design Rule ASPs; Without New Wafers, the GB/Wafer Growth Is Not Enough Due to Technology Constraints**

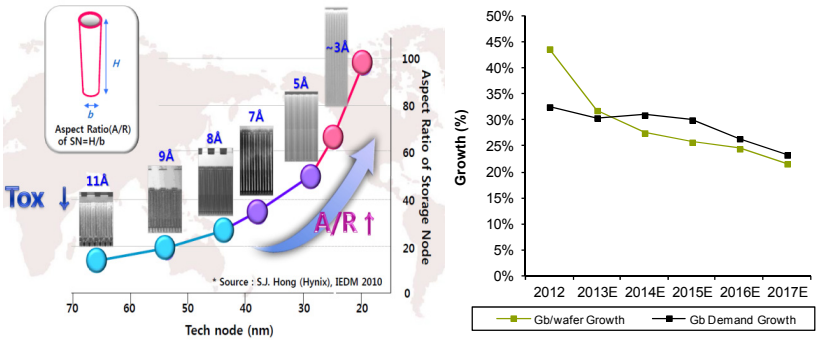


Source: SK Hynix, Gartner and Bernstein estimates and analysis.

We See DRAM Shrink Also Slowing, Which Is Causing Supply Growth to Slow Dramatically

The historical exponential cost per GB reduction may not continue as the current technology faces limitation. Even though it still has several more legs to advance than NAND, it is becoming increasingly questionable if current DRAM technology will be able to maintain the storage capacitance in decreasing cell area past 1xnm products. One of the critical challenges DRAM faces is high aspect ratio. At 3xnm, the aspect ratio (trench depth/diameter) of DRAM's cell capacitor already reached 25x, which is much higher than the world's tallest building Burj Khalifa's aspect ratio of 6x (see Exhibit 10). We see DRAM shrink slowing, which is causing supply growth to slow dramatically. Supply/demand balance will remain structurally better going forward.

Exhibit 10 **The Aspect Ratio of Capacitors Becomes Too Large as Node Shrinks; GB/Wafer Growth Is Falling Behind Demand Growth Due to Technology Constraints**



Source: DRAMeXchange, Gartner, SK Hynix and Bernstein estimates and analysis.

New Memory Technologies Needed to Extend Scaling in the Next Decade

The limitations of conventional memory devices have provoked needs for new memory technologies, and currently, there are many types being developed by both research institutions and commercial semiconductor tycoons.

2D NAND will likely co-exist with 3D NAND for several years, but has the potential to be at least partially replaced by ReRAM or 3DReRAM in the next decade. For DRAM, we do not see any viable candidate for replacement, but it may be slightly cannibalized around the edges by PCRAM, STT-MRAM and even NAND. Regardless of which technology wins here, the leaders, we have no doubt, will be the incumbents (Samsung and SanDisk in particular).

Unlike Wafer Manufacturing, IC Packaging Industry Does Not Have the Equivalent of Moore's Law; as a Result the Two Industries Have Different Growth, Market Valuation, Economics and Competitive Dynamics

Unlike the wafer manufacturing, the semiconductor packaging industry does not have the equivalent of Moore's Law. The packaging industry indeed has been constantly innovating and creating value, but the pace of technology advancement is slower than that of Moore's Law. The wafer manufacturers therefore demonstrate much stronger growth than the IC assemblers in revenue and profitability, and are better rewarded by investors.

The two industries also have very different competitive dynamics. Foundry is a business in which the winner takes all, as technology leadership is crucial to high profit, which further propels R&D to sustain technology leadership. This is evidenced in TSMC's steady market share increase. In the packaging industry, on the other hand, the absence of Moore's Law and the lower capital requirements make technology and scale much less critical, and high return on investment is mostly driven by operation efficiency. We also don't see any sign of the large players steadily gaining share. The two industries have also been maintaining a very symbiotic partnership, each providing its value to customers and collectively offering complete manufacturing services to fabless companies.

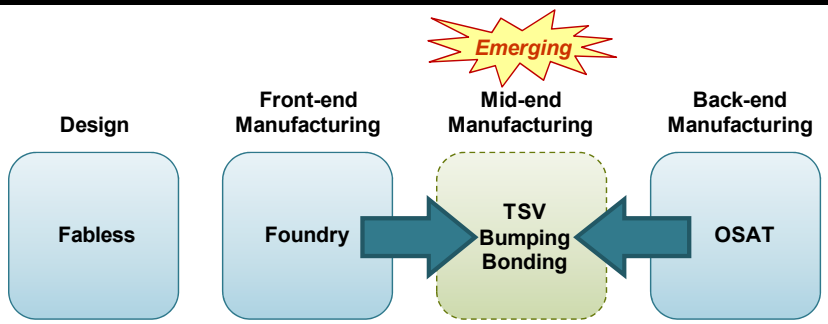
The Emergence of "Mid-End" Begins to Challenge the Partnership Between Frontend (Wafer Manufacturing, i.e. Foundry) and Backend (IC Packaging, i.e., OSAT)

Recently, as the challenges of Moore's Law mount, foundries have begun to explore other means to sustain the growth momentum, most notably by bringing wafer-/silicon-based technologies into packaging. As a result, the long-held symbiotic relationship between foundries and OSATs is put under unprecedented stress. Many innovative technologies are being developed now, most notably bumping or wafer-level package in the near term and 2.5D/3D IC in the long term. These technologies emerge from the intersection of front-end (wafer manufacturing by foundries) and back-end (IC packaging by outsourced semiconductor assembly or testing, or OSAT) and are commonly referred as "mid-end." As they represent meaningful future growth opportunities that both foundry and OSAT possibly can capture, there is a rising rivalry between the two industries (see Exhibit 11).

In the near term, bumping is gaining popularity due to the adoption of flip chip. Bumping is a wafer-based process and can be performed at foundries or OSAT companies. However, it counter-intuitively does not create tension between foundry and OSAT because of low margins. The rest of the flip chip package process is quite profitable but foundries have no interest in this. We believe that flip chip adoption in mobile applications is the most important technology trend in the OSAT industry in the next one to two years. SPIL, in particular, has high exposure to this trend and therefore is the top pick of our coverage.

In the long run, 2.5D/3D IC shifts value from OSAT and substrate sector to foundries. It is arguably the most promising technology in the "mid-end." As many wafer manufacturers invest heavily to develop this technology, we've seen growing friction between foundries and the OSAT companies. However, we believe that high cost will keep it from mass adoption in the near future, and that a de-rate on OSAT is unwarranted. Among Intel, TSMC and Samsung, we think the vertical integration at Intel and Samsung will help them bring 2.5D/3D technology to the market earlier, while TSMC risks falling behind.

Exhibit 11 **Both Foundry (Front-End) and OSAT (Back-End) Industry Are Vying for the Emerging "Mid-End" Business**



Source: Bernstein research.

The Backend Industry Will Still Be Impacted by the Slowing Moore's Law, Although the Ramifications Can Be Very Different Depending on Investment Horizon

In conclusion, the absence of Moore's Law is no guarantee that the back-end industry can survive the slowing of Moore's Law unaffected. The ramifications, however, can be very different depending on investment horizon.

Near term, we're comfortable with the growth outlook of ASE and SPIL in light of their exposure to mobile applications and flip chip. We expect the subtle balance between foundries and OSATs in bumping will be maintained.

Medium term, 2.5D/3D IC will remain too expensive to become a meaningful headwind on OSATs. We don't project it would be a significant growth area for foundries either.

Long term, the emergence of "mid-end" likely will tilt the competitive landscape in favor of foundries. However, we remain doubtful this will be able to fully offset the mounting burden in the core business as the slow death of Moore's Law takes its toll.

Valuation Methodology

Our price target for ASML at €70 corresponds to 15x 2014 earnings. For ARM, we arrive at £5.50 target at 31x 2013 earnings. For INTC, we apply a ~10x multiple to our 2014 EPS estimate ($1.85), yielding a price target of $18. We value QCOM by setting target multiples of 17x P/FE and set our target price at $80. We value BRCM by applying a ~18x multiple (~1.4x relative on a ~13x market multiple) to our "adjusted GAAP" EPS resulting in a $41 target price. We value TSMC at 3.2x NTM BV excluding intangible assets and goodwill. We value UMC at 0.55x NTM BV and SMIC at 1x NTM BV. We use historical average price to one-year forward earnings of 14.8x to value SPIL. Our target multiple for ASE is based on P/FE of 12x. Our KRW 2.5 million target price for Samsung represents ~10x our 2014 diluted EPS. Our $75 TP for SNDK is based on a 2014 P/E of 12.7x. Our KRW 35,000 target price for SK Hynix Inc. is based on 2.1x 2Q:14 book value of KRW17K. For MU, our $14.0 TP is equivalent to 8.5x CY 2014 EPS and 1.7x one year forward tangible BVPS. Our NT$14.0 price for Inotera Memories Inc. is based on 7x 2014 EPS and 2.2x 2Q:14 BVPS. Our NT$1.2 price for Nanya Technology Corp is based on a P/B multiple of 1.3x applied to book value per share forecast for 2Q:14.

Risks

Semiconductor, memory, and semi-cap equipment sectors are exposed to general macroeconomic risks, which ultimately influence end-market demand and can positively or negatively affect the entire electronics supply chain. In addition, the industry has historically been subject to seasonal and cyclical demand fluctuations for its products or services as well as technological, competitive, execution, and currency risks among others. Beyond the broader macro environment, several company-specific risks may influence the stocks in our coverage. (Please see Appendix for company-specific risks.)

Investment Conclusion

We believe **ASML** benefits almost exclusively from lithography's increasing share in equipment spending. We think the company can grow earnings by over 30% p.a. between 2012 and 2015, driven by top-line growth, margin expansion and share buyback. We rate the stock outperform with a €70 price target, corresponding to 15x 2014 earnings. We maintain our underperform rating and GBp 5.50 target price on **ARM**, as the stock has reached unsustainable valuation levels.

While longer-term investments in driving Moore's Law may very well be a long-term winning strategy, over the next two to three years **Intel** is faced with a stagnant or declining core PC market and uncertain prospects for success in fast-growing tablet and smartphone markets. Meanwhile the massive capex and investments required to win, as well as structural market shift to lower-priced devices, is likely to pressure Intel's cash flows and earnings over the next several years; we rate it underperform, TP $18. **Qualcomm, Broadcom,** and other fabless players may benefit to an extent from slowing Moore's Law particularly if this leads to commoditization of process technology resulting in lower wafer cost inflation and if design, rather than process technology, becomes the key differentiator; but if not, it could also face headwinds particularly if Intel places material pressure on a foundry space that cannot keep up. We rate Qualcomm outperform, TP $80; BRCM outperform, TP $41.

Despite **TSMC**'s leadership in 28nm and high exposure to mobile applications, the long-term challenges from Intel's and Samsung's competition (directly and indirectly) and cost escalation are mounting. Apple's business is an upside but is priced in already. Valuation is full and we therefore rate it market-perform, TP NT$107. **UMC**'s profitability and earnings are expected to deteriorate in the next few years as its small scale and thin profitability are not sufficient to cope with the high capex requirement of new technologies. We suggest investors sell the stock when it has short-term rebounds, rated underperform, TP NT$8.7. We believe **SMIC**'s emphasis on profitability shields it from the structural challenges in leading technologies. However, there are risks from small scale, UMC's competition and lagging technologies. The current valuation is unrealistic, rated underperform, PT HK$0.55. We think **ASE** is well exposed to the strong demand of advanced package used in mobile devices and can be a possible beneficiary in Apple's move to TSMC. Competition concern from foundries' entry into its space is overdone. We rate it market-perform, TP NT$27. We think **SPIL** is well positioned to benefit from the growth from flip chip and MediaTek and substantial EPS expansion is achievable this year. Competition concern from foundries is overdone. SPIL possibly can benefit from Apple's business when it's moved to TSMC, rated outperform, TP NT$42.

Samsung Electronics: DRAM scaling, similar to NAND, is coming close to the end and each node is becoming progressively more difficult. As shrink slows, more wafer capacity is required to keep up with demand growth. This complexity also further discourages new entrants as cost of entry is higher than ever. We believe this is very positive for DRAM and NAND margins going forward. Samsung is also emerging as a disruptive force in Logic and we believe the company is very well positioned in handsets, display and TVs, we rate Samsung Electronics outperform, TP KRW 2.5 million. **SanDisk Corp:** Technological uncertainty is higher than ever as NAND process technology moves to the bleeding edge of semiconductor technology. This in turn increases the financial hurdle required to make new NAND capacity investments. 3D NAND manufacturing will be necessary, but it is complex and may use different tool-sets. We rate SanDisk outperform, TP $75. **SK Hynix Inc/Micron Technology:** Both DRAM and NAND shrinks are slowing. SK Hynix and Micron are unwilling to invest in new capacity. This is very positive for both DRAM and NAND margins going forward. We rate Micron outperform, $14.0 TP. We rate SK Hynix market-perform, TP KRW 35,000. **Inotera Memories Inc/Nanya Technology Corp:** DRAM scaling is coming close to the end. We rate Inotera outperform, NT$14.0 TP and we rate Nanya underperform, TP NT$1.2.

Speculative Thoughts on the Long-Term Evolution of the Semiconductor Industry

Our *Blackbook* takes a perilous look at how the semiconductor industry's main driving force — Moore's Law — is likely to evolve. We are not first to do it and won't be the last, and past experiences also tells us most of what we will try and anticipate here will prove wrong. We nevertheless develop a framework for investors to think about the long-term future of the industry that we believe brings a useful light on today's landscape.

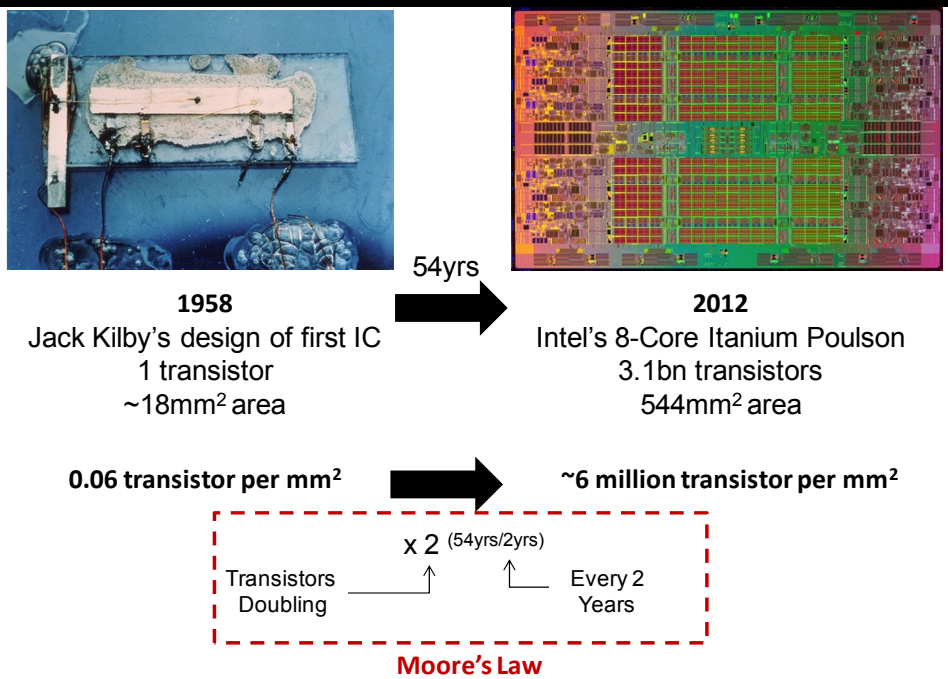
In this chapter, we establish a lay of the land: Where do we stand on semiconductor innovation? When and how shall we think about mourning Moore's Law? What are the industry-wide implications?

Moore's Law — the Driver for the Semiconductor Industry

Moore's Law Is the Single Most Important Driver of Growth, Profitability and Value-Creation in the Semiconductor Industry (and Beyond)

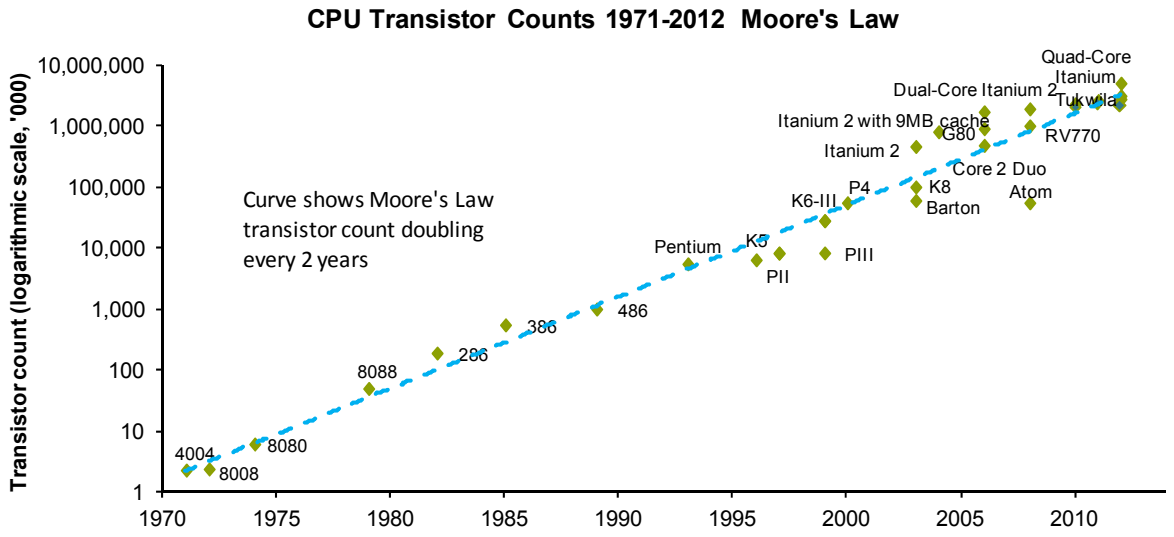
Moore's Law drives performance enhancement, which in turn drives replacement dynamics. It also drives cost efficiencies, which in turn drive elasticity-driven growth and, last but not least, technological challenges, which drive defensible competitive advantages and rights to make money across the value chain. A semiconductor industry without Moore's Law would look pretty dull (see Exhibit 12 and Exhibit 13).

Exhibit 12 Over the Last 50+ Years, Transistor Count Has Doubled Every Two Years



Source: Intel, Wikimedia Commons and Bernstein estimates and analysis.

Exhibit 13 **Moore's Law Held True Throughout This Period, as Transistor Count Inside a CPU Continued to Double Roughly Every Two Years**

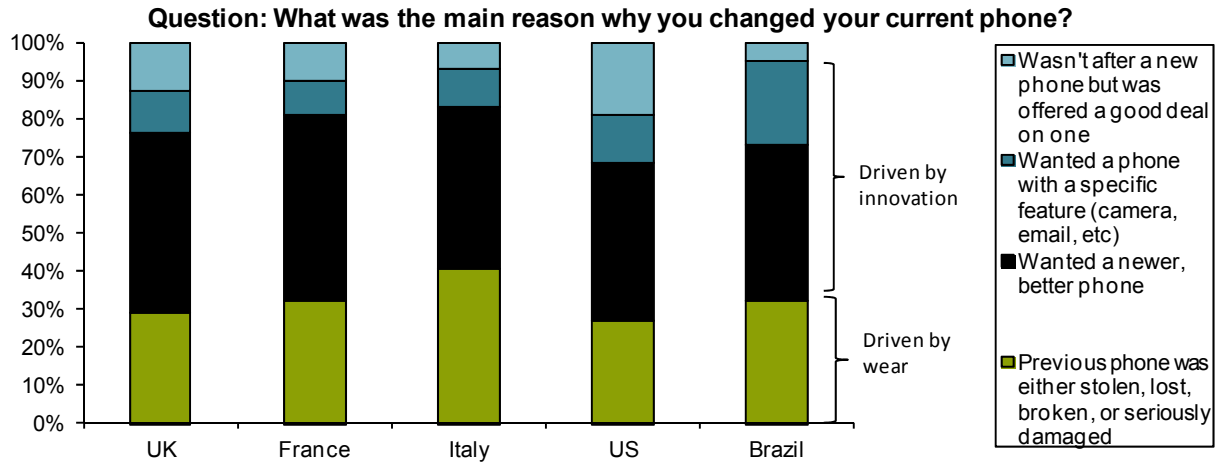


Source: Intel and Bernstein analysis.

Moore's Law Drives Performance Enhancement, Which in Turn Drives Replacement Dynamics

Moore's Law is about doubling the performance of semiconductor components every two years. Without this improvement, we believe replacement rate in these equipments would be significantly lower. As an illustration, a survey we carried out in the past showed only 32% of mobile phone replacement was driven by wear and tear, which leaves a fairly heavy weight for innovation as a replacement driver (see Exhibit 14). The same applies to personal computers, operating systems and other software products, network equipments and services, etc. Without Moore's Law, all these products wouldn't be refreshed much and the semiconductor industry, as well as the wider tech space, would be structurally an order of magnitude smaller in sales and profits.

Exhibit 14 **Better Performance, Enabled by Ever Increasing Transistors, Is the Main Driver for Replacement in Handsets, and Most Other Technology Products**



Source: Bernstein proprietary survey, spring 2008 (N = 2500; 500 per country).

Moore's Law Drives Cost Efficiencies, Which in Turn Drives Elasticity-Driven Growth

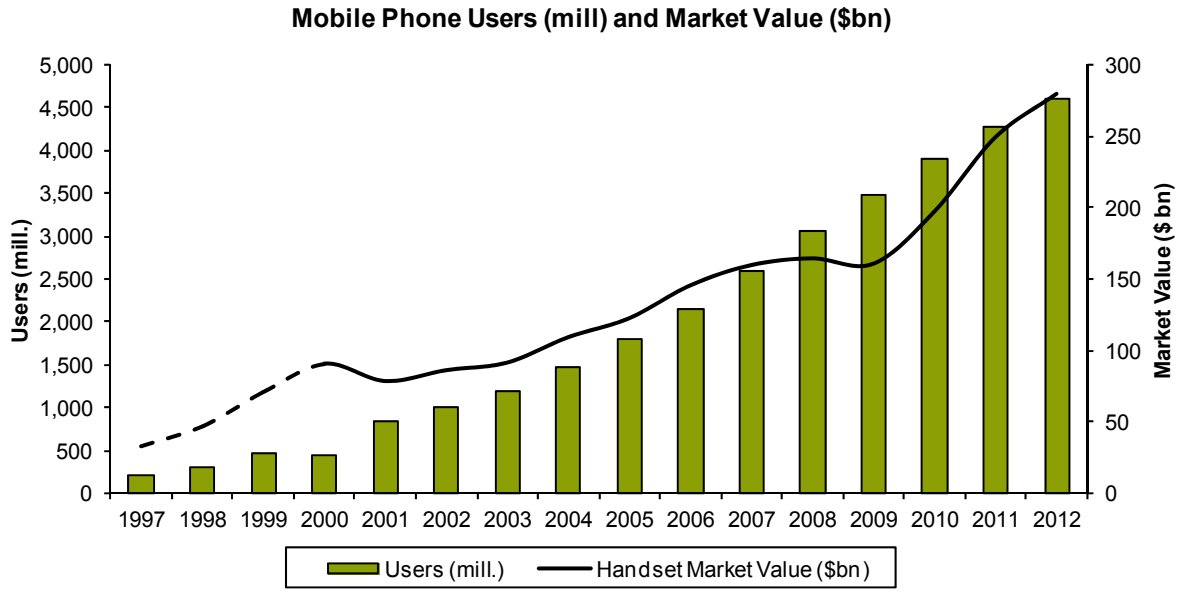
Another way to formulate Moore's Law is that the cost per transistor of semiconductor equipment comes down by 50% every two years[1] on the leading edge. This is by far the major driver behind the reduction of entry prices of most popular consumer electronics. Entry-level phones have reached $10 today versus ~$250 15 years ago, or a ~20% decline per year, which drove a 22-fold increase in the mobile phone user base (23% CAGR) and nine-fold expansion of the mobile phone market in value (15% CAGR) over the same period of time (see Exhibit 15 and Exhibit 16). Without Moore's Law, the semiconductor industry and the wider tech space wouldn't have been such a growth market.

Exhibit 15 **As Cost per Transistor Fell, Prices for Entry-Level Mobile Phones and PCs Have Declined Up to 20% p.a. Over the Last 15 Years**

	1997	2012	CAGR
Entry Level Mobile Phone	$248	$10	-19%
Entry Level PC	$1,000	$200	-10%

Source: Best Buy, mobilephonehistory.com, cnet.com and Bernstein analysis.

Exhibit 16 **With Falling Unit Prices, the Number of Mobile Phone Users as Well as the Market Value Have Expanded Significantly Over These Years**



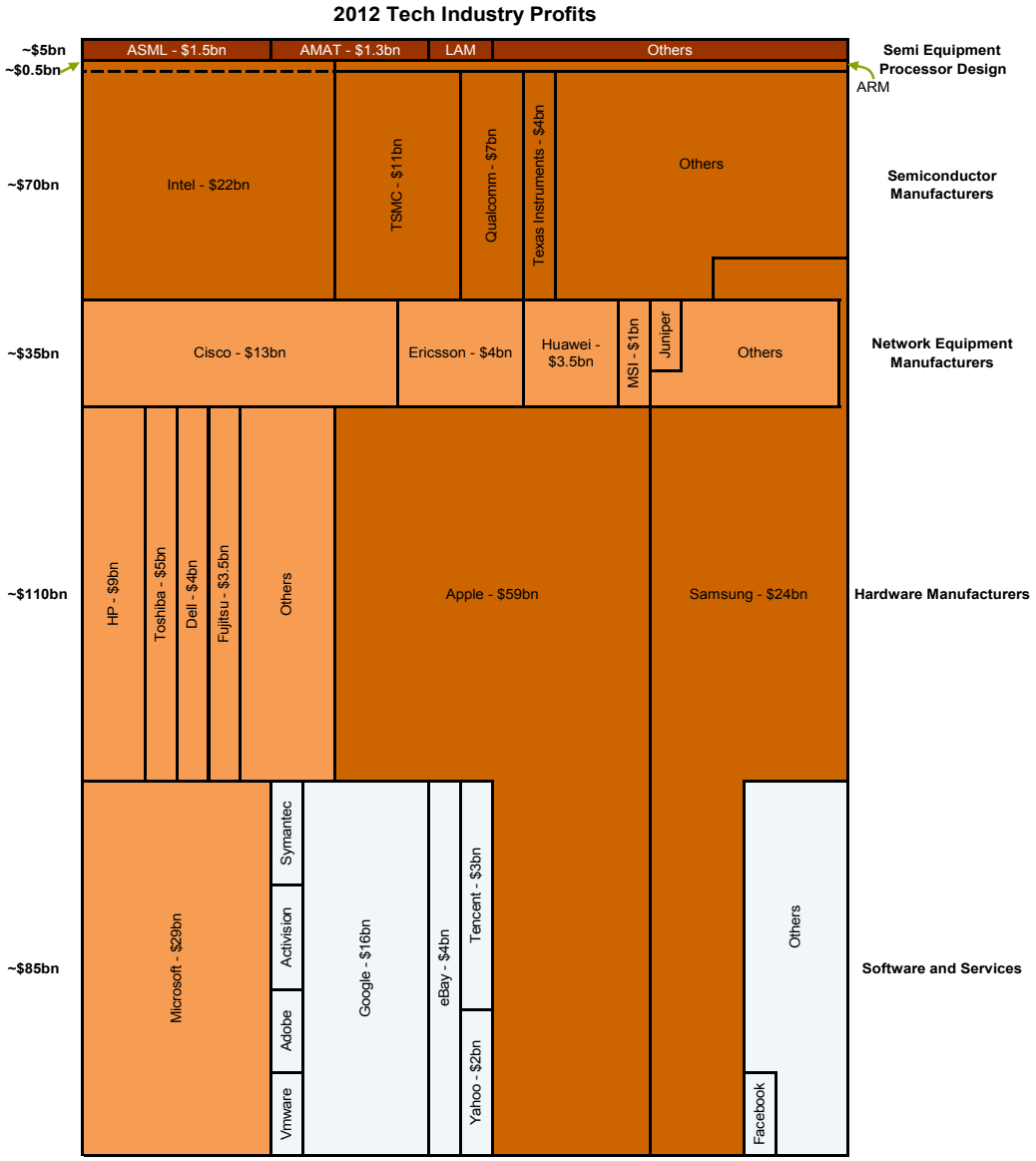
Source: Strategy Analytics and Bernstein estimates and analysis.

[1] This dimension of Moore's Law is actually coming under significant pressure. Refer to our Silicon Wars work for a comprehensive review of the growing challenges of delivering the economic side of Moore's law: **The Silicon Wars: Seismic Shifts in the Logic Semiconductor Value Chain**.

Moore's Law Drives Technological Challenges, Which Drives Defensible Competitive Advantages and the Right to Make Money Across the Value Chain

Cost efficiency and performance are well understood, but, to investors, they are the least important dimensions of Moore's Law. The foremost characteristic of the law is the technological challenges it introduces. In semiconductor manufacturing, a large share of profits sit at Intel, the champion of Moore's law that maintained a continuous manufacturing leadership, and TSMC, the sole general-purpose foundry that maintained the scale required to implement Moore's Law in a cost-competitive way. In the wider technology value chain, we would push the argument further: Microsoft's fascinating right to make money derives from the complexity Moore's Law introduced in its products and the related backward compatibility constraints, combined with upgrade cycles that Moore's Law generates! Similarly, what would Apple's gross margins be without a new application processor every year, etc. (see Exhibit 17)?

Exhibit 17 Most Profits in the Semiconductor Extended Value Chain Depend on Moore's Law



Note: Dark colors mean high dependence on Moore's Law.

Source: Capital IQ and Bernstein estimates and analysis.

A semiconductor industry without Moore's Law would look pretty dull. Our ambition for (Exhibit 18) was to represent what the Global Tech value chain would look like without Moore's Law. It's actually difficult to figure out what would survive. We are not even sure sell-side tech analysts would exist anymore.

Exhibit 18 What Would the Global Tech Value Chain Look Like Without Moore's Law?

Source: Bernstein analysis.

Moore's Law Has a Clear Absolute Physical Hard Stop

The Most Absolute Physical Hard Stop to Moore's Law Is at 0.00243nm

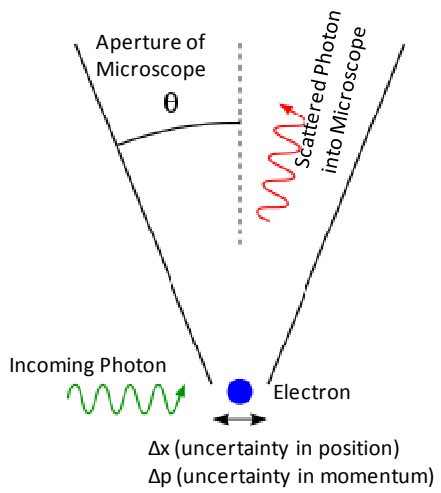
The most absolute limit to Moore's Law we can find is driven by the speed of light and the atomic and quantum nature of matter. It sets the bar far ahead: a couple of thousandth of a nanometer transistor and not before the 2060s.

The reasoning, adapted from a piece of research of James R. Powell, is the following: An electron's spin is the smallest way to materialize a bit (atomic nature of matter). Heisenberg's uncertainty principle tells us the fundamental limit to measure the position of an electron is the Compton wavelength of the particle, defined from the Planck constant and the speed of light (quantum nature of matter, speed of light) (see Exhibit 19 and Exhibit 20).

This wavelength is 0.0025 nm, which means that in pure theory, a device able to read the spin of an electron could be as small as this. Applying Moore's Law to this final dimension, we find the year to mourn Moore's Law should be between 2066 and 2094 (see Exhibit 21).

This limit is very theoretical. We have absolutely no clue (and we found absolutely nobody on Earth with a clue) of the type of device that could achieve this "electron read" with such a small feature size. The manufacturing of such a device appears rather challenging: an atom of silicon, as a very practical reference point, is still about 0.2 nm wide, or 100x larger than our minimum feature size (see Exhibit 22).

Exhibit 19 **Heisenberg's Uncertainty Principle Puts a Fundamental Limit on Measuring the Position and Momentum of an Electron**



Heisenberg's Uncertainty Principle

$$\Delta x \,.\, \Delta p \geq h$$

No matter what photon wavelength or aperture is used, the product of the uncertainty in measured position and measured momentum is greater than or equal to Planck's constant

Source: Bernstein analysis.

Exhibit 20 **From Heisenberg's Principle, It Follows That the Fundamental Limit to Measuring the Position of an Electron Is Its Compton Wavelength**

Heisenberg's Uncertainty Principle $\Delta x \,.\, \Delta p \geq h$

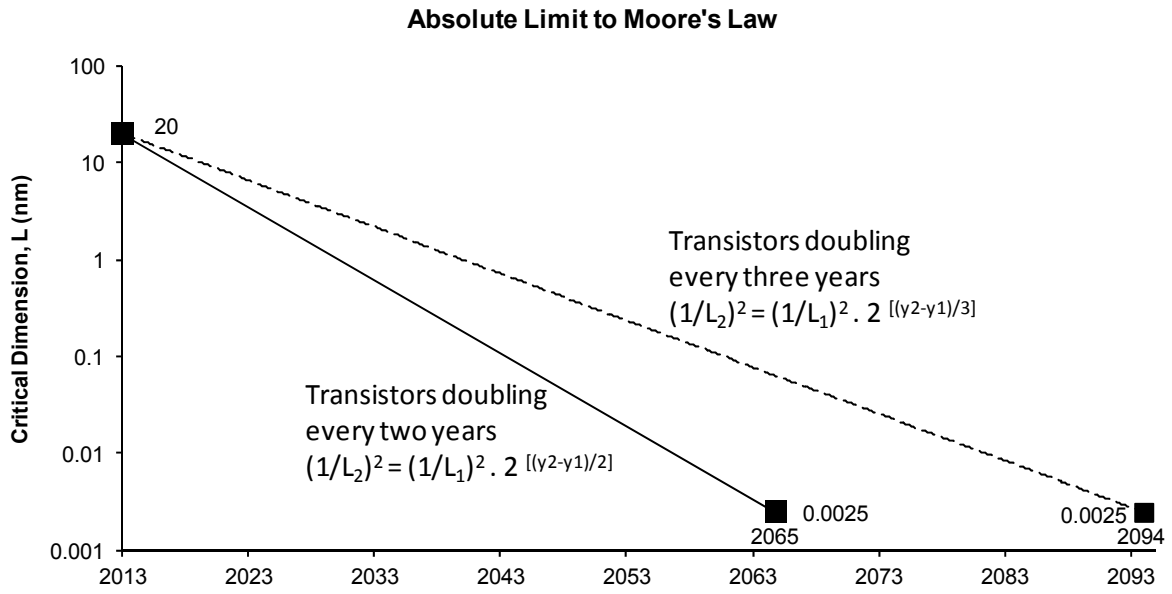
Momentum $p = m \,.\, v$

Fundamental Limit to Δx $\Delta x \geq \frac{h}{mc}$

Then the fundamental limit to measuring an electron's position based on quantum mechanics and relativity is its Compton wavelength (h/mc), which is **0.00243nm**.

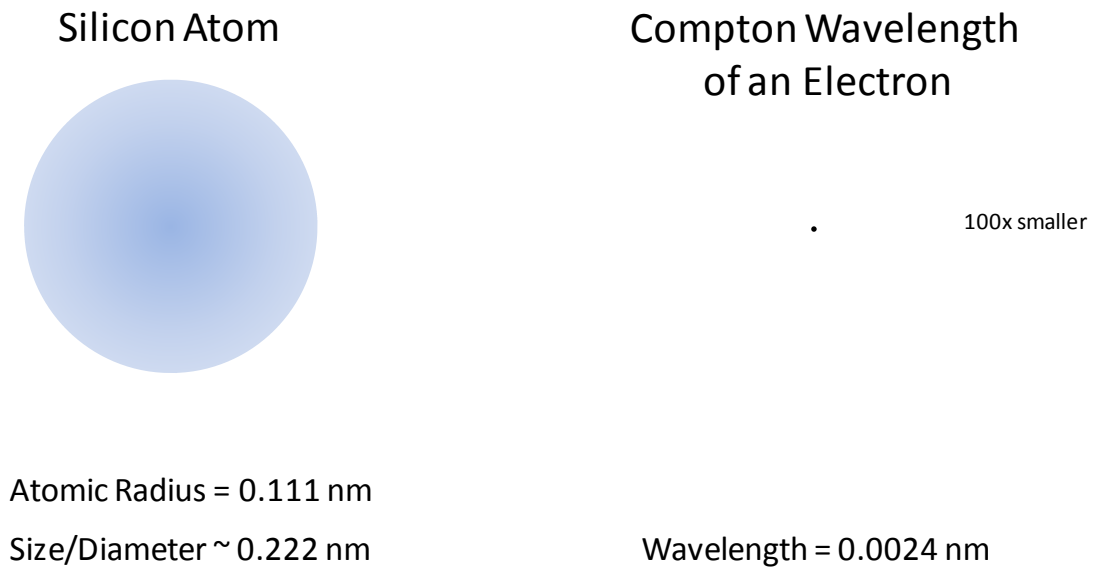
Source: Bernstein analysis.

Exhibit 21 **If the Critical Dimension Reaches This Compton Wavelength of an Electron, the Year to Mourn Moore's Law Would Be Between 2066 and 2094**



Source: Bernstein analysis.

Exhibit 22 **To Share an Idea of How Much of a Challenge This Dimension Represents, We Compare It to a Silicon Atom — the Compton Wavelength Is 100x Smaller**



Source: Bernstein analysis.

From a Thermodynamic Perspective, We Find an Earlier Hard Stop: the Minimum Energy Required to Change Transistor State

This raises the limit to a couple of nanometers and somewhere in the late 2020s.

The power required to switch a transistor from one state to another one has a thermodynamic limit. Based on the Shannon-von Neumann-Landauer expression, 0.017 eV is required as a minimum energy to change the state of a bit at room temperature, whatever its physical implementation (see Exhibit 23).

A switching power limit introduces a dimensioning limit. Linking this back to Heisenberg's uncertainty principle, we can conclude the minimum feature size of a transistor has to be above 1.5nm. This materially reduces the time horizon of Moore's Law, to somewhere around 2030 (see Exhibit 24).

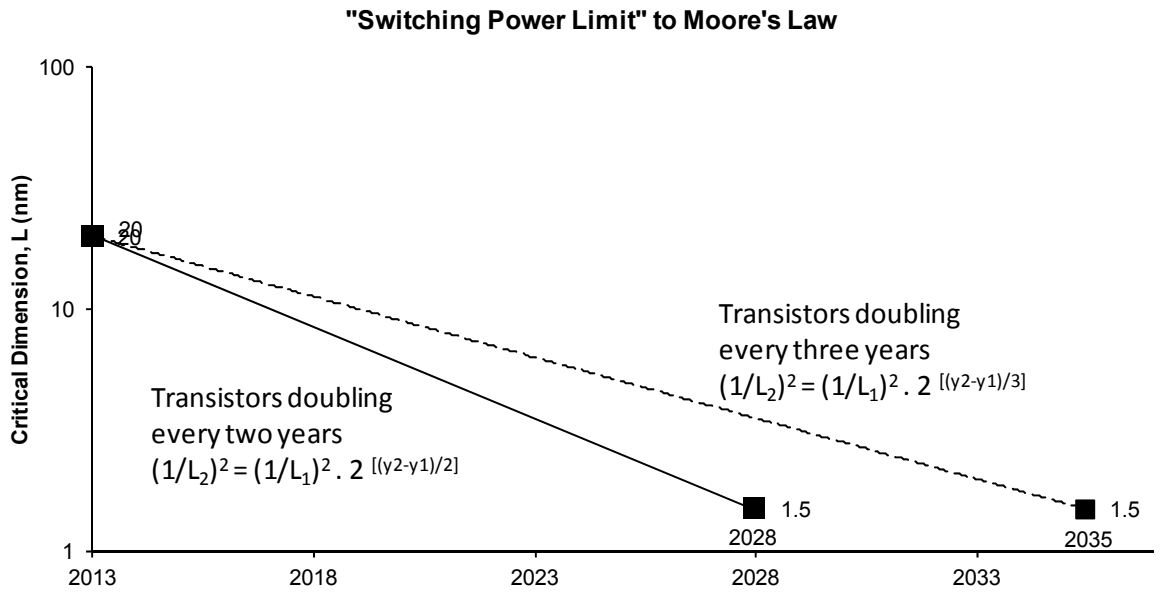
Lowering temperature doesn't work as a way to lower that limit. While reducing temperature of the transistor helps improve E_{bit}, more energy is needed to remove heat from the circuit (see Exhibit 25). This increases the power density of the transistor well beyond possible limits. Simulation work shows a sub-1nm feature size would approach a power density of 10,000,000,000 W/cm^2 versus the surface of the Sun being 6,000 W/cm^2.

Exhibit 23 **Based on the SNL Expression, We Can Derive the Minimum Energy Needed to Switch a Bit Between On/Off to Be 0.017eV**

		For a Bit
Boltzmann's Equation	**$\Delta S = k_B * \ln(W)$** ΔS is the change in entropy K is the Boltzmann constant in J/K/particle W is the number of microstates possible	1.38×10^{-23} m^2 kg s^{-2} 2 (on/off)
+		
Second Law of Thermodynamics	**$\Delta S = \Delta Q / T$** ΔQ is the change in Energy T is the Temperature (°K)	300°K (Room temp)
=		
Shannon-von Neumann-Landauer (SNL) Expression	**$E_{bit} = k_B T \ln(2)$**	**= 0.017eV** to process a bit at room temperature

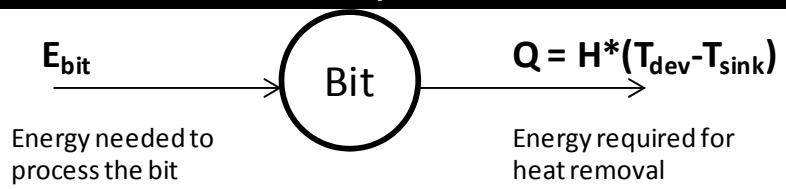
Source: Stanford University (Suhas Kumar) and Bernstein analysis.

Exhibit 24 **Linking This Back to Heisenberg's Uncertainty Principle, the Minimum Feature Size Would Need to Be >1.5nm, i.e., the Industry Reaches the Last Critical Dimension Somewhere Around 2030**



Source: Bernstein analysis.

Exhibit 25 **At Less Than 1nm Levels, We Hit Major Thermal Barriers, Leading to Impractical Levels of Power Density on the Surface**



Below 1nm

- Total Energy required driving power density too high
- Cooling the chip doesn't help reduce feature size

Source: Stanford University (Suhas Kumar) and Bernstein analysis.

Many Roadblocks Nevertheless Stand Ahead of Us on the Path to 1.5nm

Practical limitations are starting to play a role already today, and it is just the beginning. The most immediate ones are related to direct-tunneling leakage (the quantum property of electrons to go through matter inadvertently), Lithography, and other manufacturing roadblocks.

The Leakage Roadblocks

The source and drain of a transistor are separated by a channel, which is the corridor through which current can flow in the on-state, and which is regulated by a "gate." The material properties and doping of the channel determine a "band gap," or the energy gap separating the valance band in a material (the energy level in which electrons are not free to move) from the conduction band (a higher energy level that, once electrons are energized at, allows them to flow through a material). Applying a voltage to the transistor gate "bends" these bands; when enough voltage is applied (the threshold voltage) electrons can make the jump, carriers populate the channel, and current can flow between the source and the drain. Below the threshold voltage, the band gap (at least classically) prevents substantial current leakage in the "off" state of a transistor (though leakage is becoming a much bigger issue, from this and other sources, as transistors continue to scale ever smaller.

Leakage is a function of the dimensions of the gap, and the transistor structure and material properties. Down to a certain feature size, leakage is predominantly thermal assisted, i.e., can be controlled, but as the size of the gap shrinks, direct tunneling becomes a primary leakage driver and cannot be controlled anymore (see Exhibit 26).

The design of transistors is being evolved to limit leakage. We nevertheless see a hard stop for today's Silicon-based FinFET/Tri-Gate designs at 5 nm node at the latest, a dimension that we expect the industry will have fully ramped somewhere in the 2020s (see Exhibit 27).

At 5nm or even maybe before, alternatives to Silicon and new designs will need to be introduced. The primary driver for these alternatives is to increase carrier mobility in the channel, reduce leakage currents, and minimize short channel effects; all of which are interlinked and start to surface already at sub-22nm feature size. For example, a high band gap will enable low leakage, but will provide low drive current (carrier mobility).

In today's transistors, as channel length is scaled down, strain is induced in silicon to increase drive current, but this approach used today will soon hit limits on carrier mobility. New materials (that have inherently better transport

characteristics) and new transistor designs are required to enable scaling in the sub-10nm domain:

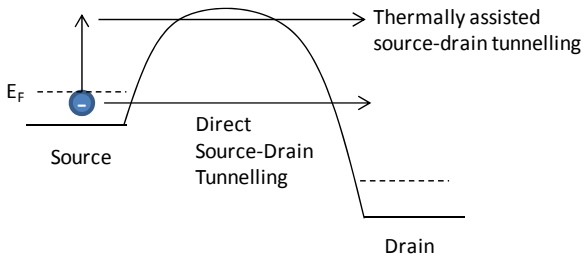
Ge-based or III-V materials. The industry is expected to move to next-generation high-mobility FinFET at 7nm. One option is a FinFET with Ge for both the p and n channels, and another option is Ge for the p channel and indium gallium arsenide (InGaAs) for the n channel. Intel is working on the latter design for its FinFET transistors that could come in by 2020 (see Exhibit 28).

Carbon-based field effect transistors (FET). Materials such as carbon nanotubes have much higher intrinsic transport properties, such as electron mobility and thermal conductivity and will allow continued channel length scaling beyond what silicon permits (see Exhibit 29). Graphene, made up of a hexagonal structure of carbon atoms one-atom thick, also exhibits very high carrier mobility. Moreover, the "band gap" of Graphene can be tuned and is very low compared to Silicon. Issues in transferring Graphene sheets onto a target substrate while retaining high mobility remain a challenge, but IBM researchers have created first grapheme-based ICs that can withstand temperatures up to 127°C and operate at frequencies as high as 10Ghz.

New Transistor Designs. Several new transistor design options are also being explored to overcome limits of current silicon transistors.

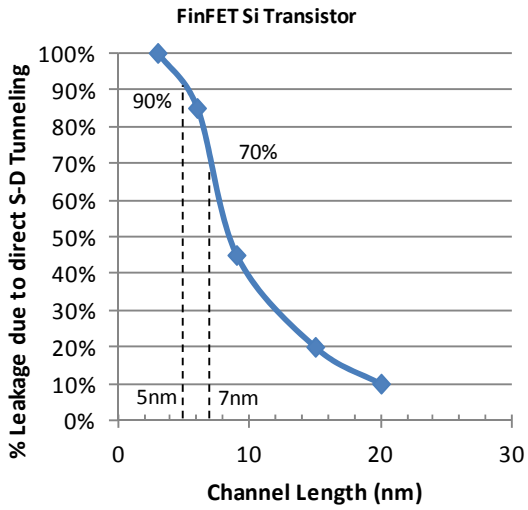
- **Junctionless transistors**. These transistors use a control gate around a silicon nanowire that can tighten around the wire (through electrostatic pinch-off) to the point of closing down the flow of electrons without using junctions or doping (see Exhibit 30). These designs should be particularly applicable in manufacturing of transistors below 10nm and display a host of benefits: extremely low leakage currents, less degradation of mobility with voltage and temperatures, and near-ideal sub-threshold slope.
- **Spin field-effect transistor (FET).** A spin transistor utilizes the natural ability of the electrons to show two states: "spin up" and "spin down." A primary advantage of these transistors over regular ones is that these spin states can be detected and altered without necessarily passing electric current. As such, these designs consume less power, are faster and are more easily scaled.
- **Tunnel FET**. Leakage current increases exponentially as transistors are scaled as electrons go over the "band gap" (short channel effect). Tunnel FET overcome this limit by allowing electrons to go through this energy barrier through band-to-band tunneling, which is then controlled by a gate. Presently, the drive current obtained from this approach is limited and the industry would need new materials to allow more efficient tunneling (see Exhibit 31).
- Exhibit 32 presents a summary of advantages and limitations of these emerging technologies.

Exhibit 26 **Direct Source-Drain Tunneling Effects Put a Limit of 5nm to 10nm on Moore's Law**



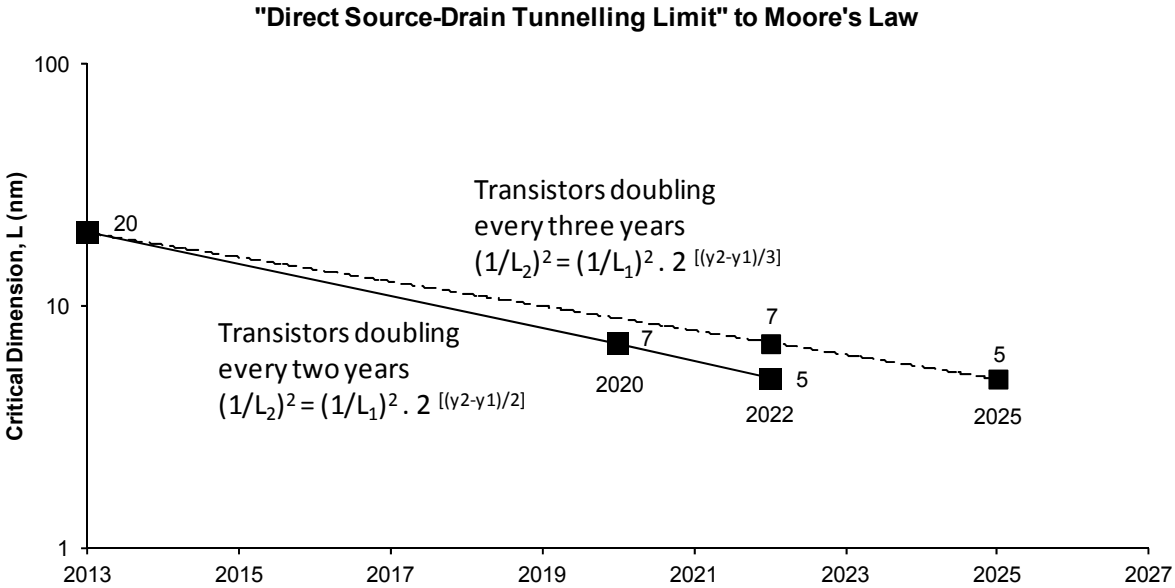
$$T \;\alpha\; \exp\left[-2\,(2m^*/\hbar^2)^{1/2}\,(q\Phi)^{1/2}\,d \right]$$

T = transmission probability over barrier
M* = Effective mass of Silicon
Φ = Barrier Height
D = Barrier Width



Source: Monolithic3D, Lundstrom et al and IEDM 2002.

Exhibit 27 **Direct Source-Drain Tunneling Sets the Limit to Moore's Law at 5nm or Sometime in the 2020s, With Silicon FinFET**



Source: Bernstein estimates and analysis.

Exhibit 28 New Channel Materials That Can Enable Higher Electron Mobility Are Among the Ways to Enable Scaling in the Sub-10nm Domain

Material -> Property	Si	Ge	GaAs	InAs	InSb
Electron Mobility	1600	3900	9200	40000	77000
Hole Mobility	430	1900	400	500	850
BandGap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric Constant	11.8	16	12.4	14.8	17.7

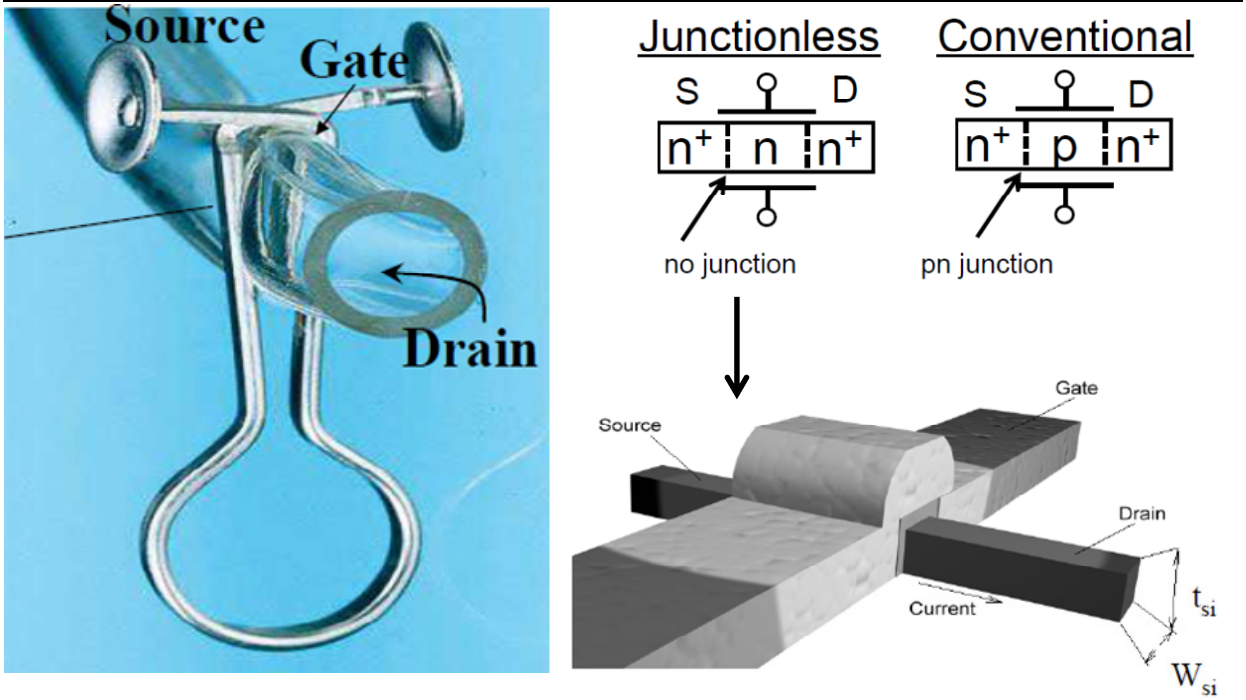
Source: Intel and Bernstein analysis.

Exhibit 29 Carbon Nanotubes Have Excellent Intrinsic Transport Properties

	Si	Single Wall Carbon Nano Tube
Mobility (cm2/V/s)	1400	>10000
Mean Free Path (nm) @ room temp	30	>1000
Thermal conductivity (W/mK)	150	5800

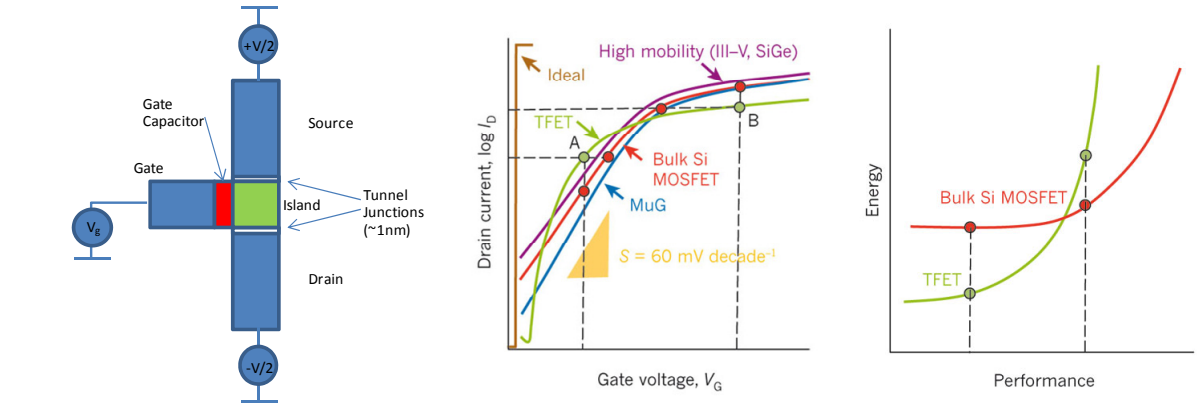
Source: K Banerjee (UC Santa Barbara).

Exhibit 30 Junctionless Transistors Use a Control Gate Around a Silicon Nanowire That Can Tighten Around the Wire to Close the Passage of Electrons, Without the Use of Junctions or Doping



Source: Jean-Pierre Colinge (Tyndall National Institute).

Exhibit 31 **Tunnel FETs Use Band-to-Band Tunneling as the Transport Mechanism, Are Closer to an Ideal Transistor Operation and Are More Power Efficient Designs vs. Bulk Si MOSFET Designs**



The energy to jump the junction must equal the **coulomb energy** ($e^2/2Cg$). Voltage needed to transfer an electron is e/C. Thermal energy k_BT must be below the charging energy for no thermal transfer. Since the Gate is thicker, not tunneling occurs through it.

Tunnel transistors are closer to an ideal design for a transistor

These transistors consume less energy for the same performance at moderate performance levels

Source: Nature and Bernstein analysis.

Exhibit 32 **Summary of Advantages and Challenges of Emerging Technologies**

	Advantage	Issues
Junctionless FET	CMOS process compatibility	Worse gate control in short-channel
Spin FET	Low Power, Suitable for Memory (non-volatile info storage)	Low efficiency of spin injection
Tunnel FET	Lower V_{dd}; Lower I_{off}	Lower I_{on}
Carbon Nanotubes	Higher transport velocity	Low density and alignment, reproducibility, integration
Graphene FET	RF application	Huge I_{off}

Source: Frontier Research Center (TIT).

The Lithography Roadblocks

Lithography tools define the feature size of an integrated circuit and their limitations introduce significant roadblocks as well. We see three successive "Lithography barriers."

The first Lithography barrier: ArFi and 38 nm. The wavelength of the light used by today's leading-edge tools (ArF), of 193nm, limits single pattern critical dimensions to 38nm. This sub-wavelength Lithography has been already in itself a technological prowess, leveraging mask making and optics technology improvements and immersion lens technology (see Exhibit 33 and Exhibit 34). This roadblock was already reached in 2010, when the industry started ramping up the 32nm node, but overcome with the introduction of multiple patterning.

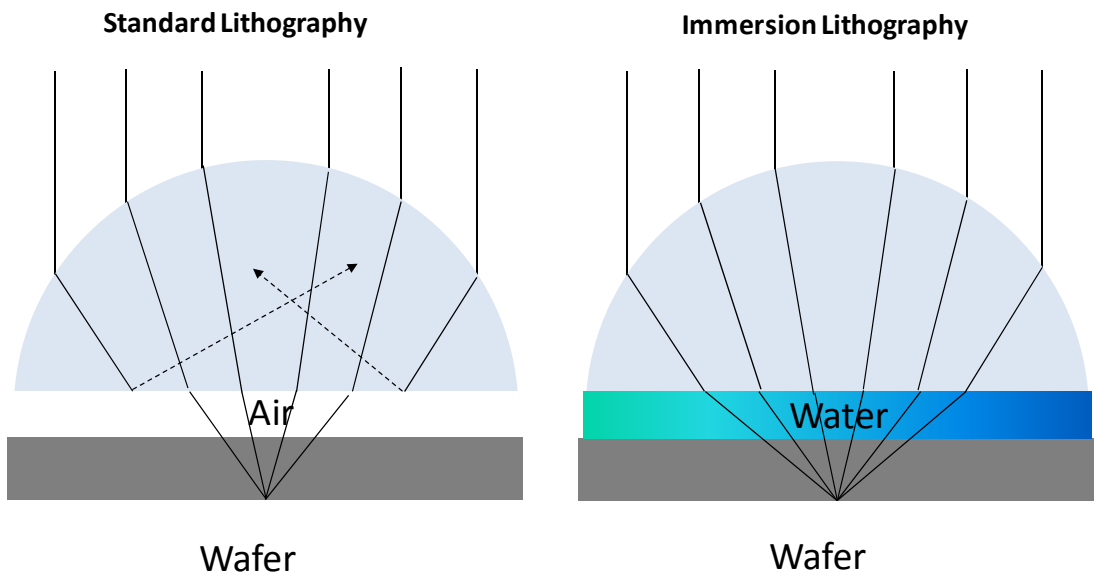
The second Lithography barrier: ArFi Multiple patterning and 10nm. With several successive exposures, ArFi tools can generate patterns with critical dimensions down to 10 nm, at the cost of steep increase in Lithography costs and important design limitations. The industry seems confident about the ability of ArFi

multiple patterning to push back critical dimensions to 10nm (see Exhibit 35), fuelling Moore's Law to the back end of this decade (we expect the 10nm node to start in 2016-17 and peak in capacity by 2020). We also believe the 7nm node might be achievable with ArFi multiple patterning as well. Beyond that point, a new technology using shorter-wavelength light is required.

The third Lithography barrier: EUV and…a minimum critical dimension still to be defined. Lithography tools using EUV (Extreme Ultra Violet) light with a shorter wavelength (13.5nm) is the technology coming after ArFi multiple patterning. We expect the technology to make its debut in production in 2014 and to ramp up capabilities progressively, as ArFi limits are reached. The industry already has a roadmap down to below 7nm for Lithography (see Exhibit 36) and we estimate that with 13.5nm EUV light, the technology can get to a 4nm critical dimension, if EUV tools reach the level of optical quality of current ArF tools (see Exhibit 37). EUV optics being far more challenging to manufacture, such a resolution might never be achieved with single patterning and a 13.5nm light source.

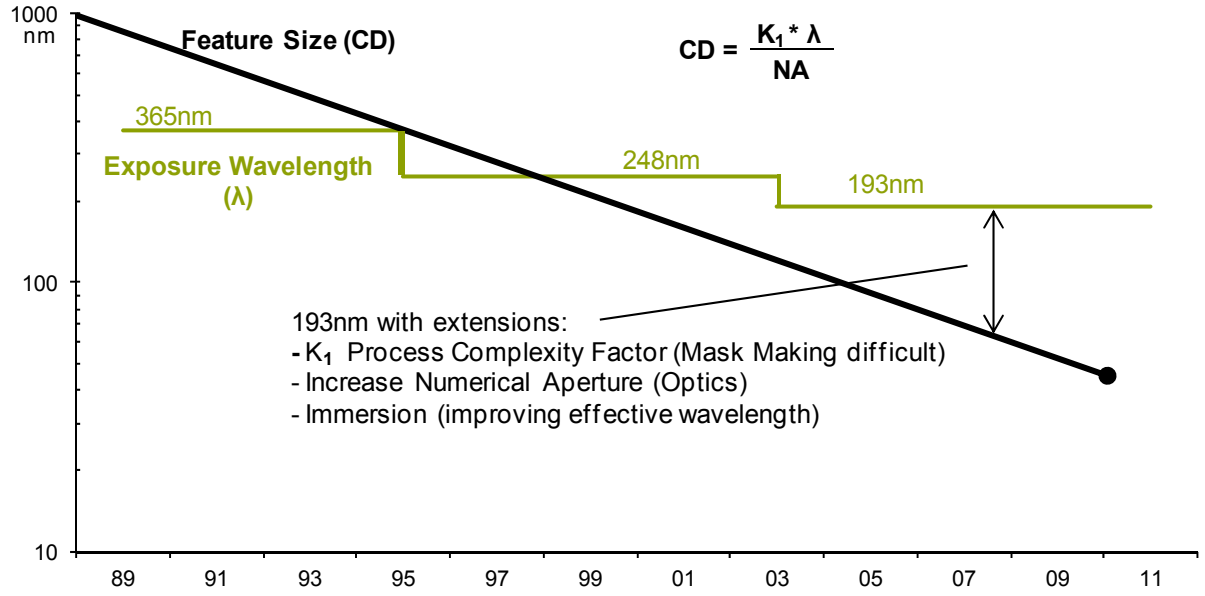
Beyond that point, new light sources with even shorter wavelength and EUV multiple patterning will likely take the resolution of Lithography a step further, closer to our ultimate "sub 2nm" hard stop. At this stage, there isn't much visibility on how far Lithography can take the industry. On a side note, electron beam Lithography could also emerge at some point as a successor to EUV Lithography, but again, visibility is very limited.

Exhibit 33 Immersion Technology Allows Improvement in Numerical Aperture



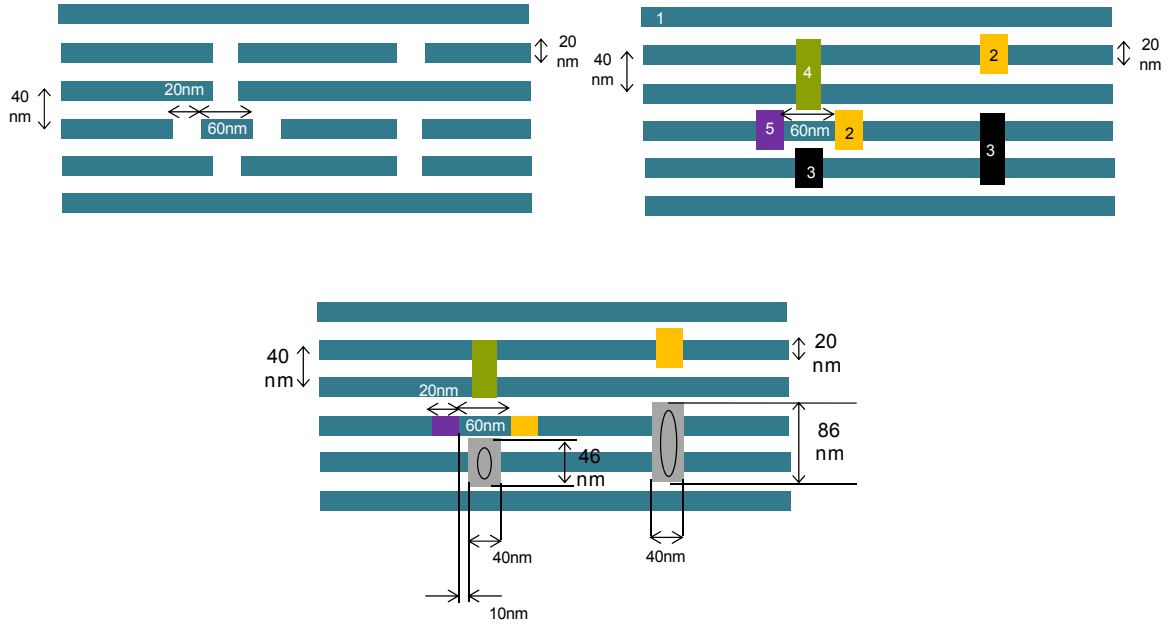
Source: ASML and Bernstein analysis.

Exhibit 34 **Technological Advancements in Mask-Making, Optics, and Use of Immersion Technology Have Allowed Using 193nm Light Up to 38nm Using Single Patterning**



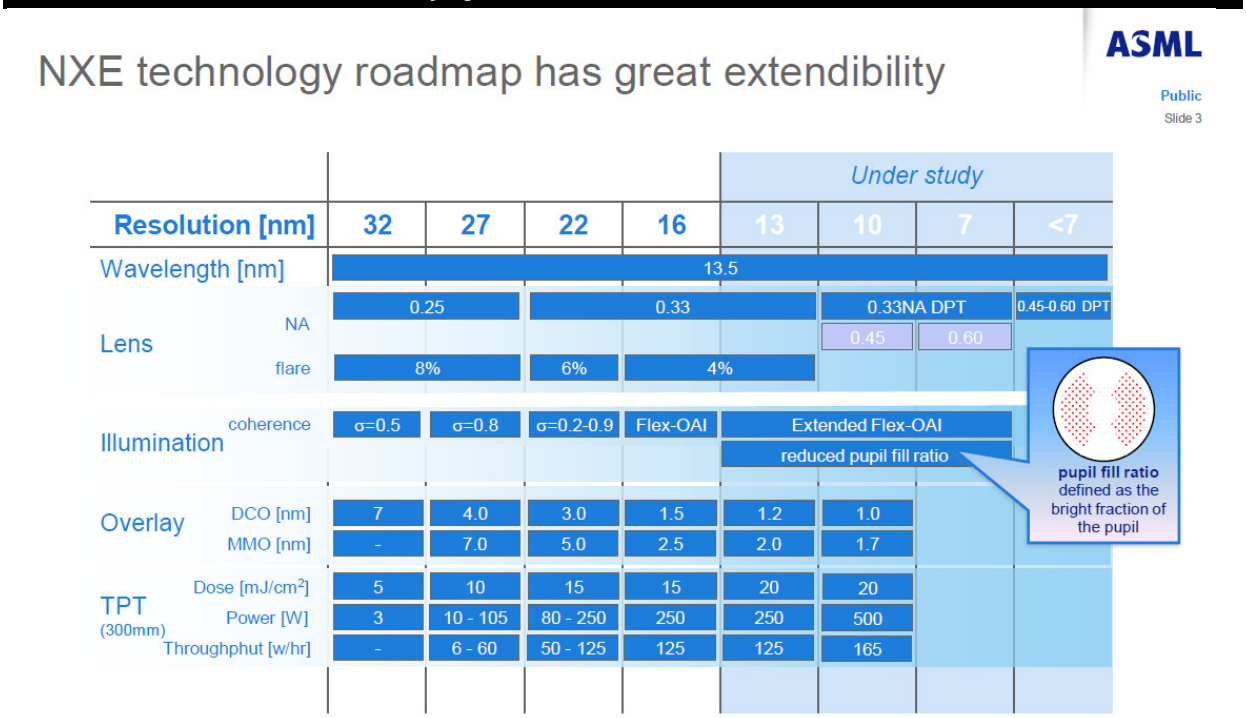
Source: Intel and Bernstein analysis.

Exhibit 35 **Below 38nm, Multiple Patterning Is Required With ArFi; Intel Already Has Plans for Quintuple Patterning for 10nm**



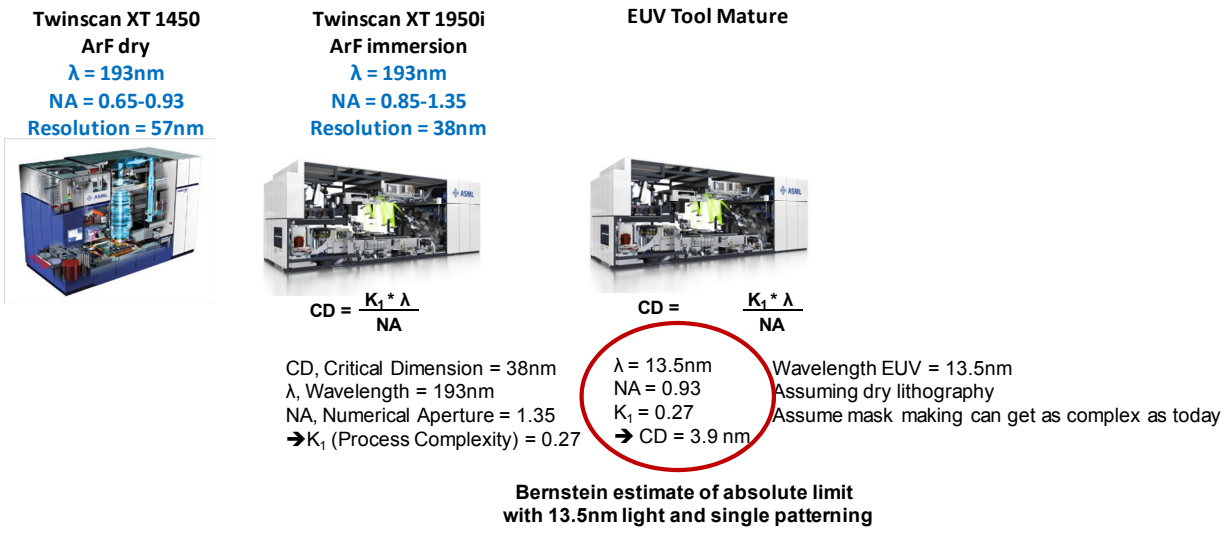
Source: Intel and Bernstein analysis.

Exhibit 36 **ASML Recently Shared Its Roadmap for EUV Technology at SPIE 2013; the Company Is Studying <7nm Resolution**



Source: ASML.

Exhibit 37 **Assuming Optics of EUV Tools Improve to Levels Similar to Dry ArF Tools, Resolution Could Come Down to 4nm**



Source: Bernstein estimates and analysis.

Other Roadblocks

Beyond leakage and Lithography, we see a long list of mounting difficulties for the industry to continue to deliver Moore's Law. Virtually no process step is exempt from challenges: Material challenges for interconnect layers will surface soon, similar to those described for transistor layers, the increase in power density poses material challenge as well, as do metrology, test, defect detection and measurement of smaller and 3D structures. If none of these barriers appear insurmountable, their

combination is clearly changing the economic side of Moore's Law and increasing the chances of roadmap slippage and slower node transitions (see Exhibit 38).

Exhibit 38 Beyond Leakage and Lithography, We See a Long List of Mounting Difficulties for the Industry to Continue to Deliver Moore's Law

Other Roadblocks	
Transistor Manufacturing	PD-SOI and FD-SOI; Multi-gate design; High-k gate dielectric materials
Interconnect	New materials (low-k); process complexity (etch, clean, fill), integration issues (CMP damage, resist poisoning, low-k degradation, thermomechanical effects); chip stacking; line-edge roughness
Metrology, Test, and Defect Detection	Non-destructive production worthy CD measurement techniques at low nm; cost of testing increasingly complex devices (30+x more transistors by 2023); systemic defect detection and reliability screening.
Power density	Issues with heat dissipation and power densities reaching unrealistic levels at lower nodes; hot-spot management

Source: ITRS and Bernstein analysis (U.S. and European Semi Teams).

We present here a detailed discussion of various transistor manufacturing challenges and the current state of solutions.

Silicon on Insulator (SOI). Conventional silicon (bulk CMOS) can suffer from parasitic capacitance that forms between the junction and the substrate. SOI-based devices introduce an insulator between the substrate and the silicon junction (see Exhibit 39). This isolation reduces parasitic capacitance effect and allows the circuit to operate with a reduced supply voltage, which improves power consumption at matched performance. This design also minimizes latchup (or short circuit) due to complete isolation of n- and p- structures and enables design of denser and more reliable circuits. However, all of this comes with manufacturing complexity and higher costs. The current roadmap for the industry is to move from partially depleted SOI (PD-SOI) to fully depleted SOI (FD-SOI) over the coming years. ST-Ericsson is already using FD-SOI at 28nm for its NovaThor L8580 chipsets. Another way to overcome the limitations of a bulk CMOS design is using 3D transistors. Intel uses bulk CMOS technology at 22nm, however, together with high-k metal gate and 3D transistors. For a bulk CMOS with planar transistors, however, the parasitic capacitance and latchup deteriorate performance significantly at the 32nm node, making it essential to use SOI at 20nm. IBM has suggested that SOI technology, used together with 3D transistors, could facilitate scaling to 5nm.

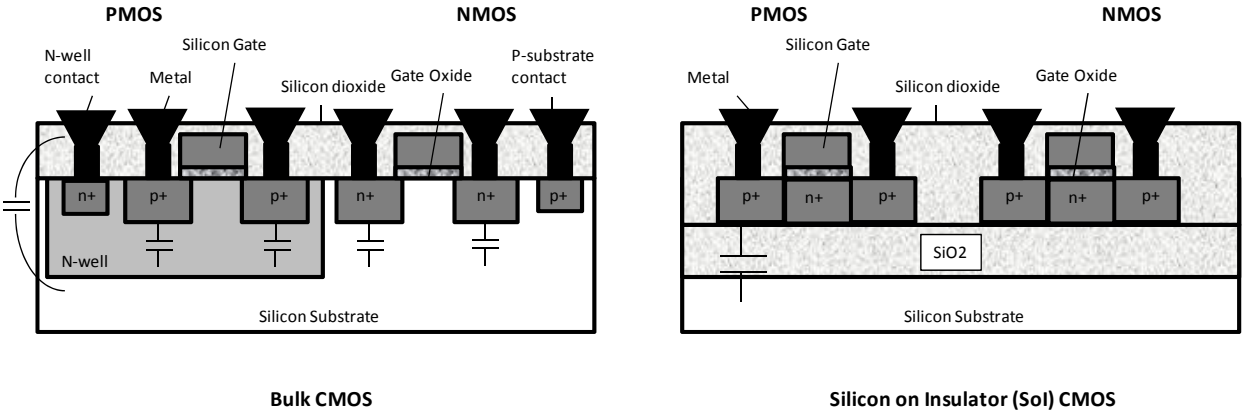
3D transistors. For Foundries, 20nm represents the last node with planar transistors, because the planar design begins to suffer from short-channel effects. As the channel length is scaled down, the channel region starts to get influenced by the source/drain as much as by the gate (see Exhibit 40). Thus, the threshold condition (for electrons to move) can be reached at a lower gate voltage as the drain creates a larger depletion region (see Exhibit 41). This slows down the variation of

current with gate voltage, resulting in higher off current (I_{off}). The consequence of a higher off current (I_{off}) is greater stand-by power consumption, limiting further shrink. This is measured by Drain Induced Barrier Lowering (DIBL) and a higher value is an indication of poor short-channel behavior. The 3D (or FinFET) transistor design utilizes a gate electrode that controls silicon from multiple sides (three for tri-gate) (see Exhibit 42), instead of one in a planar transistor design. This reduces the minimum channel length at which the short channel effects start to appear by a factor of two, allowing continued shrink (see Exhibit 43). Today's FinFET design would allow the industry to scale up to 10nm, beyond which the industry would need next-generation FinFETs, involving alternative channel materials to provide higher electron mobility, according to an executive at GlobalFoundries.

High-k metal gate. Gate dielectric thickness in transistors has shrunk over time, in order to provide better gate capacitance and improve drive current. However, as we scale down to gate dielectric thicknesses below 2nm, the leakage current increases due to tunneling, leading to higher power consumption and poor reliability. New materials with a higher dielectric constant are an alternative way to increase capacitance while keeping higher thickness (see Exhibit 44). In replacing silicon dioxide, materials that have received considerable attention are hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide, typically deposited using atomic layer deposition. The key consideration in choosing the material is high di-electric constant but also easily to manufacture. As a comparison, SiO2 has a dielectric constant of 3.9 versus Hafnium dioxide (HfO2) at ~25 and Hafnium Silicate (HfSiO) at ~15, suggesting that using these materials we can get 4-6x thicker gate dielectrics with the same capacitance.

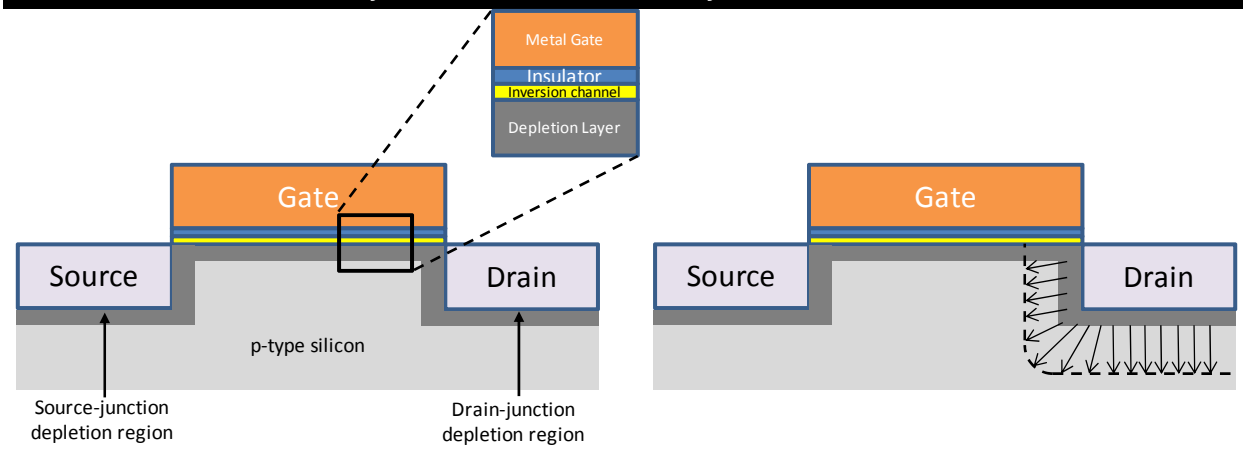
We summarize in Exhibit 45 these discussed effects, the limits to shrink they represent, as well as the solutions and the extension to shrink they can provide.

Exhibit 39 **A SOI Design Inserts an Insulator Between the Junction and the Substrate, Thereby Reducing Parasitic Capacitances Significantly**



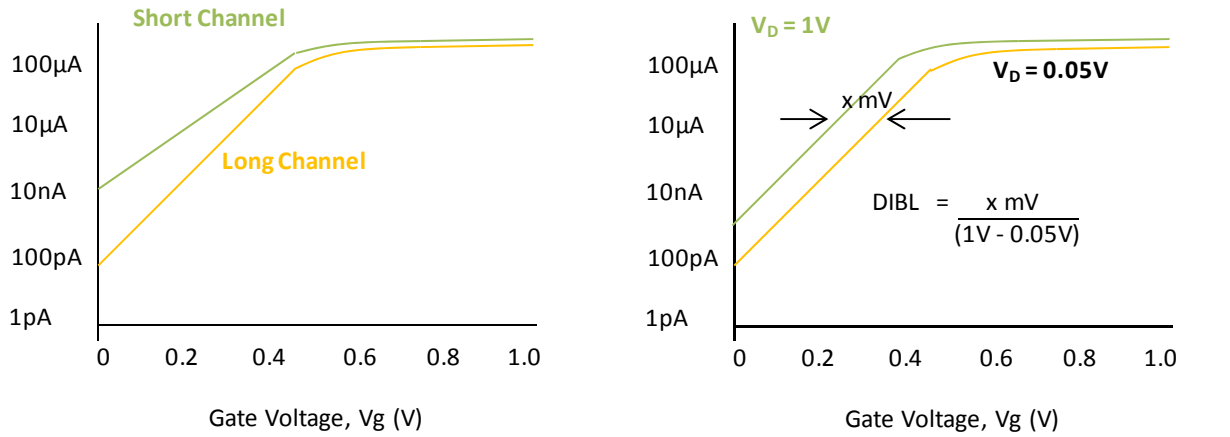
Source: Bernstein analysis.

Exhibit 40 **As the Channel Length Is Scaled Down, the Channel Region Starts to Get Influenced by the Source/Drain as Much as by the Gate**



Source: Bernstein analysis.

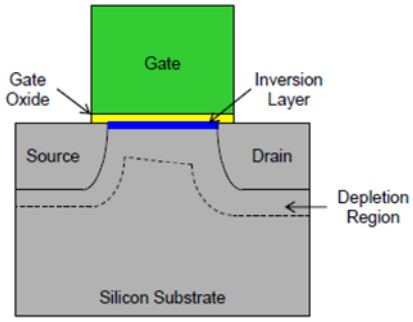
Exhibit 41 **Short Channel Effect Results in Higher Off Current, Which Increases Standby Power; DIBL Is Used to Characterize Short Channel Effect**



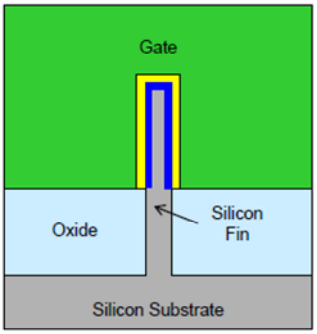
Source: *Nature* and Bernstein analysis.

Exhibit 42 **The 3D Structure Forms Conducting Channels on Three Sides of the Fin Structure, Providing "Fully Depleted" Operation or Reduced Leakage Current**

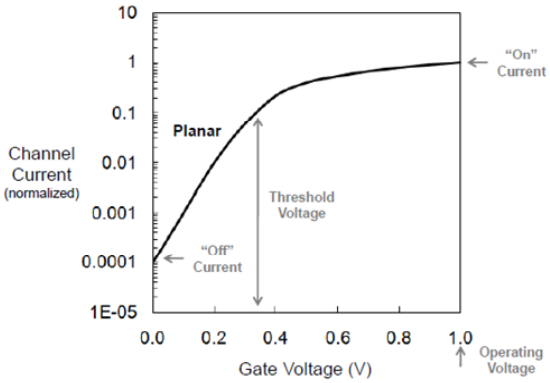
Silicon substrate voltage exerts some electrical influence on the inversion layer (where source drain current flows)



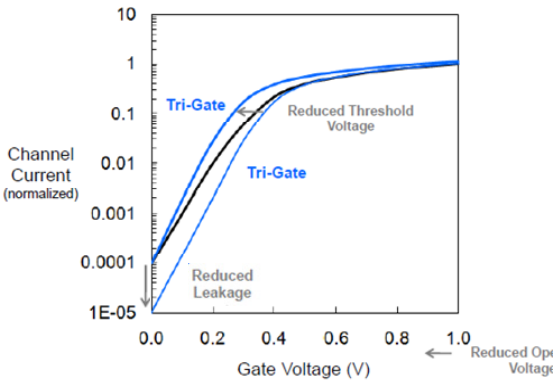
Gate electrode controls silicon fin from three sides, providing improved sub-threshold slope. Inversion layer area increased for higher drive current. Process cost added ~2-3%



The influence of substrate voltage degrades electrical sub-threshold slope (transistor turn off-characteristics)

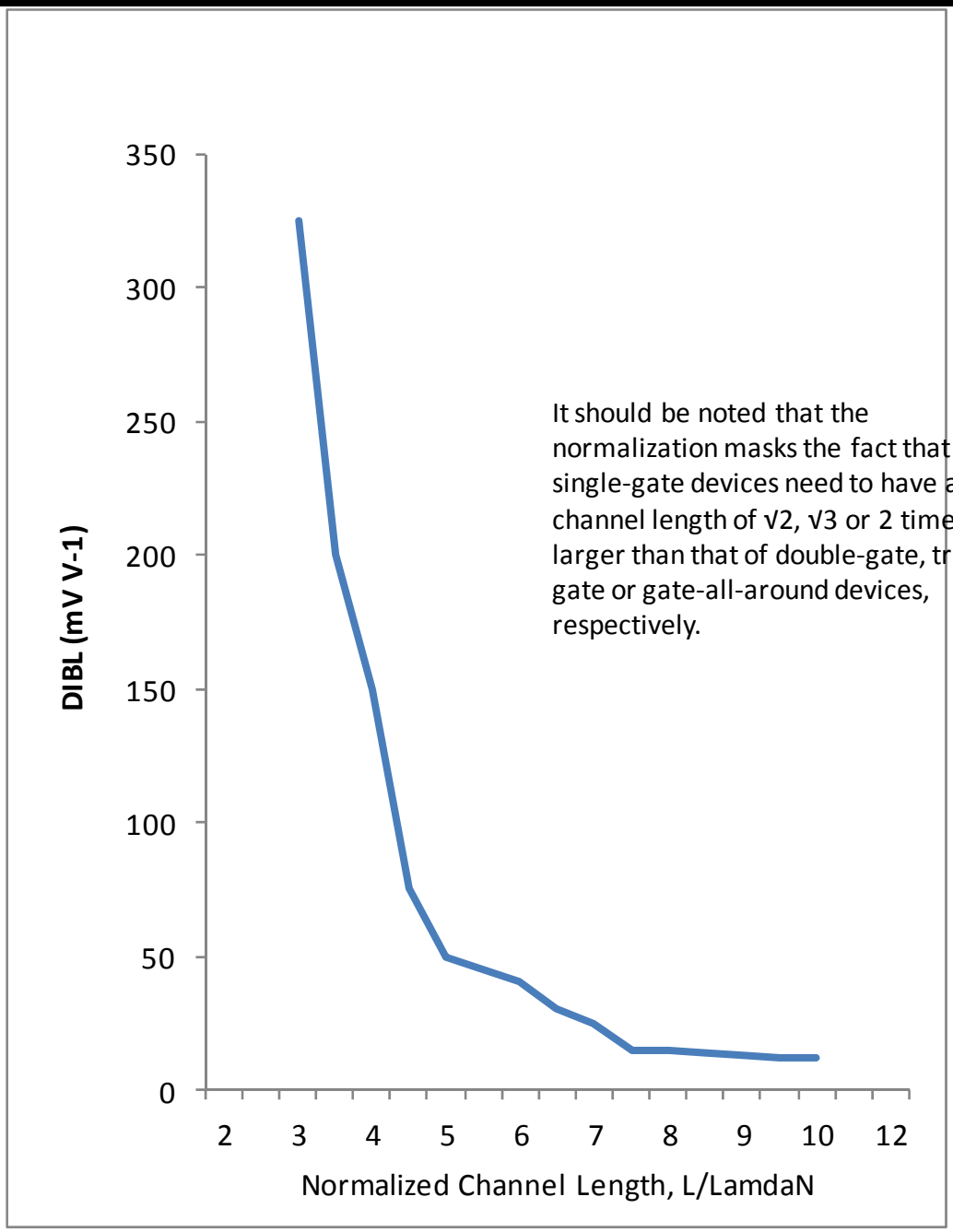


The "fully depleted" characteristics provide steeper sub-threshold slope that reduce leakage current (better power efficiency). The steep slope can also be used to operate at lower voltage to reduce power and/or improve switching speed.



Source: Intel and Bernstein analysis.

Exhibit 43 **Below the Normalized Channel Lengths of 6, Short Channel Effects Start Becoming Significant; Multi-Gate Transistor Designs, Such as Tri-Gate, Allow Up to Two Times Smaller Channel Lengths vs. Single Gate (Planar) Designs**



Note: Includes Double gate, Tri-gate, Pi-gate, Omega gate and All-round gate.

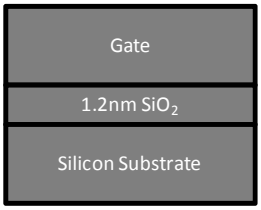
Source: *Nature* and Bernstein analysis.

Exhibit 44 High K Dielectrics Allow Better Capacitive Performance With Higher Thickness

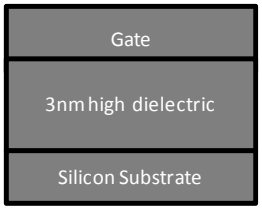
High-K Dielectrics allow higher Capacitance even with a higher thickness

$$C = \frac{k\,\varepsilon_o\,A}{t}$$

A is the capacitor area
κ is the relative dielectric constant of the material
ε_0 is the permittivity of free space
t is the thickness of the capacitor oxide insulator



Existing 90mm Process
Capacitance = 1x
Leakage Current = 1x



With a high-K dielectric
Capacitance = 1.6x
Leakage Current = 0.01x

With other operating constraints, higher Capacitance allows higher drive current

$$I_D = \frac{W}{L}\,\mu\,C_{inv}\,\frac{(V_G - V_{th})^2}{2}$$

Source: Bernstein analysis.

Exhibit 45 Summary of Current Transistor Manufacturing Issues and Industry Solutions to Extend Shrink to Below 5nm

	Technological Issues	Current Limit to Shrink Up to	Current Industry Solution	Extension Up to
1	Parasitic Capacitance	32nm	a) Silicon on Insulator (SOI), with planar	<20nm
	Latch up	(with bulk CMOS with planar architecture)	b) Multigate (or 3D) Transistors	~14-22nm
			c) SOI and 3D Transistors	5nm
2	Leakage across the gate dielectric	2nm for the gate	high-K gate dielectric	
3	Short Channel Effect	22nm	3D transistors	10nm
4	Electron Mobility	>10nm	3D transistors with alternative channel material	<7nm

Source: Bernstein analysis.

When to Mourn Moore's Law?

The economic side of Moore's Law is already entering a slow death, but shrinking feature size will continue to be in the headlines for the next 15 years.

The Economic Side of Moore's Law Is Dying a Slow Death Already

We have enough evidence that the roadblocks we have described are pushing up manufacturing costs, progressively absorbing the economic benefits of Moore's Law (see Exhibit 46). Today's transition to multiple patterning and the looming introduction of EUV are already taking their toll and it is only the beginning (see Exhibit 47).

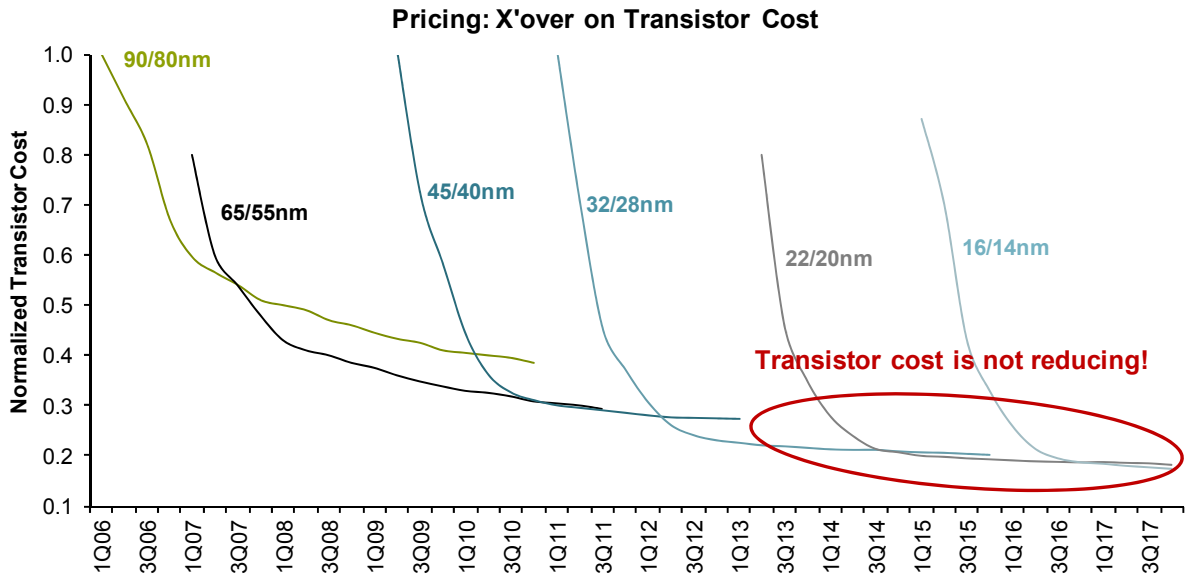
From that perspective, the most rigorous expression of Moore's Law (the cost of transistors halves every two years) is not going to be true going forward. If transistor density can continue to increase for some time, it happens at a steadily increasing cost.

We believe the capex per additional wafer start, which came down about 6% p.a. in the last 17 years, will now increase, between 9% and 15% p.a. going

forward, depending on the scenario we consider (see Exhibit 48). This is based on the assumption that capex per leading edge wafer start will shoot up by 50% between the 30 and 20nm nodes, then increase at a slightly lower pace and that the 450mm migration will introduce over time a ~30% cost reduction (see Exhibit 49).

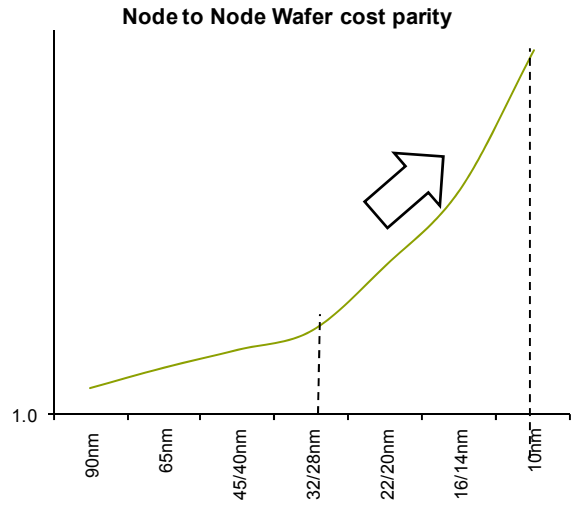
As a result, we model the average capital cost per transistor (including lagging edge) that declined on average 20% p.a. in the last 17 years to decline only 10-13% p.a. going forward (see Exhibit 50).

Exhibit 46 The Economic Side of Moore's Law Is Already Dying a Slow Death



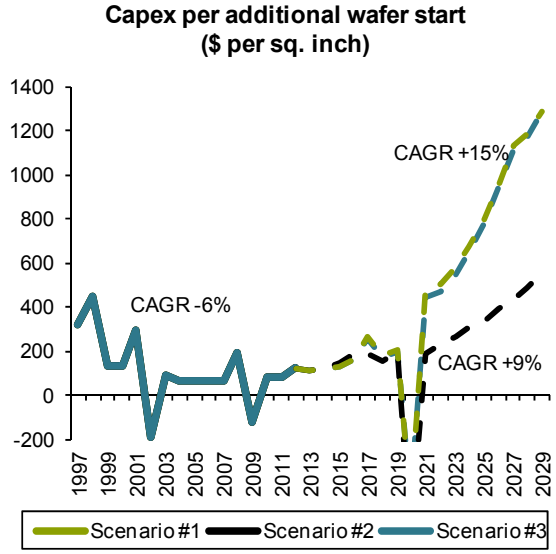
Source: Nvidia and Bernstein analysis.

Exhibit 47 But After That, EUV Multiple Patterning, New Transistor Architecture and Non-Silicon Technologies Are Likely to Add to the Costs Again



Source: TSMC and Bernstein analysis.

Exhibit 48 We Believe the Capex per Additional Wafer Start, Which Came Down About 6% p.a. in the Last 17 Years, Will Now Increase, Between 9% and 15% p.a. Going Forward



Source: Gartner and Bernstein estimates and analysis.

Exhibit 49 **This Is Based on the Assumption That Capex per Leading Edge Wafer Start Will Shoot Up by 50% Between the 32/28nm and 22/20nm Nodes, Then Increase at a Slightly Lower Pace and That the 450mm Migration Will Introduce Over Time a ~30% Cost Reduction**

Increase in Capex per leading edge wafer

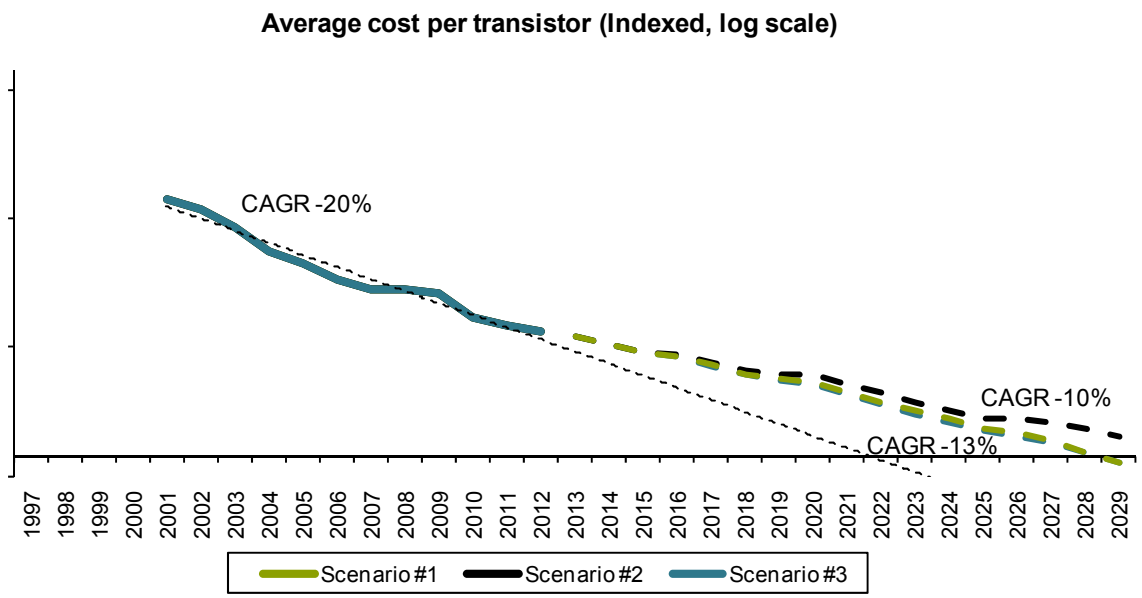
	2012-2014	*2014-2017*	*2017-2029*
Node progressions	22% p.a.	16% p.a.	16% p.a.
Saving from 450mm			-2.5% p.a.
	22% p.a.	16% p.a.	13.5% p.a.

Average Increase in Capex per leading edge wafer (2012-2029) 15% p.a.

Drivers	**Wafer capex inflation**
32/28nm-> 22/20nm	50% over 2 years
Subsequent node progressions	35% over 2 years
450mm saving	-30% between 2017-2029

Source: Bernstein estimates and analysis.

Exhibit 50 **As a Result, We Model the Average Capital Cost per Transistor (Including Lagging Edge) That Declined on Average 20% p.a. in the Last 17 Years to Decline Only 10-13% p.a. Going Forward**



Source: Gartner and Bernstein estimates and analysis.

This Isn't the "End of Shrink"

Historically, **for the same budget**, Moore's Law used to deliver about twice the performance every two years and this has been the main driver of the industry. As shrink becomes more challenging, this won't work anymore, but looking at performance only doesn't bring in the full picture.

Going forward, **for the same budget**, Moore's Law won't deliver the same performance improvement because the growth in transistor count will have to slow to keep cost in check. This will drive a mechanical reduction in die size and therefore power efficiency gains, compensating in some way for the slowdown in performance improvement. Exhibit 51 shows how these dynamics would play out in a scenario in which manufacturers compensate the structural increase in capital cost per wafer by a structural decrease in die size (scenario #3).

The mechanical improvement in power efficiency that a slowdown in the growth of transistor count would drive can't be ignored: The importance of power efficiency is growing fast (see Exhibit 52 through Exhibit 54) whereas the continued increase in performance may prove less critical, as it has in PCs (see Exhibit 55).

We don't have consensus within our global semiconductor team on how this will influence growth dynamics going forward and we discuss the matter later, along three scenarios (see Exhibit 63). In all cases, we see enough value in shrink for it to keep going, though possibly at a slower rate eventually.

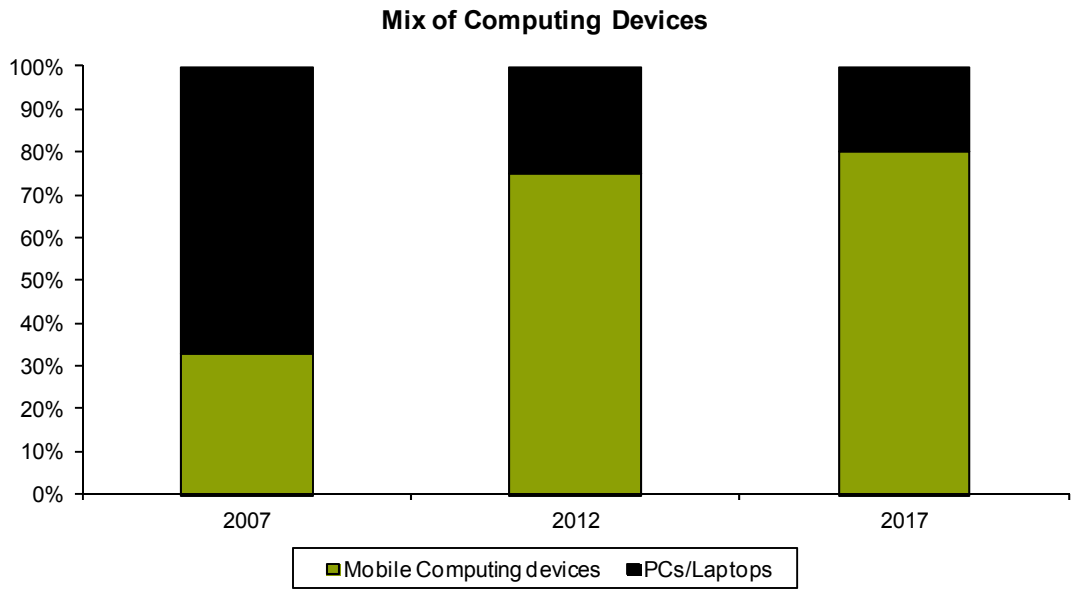
Exhibit 51 Going Forward, Continued Shrink Will Actually Deliver, for the Same Budget, Progressively Less Performance Improvement But More Power Efficiency Gains

		Before	Mourning Moore's Law
		n → n x .7	n → n x .7
Leading Edge	Chip Size	Unchanged	Down ~25%
	# of transistors / chip	Doubled	Up 50% only
	Cost per wafer	Slight Increase	Increase 30-40%
	Cost per chip	Slight Increase	Slight Increase
		y → y + 2 years	y → y + 2 or 3 years
Industry Average	Chip Size	~Unchanged	Down ~9%
	# of transistors / chip	Up ~40%	Up ~25%
	Cost per wafer	Down 10%	Up 4%
	Cost per chip	Down 8%	Down 4%

Note: Industry average based on scenario 3.

Source: Bernstein estimates and analysis.

Exhibit 52 **More and More Computing Devices Are Becoming Mobile, and Hence Value Power Efficiency**



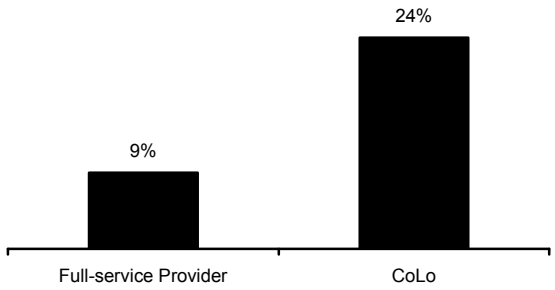
Source: Strategy Analytics and Bernstein estimates and analysis.

Exhibit 53 **Power Consumption vs. Server Capital Costs**

Wholesale ASP ($)	$2,500	
Lifetime (years)	3	
Annualized replacement cost ($)	$833	
Watt	308	
PUE	2.0	1.3
Annual Power (KWh)	5,392	3,505
Cost / KWh	$0.10	$0.10
Annual Power ($)	$539	$350
Power / CapEx	65%	42%

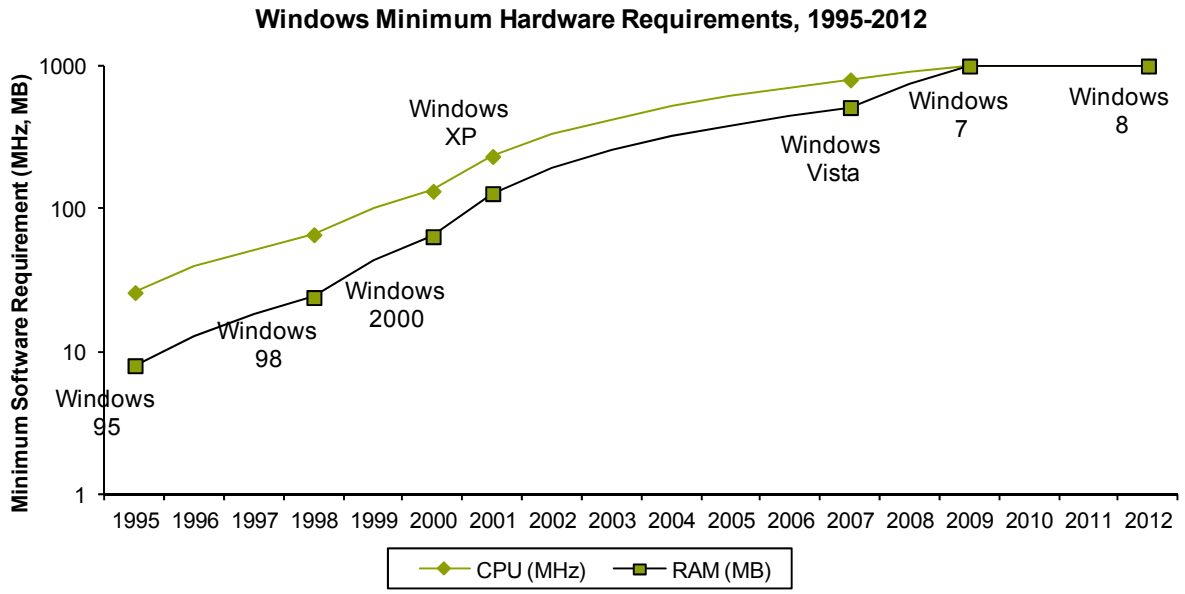
Source: Bernstein estimates and analysis (U.S. IT Hardware team).

Exhibit 54 **Power Costs as Percentage of Operating Expenses**



Source: Corporate reports and Bernstein analysis (U.S. IT Hardware team).

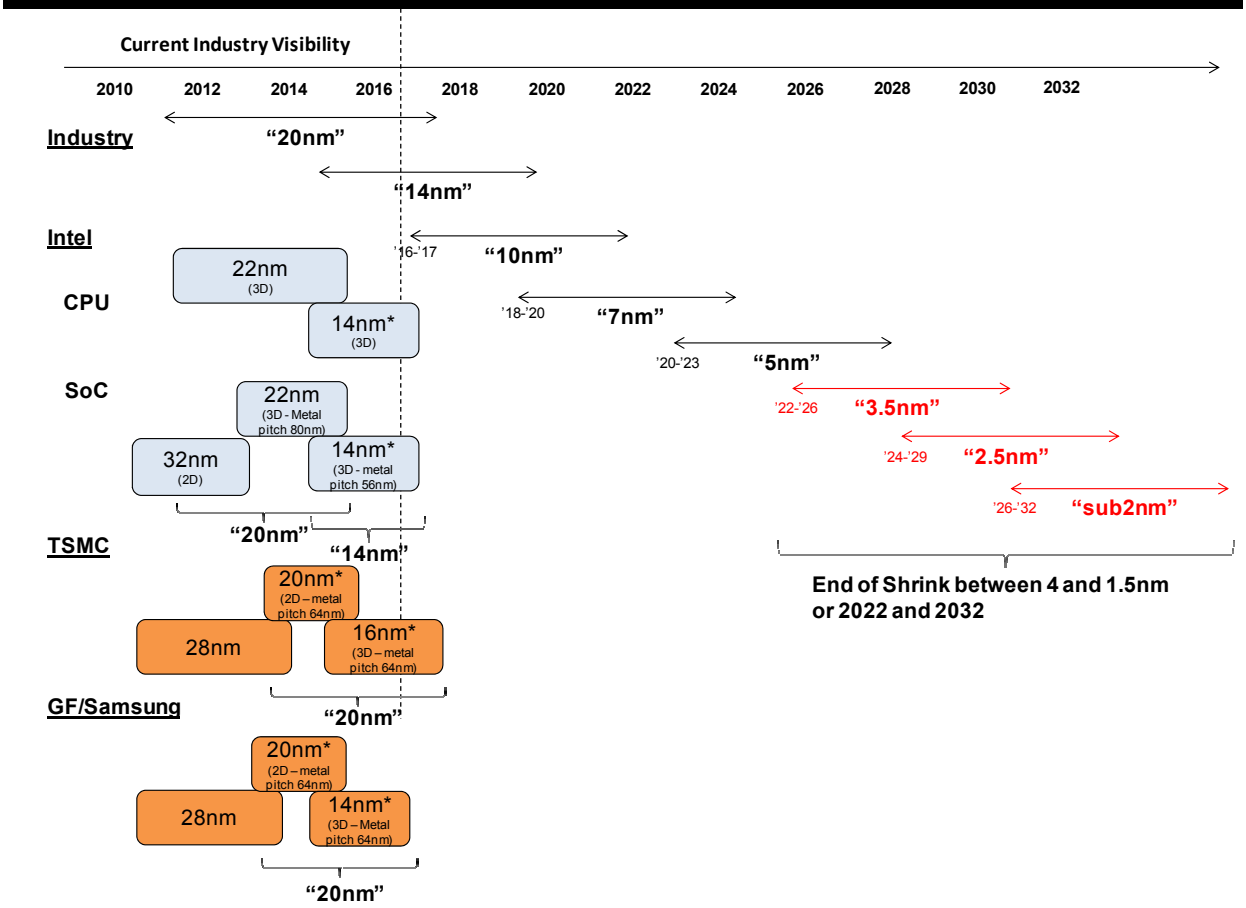
Exhibit 55 Minimum Hardware Requirements for New Software Have Saturated



Source: Microsoft and Bernstein analysis.

We expect the end of shrink to happen at a critical dimension between 4nm and 1.5nm and by 2030. We see the limitation imposed by the Shannon-von Neumann-Landauer expression as very fundamental and unlikely to be ever beaten, and as the practical path beyond 4nm is still very unclear, we expect the final point to Moore's Law to happen in that range, and not before the end of next decade (see Exhibit 56 and Exhibit 57).

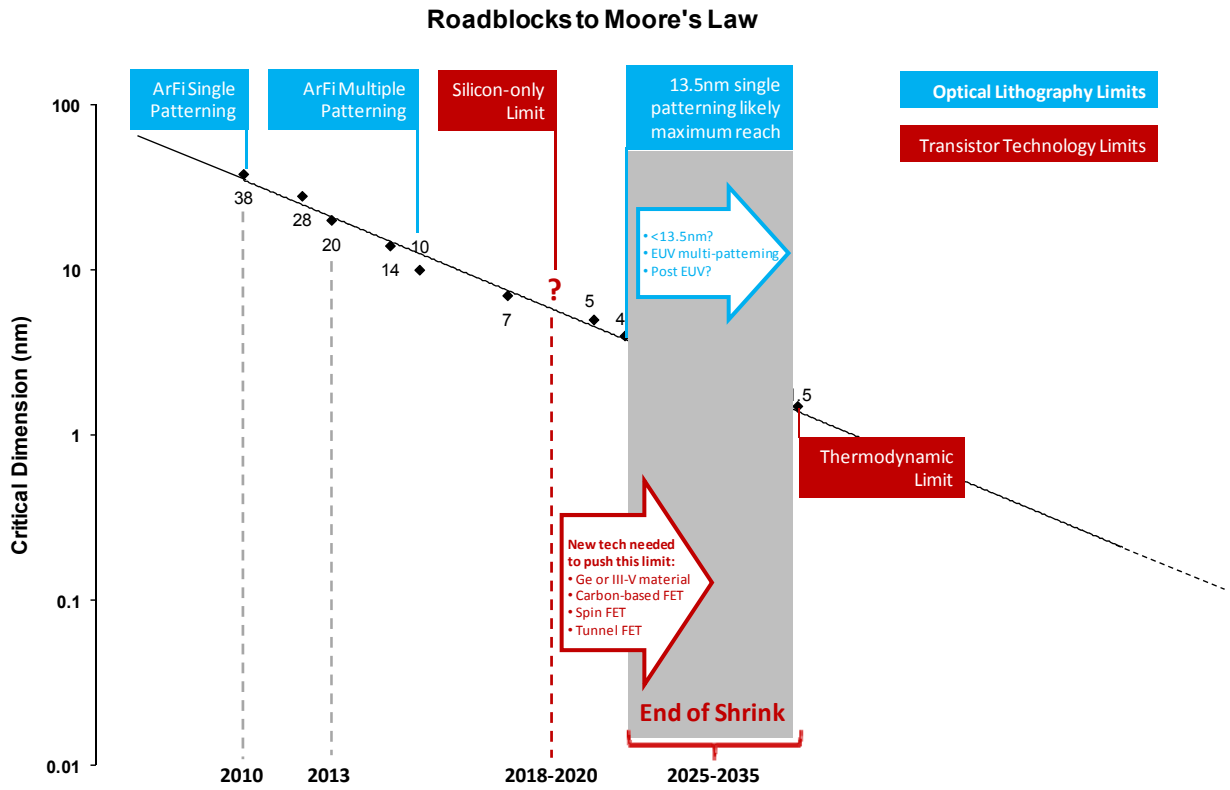
Exhibit 56 **When to Mourn Moore's Law? Already Today for Its Economic Side, and in 15 Years for "Shrink"**



* The 22nm, 20nm, 16nm, 14nm nodes of TSMC and Samsung are all based on the same critical dimension of ~20nm and metal pitch of 64nm. Intel's 22nm node has a larger critical dimension (metal pitch 80nm) and Intel's 14nm node smaller one (metal pitch 54nm)

Source: Bernstein estimates and analysis.

Exhibit 57 **Mourning Moore's Law: Many Roadblocks on the Shrink Road Going Forward**



Source: Bernstein estimates and analysis.

It is also worth noting that the end of Moore's Law isn't the end of innovation and productivity gains. The industry has many alternatives to Moore's Law, beyond natural efficiency gains we should expect from the maturing of all technologies involved in manufacturing.

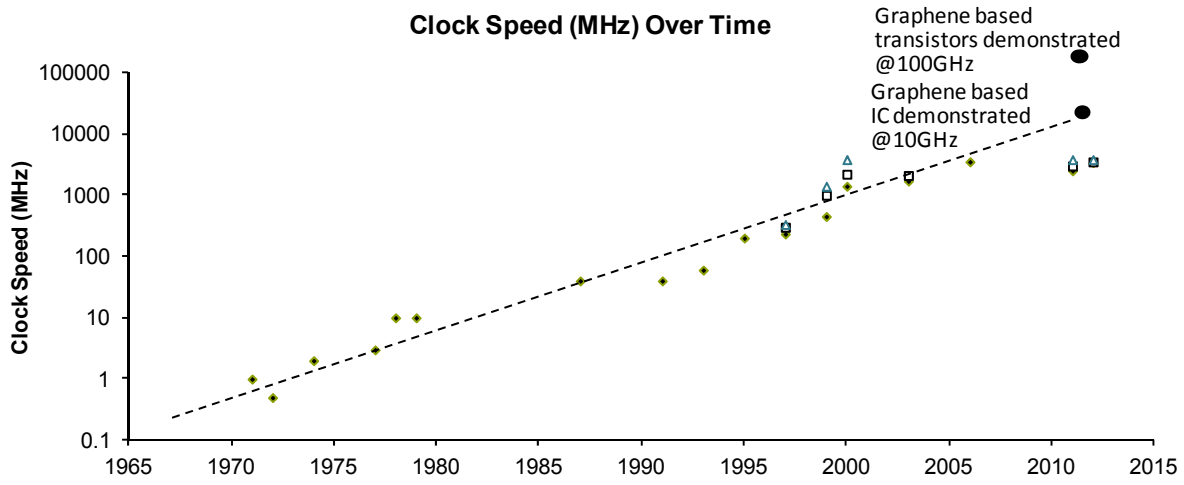
For instance, the introduction of higher mobility materials opens the doors to a new race for processor clock speed, 450 mm wafer manufacturing will provide in the coming year a very welcome productivity jump, 3D layout may speed up cost efficiency in memory, etc.

- **High Mobility Materials.** Carbon-based Field effect transistors have very attractive intrinsic transport characteristics that can support much higher carrier mobility, providing significantly faster clock speed that has saturated around 3-4Ghz over the past 10 years (see Exhibit 58). IBM researchers have created the first Graphene-based ICs that can withstand temperatures up to 127°C and operate at frequencies as high as 10 GHz. Transistors operating at 100 GHz have been demonstrated. These innovations bring us back to the historical trend of ever-increasing clock speed and provide room for further extension of this phenomenon. Moreover, the "band gap" of Graphene can be tuned and is very low compared to Silicon, allowing better power efficiency.
- **Wafer size**. When increasing the wafer size, increased area is the biggest productivity gain that offsets all the major elements of cost increases, such as more expensive equipment and lower throughput of beam tools. Overall, for instance, the transition of wafers from 300mm to 450mm can yield a net 20-40% saving in transistor cost (see Exhibit 59). Assuming the same chip die size, the capex per fab for the same chip throughput can be reduced by over 25% (see Exhibit 60). In the past, the wafer area has more than doubled (2.25x) roughly every 10 years. 450mm, despite taking longer than prior wafer size transitions,

should be an important step to lower the manufacturing cost in the future (see Exhibit 61).

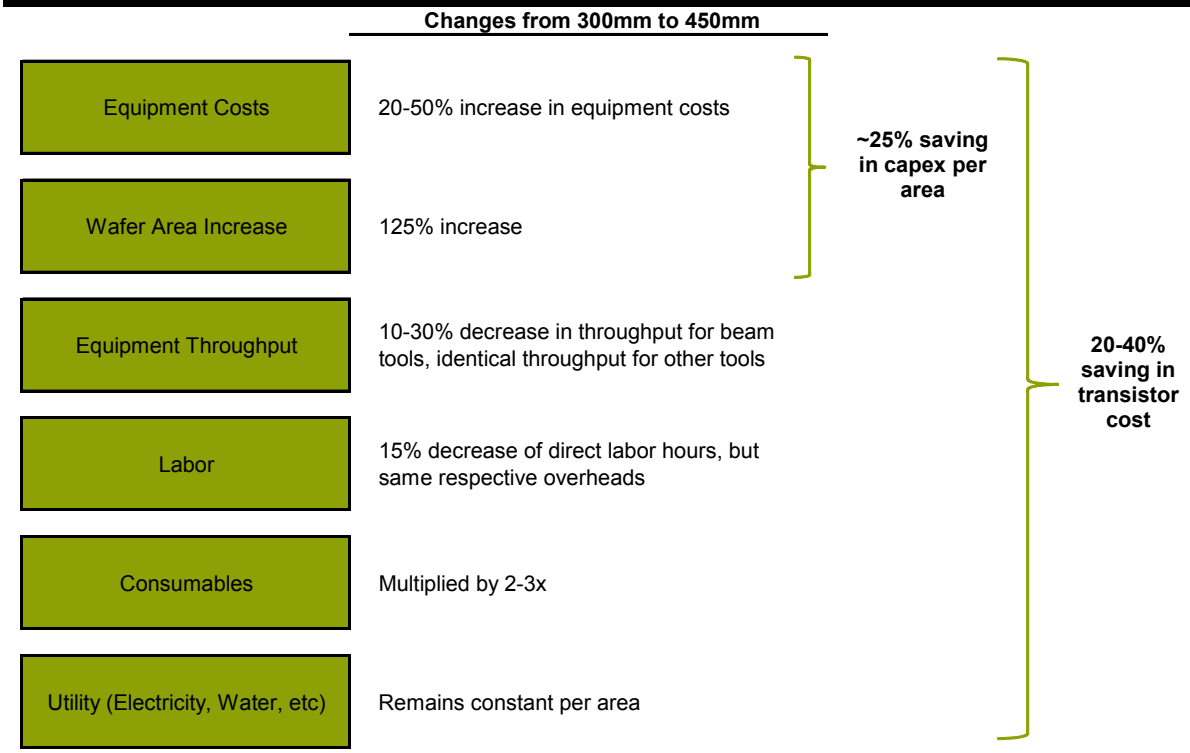
- **3D Layout in Memory**. 3D memory architectures will be key to continuing cost declines beyond 10nm. The concept simply involves stacking cells on top of each other instead of laying them flat on a surface, enabling higher packing density. Already, most major memory manufacturers are heavily investing in different types of 3D or vertical NAND architectures (see Exhibit 62).

Exhibit 58 **Processor Clock Speed May Increase to as High as 100GHz, With Use of New Materials That Enable Higher Carrier Mobility**



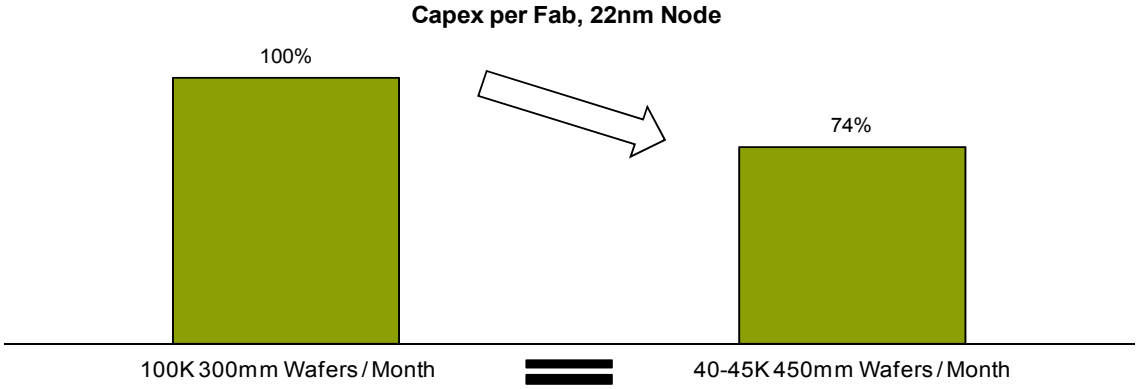
Source: IBM, Buzzle.com and Bernstein analysis.

Exhibit 59 **Current Cost Models Support 450mm and Can Achieve Cost Reduction Similar to 300mm Transition**



Source: IC Knowledge, GlobalFoundries, TSMC and Bernstein estimates and analysis.

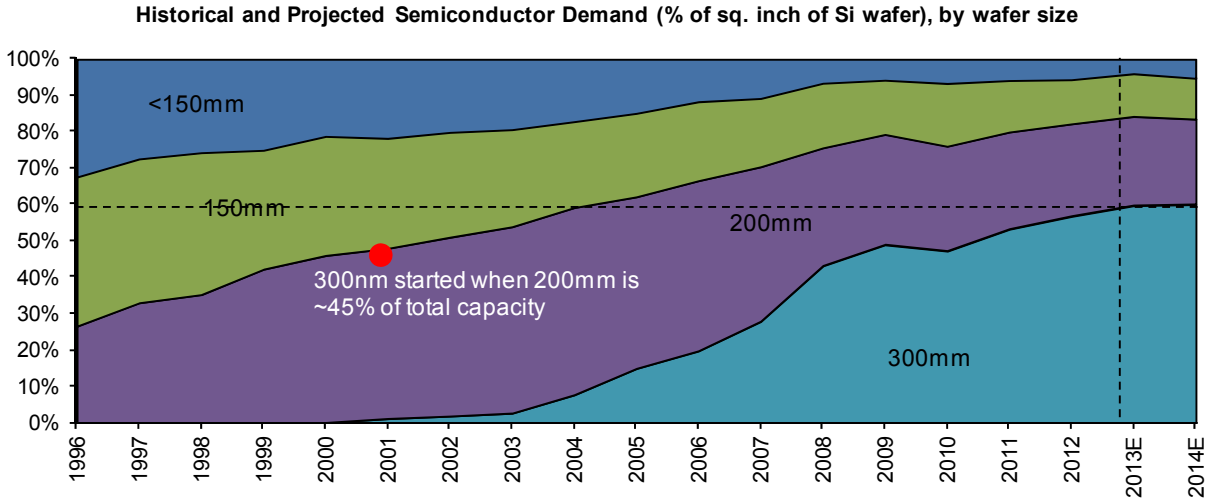
Exhibit 60 **Chipmakers Can Benefit from the Lower per-Wafer Capex Requirement of 450mm**



Note: For 5mm x 8mm die size, 300mm fab produces approximately 1,450 dies, while 450mm fab produces approximately 3,400 dies per wafer. Assume 22nm, 40,000 wafers per month in 450mm, is equivalent to 100,000 wafer per month in 300mm.

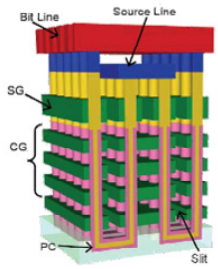
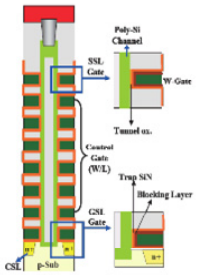
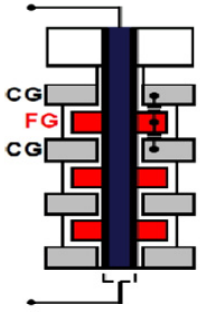
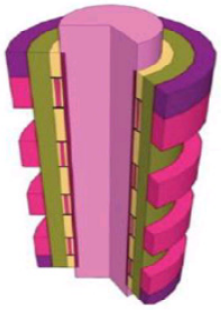
Source: GlobalFoundries, IC Knowledge and Bernstein analysis.

Exhibit 61 **In the Past, the Wafer Area Has More Than Doubled (2.25x) Roughly Every 10 Years**



Source: TEL, IC Knowledge, TSMC and Bernstein estimates and analysis.

Exhibit 62 **Already, Most Major Memory Manufacturers Are Heavily Investing in Different Types of 3D or Vertical NAND Architectures**

	p-BiCS (Toshiba)	TCAT (Samsung)	3D FG (Hynix)	Micron
Structure	 Tanaka. H, VLSIT 2007	 J. Jang, VLSIT 2009	 S. Whang, IEDM 2010	 G. Hawk, FMS 2011
Key Features	- P+ SONOS Cell	- TANOS Cell	- Floating Gate	?
Key Issue	- Large Cell Size - Reliability	- Large Cell Size - SL Resistance	- Process of bit separation - Disturbance	?

Source: SK Hynix.

Implications for the Industry? This Is Not the End…on the Contrary

The end of Moore's Law is often viewed as the dusk of the industry. Our research suggests the mourning of the Law will actually last long and keep the industry going, but at a cost. We see three potential scenarios (see Exhibit 63).

Scenario #1: The Mourning of Moore's Law Structurally Affects End-Demand

Elasticity matters on the demand side, and end markets cannot absorb broad cost increases. With manufacturing costs increasing, unit shipment growth slows down, squeezing the industry for the long term (see Exhibit 64).

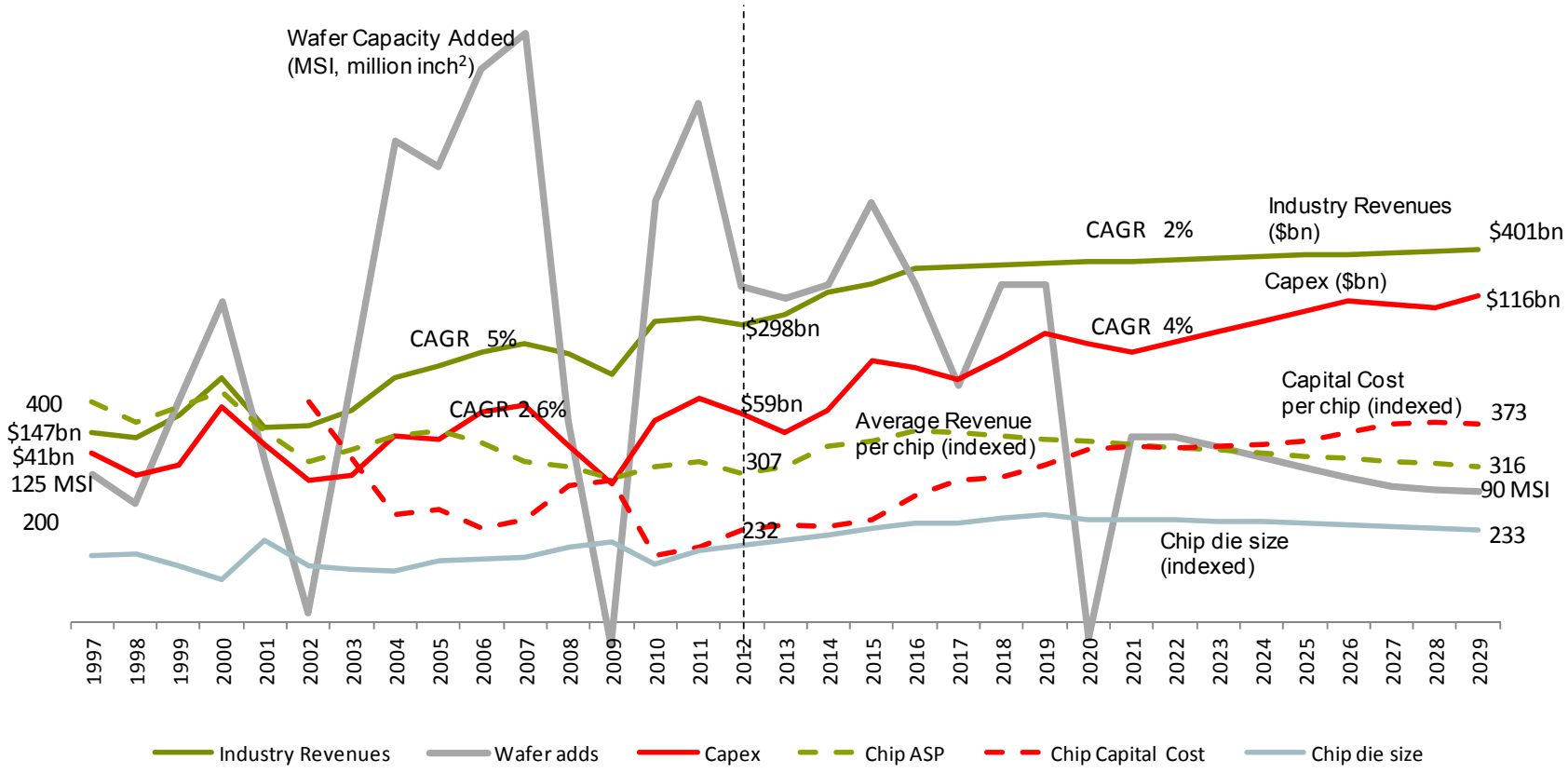
- In this scenario, we model an increase of 15% p.a. of the capex per additional wafer start, and a stable die size. This results in a steady increase in capital cost per chip at the leading edge that turns, as an industry average (leading and lagging edge) into an increase in the capital cost per chip of 3% p.a. versus a decline of 4% p.a. in the past.
- We then assume in this scenario that manufacturers pass on to customers this cost increase, which results in a flattening of revenues per chip versus a 2% p.a. decline in the past. This destroys demand, bringing down industry shipment growth to below 2% p.a. versus close to 7% in the past.
- As a consequence, the growth of industry revenues slows to below 2% versus close to 5% in the past, despite an acceleration of capex growth (4% vs. 2.6% in the last 17 years). Most obviously, this scenario creates material margin pressure across manufacturers and foundries, along with an industry going almost ex-growth.

Exhibit 63 Mourning Moore's Law: Summary of the Three Potential Outcomes for the Industry

	Scenario 1 *End demand structurally reduced* (CAGR)		Scenario 2 *Margins squeezed at chipmakers* (CAGR)		Scenario 3 *Power efficiency quest keeps status quo* (CAGR)	
	1997-2012	2012-2029	1997-2012	2012-2029	1997-2012	2012-2029
Capex per additional wafer capacity ($ / sq inch added)	-6.4%	15.0%	-6.4%	9.4%	-6.4%	15.0%
Revenue per wafer	-2.1%	-0.4%	-2.1%	-0.8%	-2.1%	2.4%
Capital cost per wafer	-5.3%	2.1%	-5.3%	5.0%	-5.3%	2.2%
Revenue per chip	-1.7%	0.2%	-1.7%	-1.0%	-1.7%	-1.9%
Capital cost per chip	-3.7%	2.8%	-3.7%	4.8%	-3.7%	-2.0%
Revenue per transistor	-16.6%	-15.0%	-16.6%	-15.3%	-16.6%	-12.6%
Capital cost per transistor	-19.5%	-12.8%	-19.5%	-10.4%	-19.5%	-12.8%
Chip die size	0.4%	0.6%	0.4%	-0.3%	0.4%	-4.2%
Transistors per chip	17.8%	18.0%	17.8%	17.0%	17.8%	12.3%
Wafer Growth	7.1%	2.2%	7.1%	3.7%	7.1%	2.2%
Chip growth	6.7%	1.6%	6.7%	4.0%	6.7%	6.7%
Industry revenue	4.8%	1.8%	4.8%	2.9%	4.8%	4.6%
Industry Capex	2.6%	4.0%	2.6%	9.5%	2.6%	4.0%

Source: Gartner and Bernstein estimates and analysis.

Exhibit 64 Scenario #1: The Mourning of Moore's Law Structurally Affects End-Demand



Source: Gartner and Bernstein estimates and analysis.

Scenario #2: The Mourning of Moore's Law Squeezes Margins

Manufacturers continue to deliver a steady improvement in performance, but at an increasing cost. Competition keeps the chase for incremental demand vivid, at best keeping chip ASPs on their historical trajectory, i.e. not enough to keep up with increasing costs. Margins pay the bill (see Exhibit 65).

- In this scenario, we model an increase of only 9% p.a. in capex per additional wafer start. This is based on the same economic model of other scenarios and described in Exhibit 49, but with a stronger wafer addition, which turns into less modernization capex and therefore a structurally lower capex per wafer addition.
- We take the view in this scenario that wafer additions keep going at a good rhythm because manufacturers, in a fierce battle for market share and growth, absorb the extra cost and keep die size stable and ASPs declining.
- As a result, this scenario creates massive pricing pressure on manufacturers (and foundries) with capex growing at three times the rate of revenues and capital cost per wafer growing 5% a year versus revenues per wafer declining around 1% a year.
- Obviously, this scenario creates even more pressure on industry margins and would actually be unsustainable beyond a few years.

Scenario #3: Power Efficiency Matters and Saves the Industry

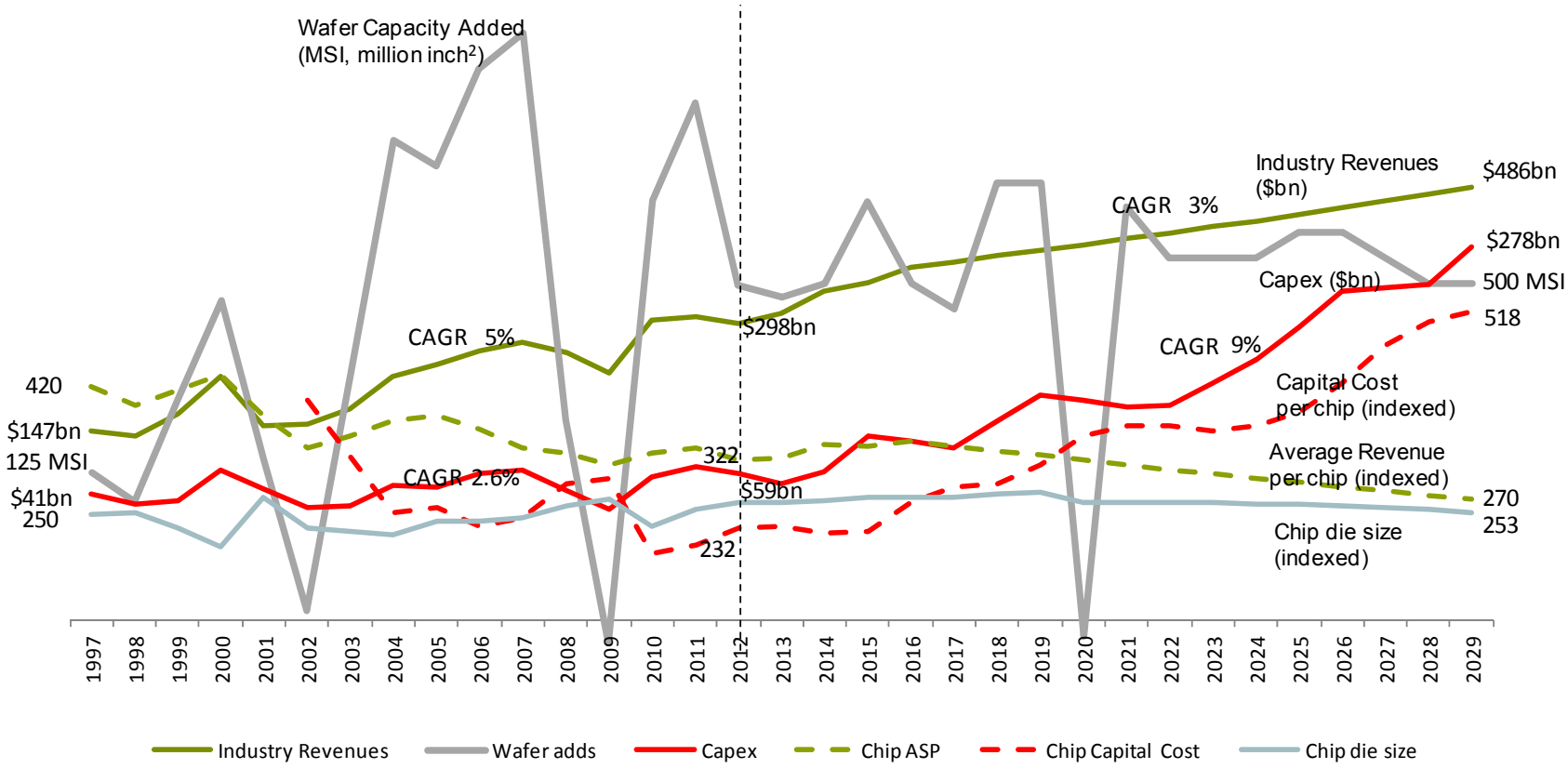
As the decline in capital cost per transistor flattens, manufacturers slow the increase in transistor count per chip, delivering less incremental performance, but more power efficiency, as die sizes come down. This is valued by customers and keeps chip costs stable (even as wafer costs rise), and end demand intact. As a result, units and revenues stay on steady historical trends, but wafer addition slows (see Exhibit 66).

- In this scenario, we model an increase of 15% p.a. of the capex per additional wafer start as well, but a shrinking die size (down 4% p.a. vs. historically flat for the overall industry). This results in the capital cost per chip staying on a trajectory similar to what we saw in the last 17 years (2% p.a. decline).
- The key assumption of this scenario is that chip ASPs do not suffer much from this decline in die size: customers continue to pay the same price for less performance improvement but for more power efficiency. We therefore model chip ASPs staying on their 2% p.a. decline trend line.
- As a result, demand is preserved, the industry continues to grow at its historical growth rate and capex intensity stabilizes, versus a steady decline in the past, which turns into capex growing faster, at 4% p.a. versus 2.6% p.a. in the past. But wafer additions slow, from 7% p.a. to 2% p.a., as each wafer carries more and more chips.
- This scenario is the most favorable to manufacturers, with good growth and margins well defended, but the question of how margins would evolve at foundries remains open…and will mostly depend on the intensity of competition between the three or four major players, which we see ramping up at the moment (see our "Silicon Wars" series for more details).

Given the competitive landscape we described last year in the "Silicon Wars," we collectively don't give a high probability to the first scenario, at least in the near future, in which manufacturers should remain competitive on prices and keep demand high.

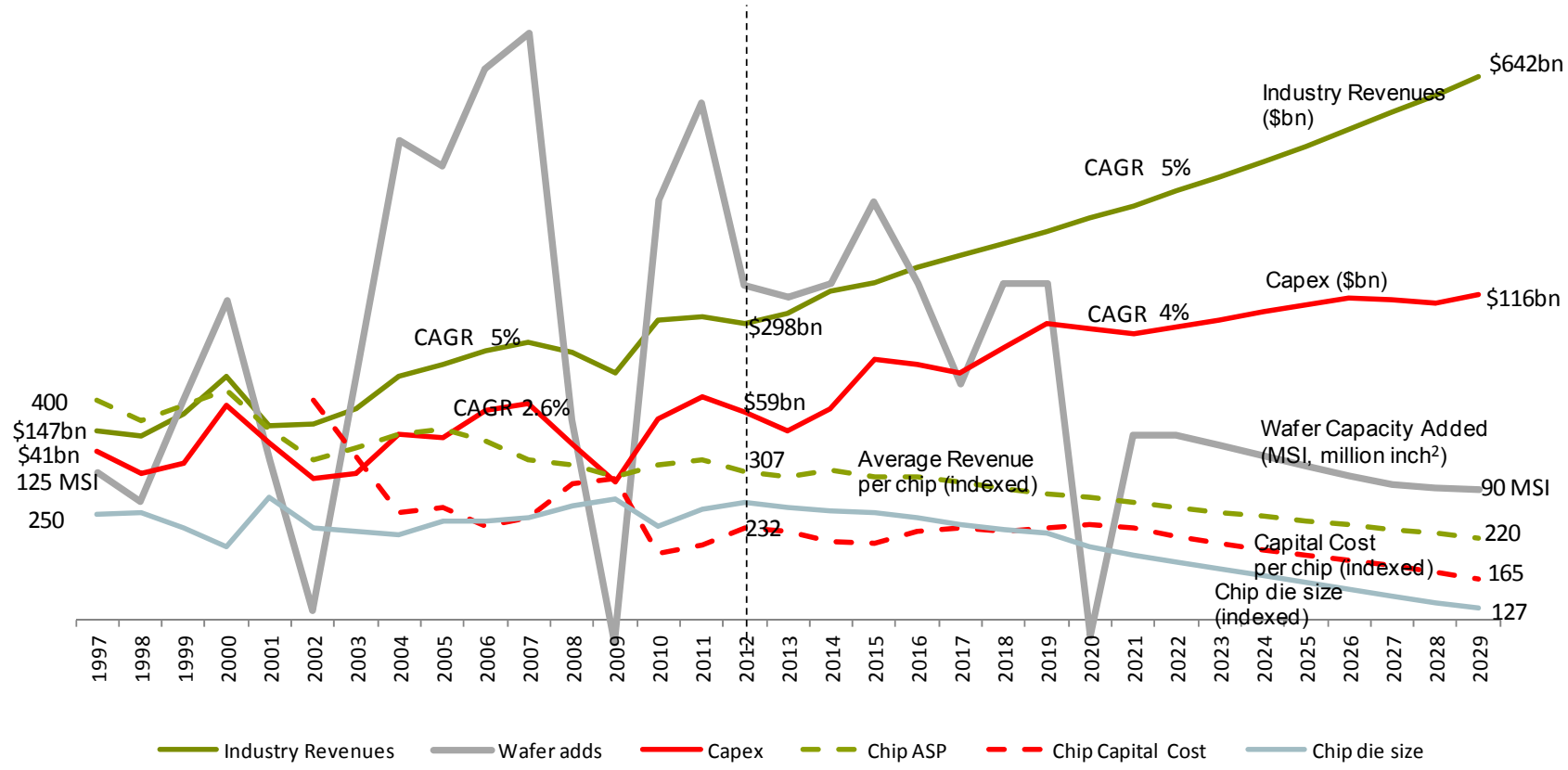
Some of us see the second scenario as the most likely, at least in the near term. As it is probably not a sustainable one on a 10- to 15-year horizon, they recognize a possible ultimate evolution along the lines of the third or even the first scenario. Some of us see the third as the most likely, but recognize the risk of a painful transition in the coming years, along the lines of the second scenario! All in all, we all value the perspective of each other and collectively agree that things are more likely to play out over time somewhere between the second and third scenarios and we base our research on this assumption.

Exhibit 65 Scenario #2: The Mourning of Moore's Law Squeezes Margins



Source: Gartner and Bernstein estimates and analysis.

Exhibit 66 Scenario #3: Power Efficiency Matters and Saves the Industry



Source: Gartner and Bernstein estimates and analysis.

Dawn or Dusk for Semi Capital Equipment Manufacturers?

Mourning Moore's Law: More Capex and Less Wafer Starts

In this chapter, we review implications for equipment manufacturers. Overall, we expect growth in the semi-cap industry to be stronger in the next decades than it was in previous ones, whatever the evolution scenario we consider. At the same time, all process steps won't benefit equally, there will be winners and losers.

For Lithography, mourning Moore's Law means a structural increase in market size, as more and more expensive scanners are required to shrink transistors further. For Metrology and Inspection, more challenging feature size also means a structural increase in spending, but with a more open competitive outlook: technological turns open the door to share shifts between players.

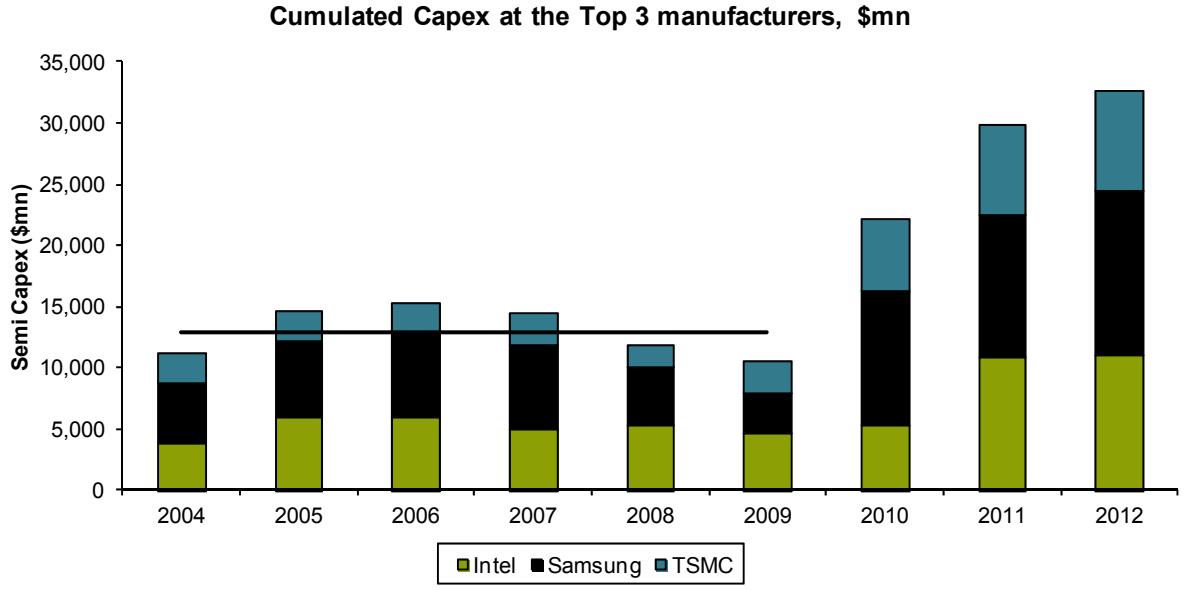
In most other manufacturing steps, we actually see challenging times ahead, as we believe the primary economic driver there is the number of wafer starts, whose growth we see abating, under the combined effect of the growing manufacturing cost per wafer and the migration to 450mm wafers.

In our coverage, ASML is a structural winner and remains a top pick.

More Expensive Wafer Starts Can't Be Bad for Capital Equipment

If mourning Moore's Law is about more expensive wafer starts, it can't be bad for capital equipment spending as a whole — and indeed it isn't. We described in our Silicon War research last year how competition for manufacturing leadership structurally increased capital expenses at leading foundries and IDMs. Combined with the concentration of the industry, the picture is fairly impressive. Cumulated capex of the top three manufacturers reached ~$33 billion last year, versus an average of $13 billion from 2004 to 2009 (see Exhibit 67)

Exhibit 67 **Cumulated Capex of the Top Three Manufacturers Reached ~$33 Billion Last Year, vs. an Average of $13 Billion Between 2004 and 2009**

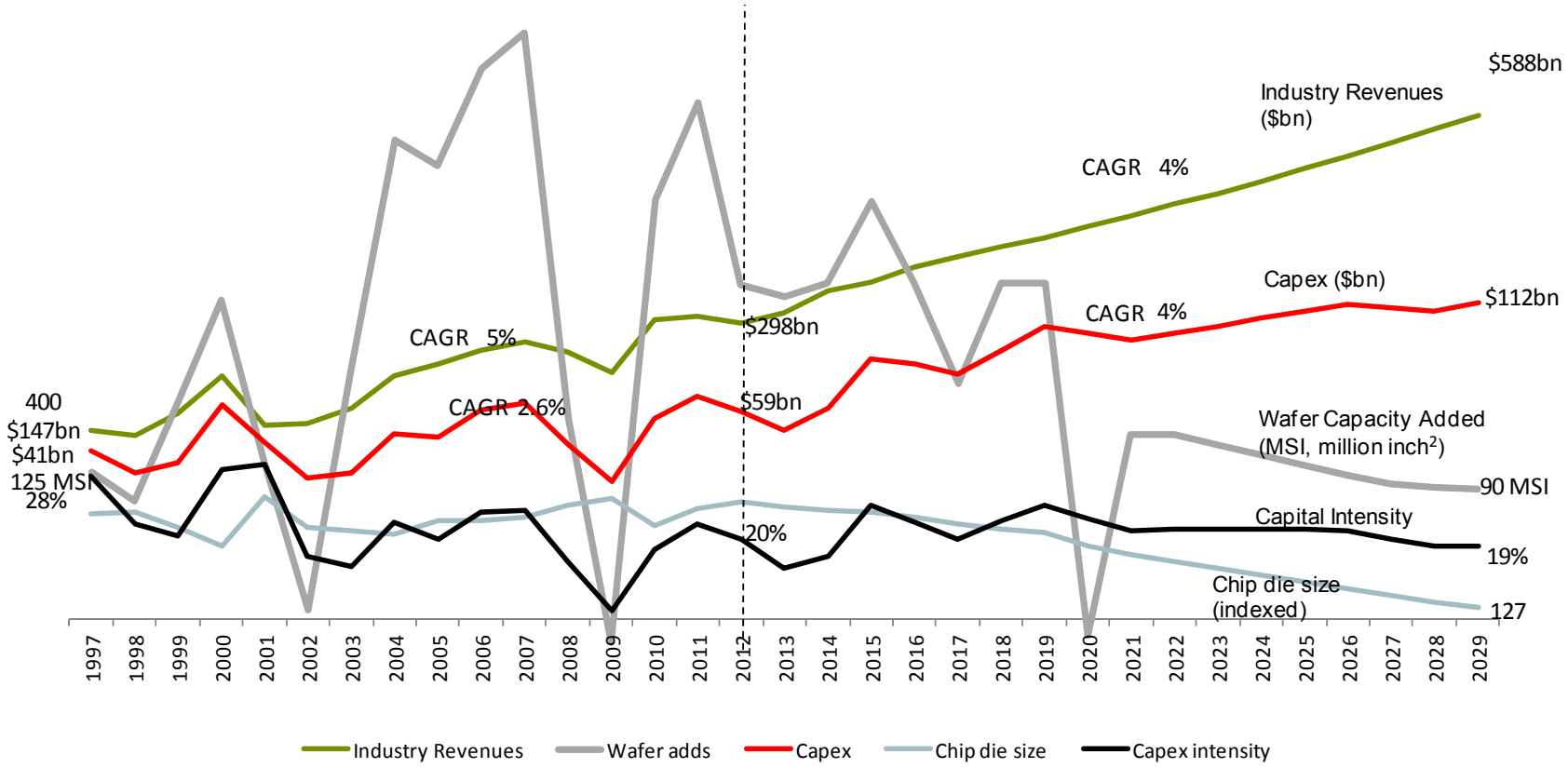


Source: Corporate reports and Bernstein analysis.

We don't see the trend inverting in the future. In our most conservative scenario for equipment manufacturers (i.e., scenario #3), as wafers get more and more expensive to produce, we expect the number of chips per wafer to increase, balancing out the increase in cost per wafer and keeping industry capex as a percentage of sales flat, versus a structural decline in the past (see Exhibit 68).

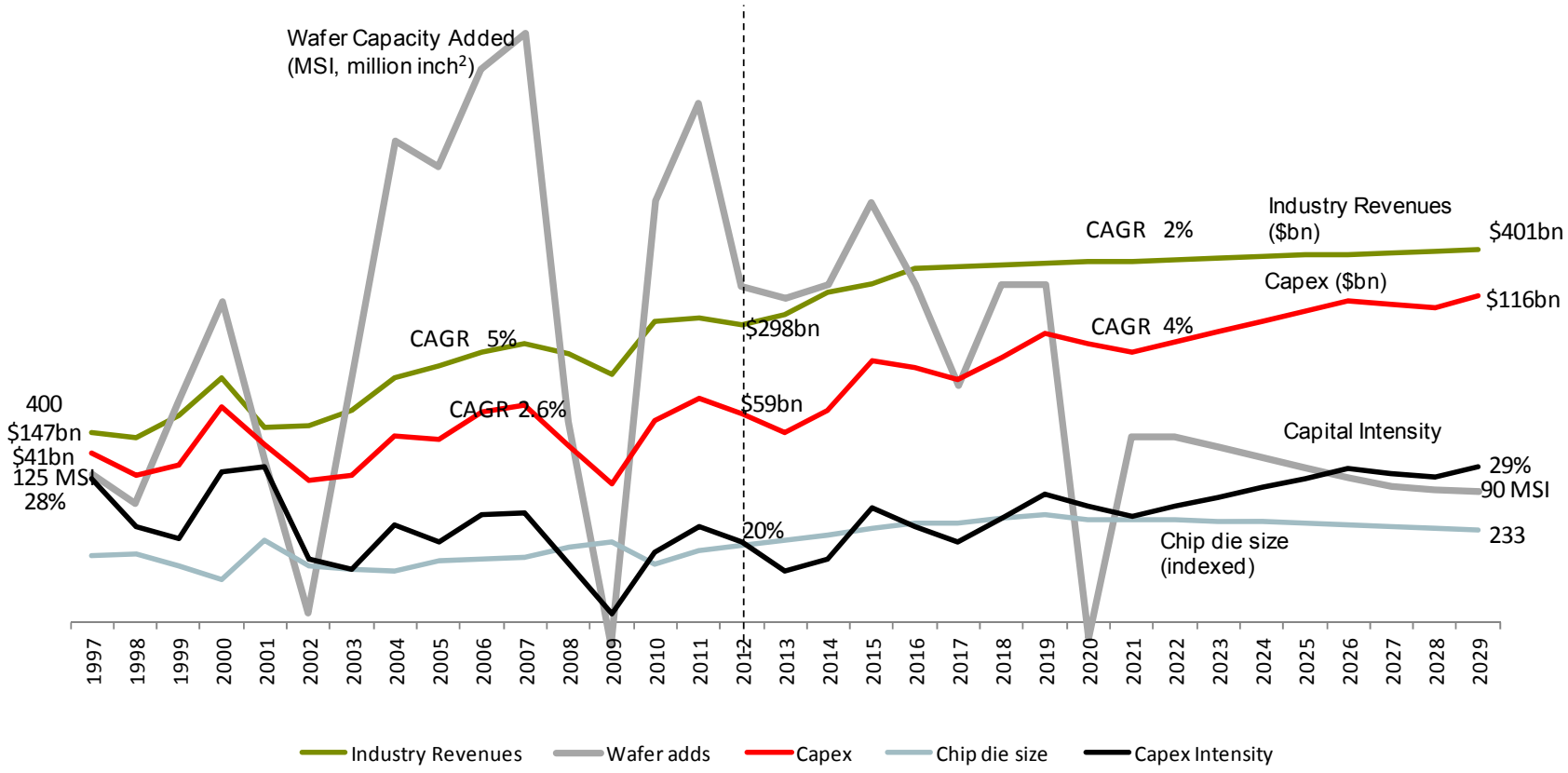
In more cautious scenarios, in which manufacturers can't reduce the average die size and either destroy end-demand, passing on cost increases to customers, or take a significant margin hit, capital intensity increases significantly more over time (see Exhibit 69 and Exhibit 70).

Exhibit 68 Scenario #3: Power Efficiency Matters and Saves the Industry; Conservative Scenario for Capex Intensity Going Forward



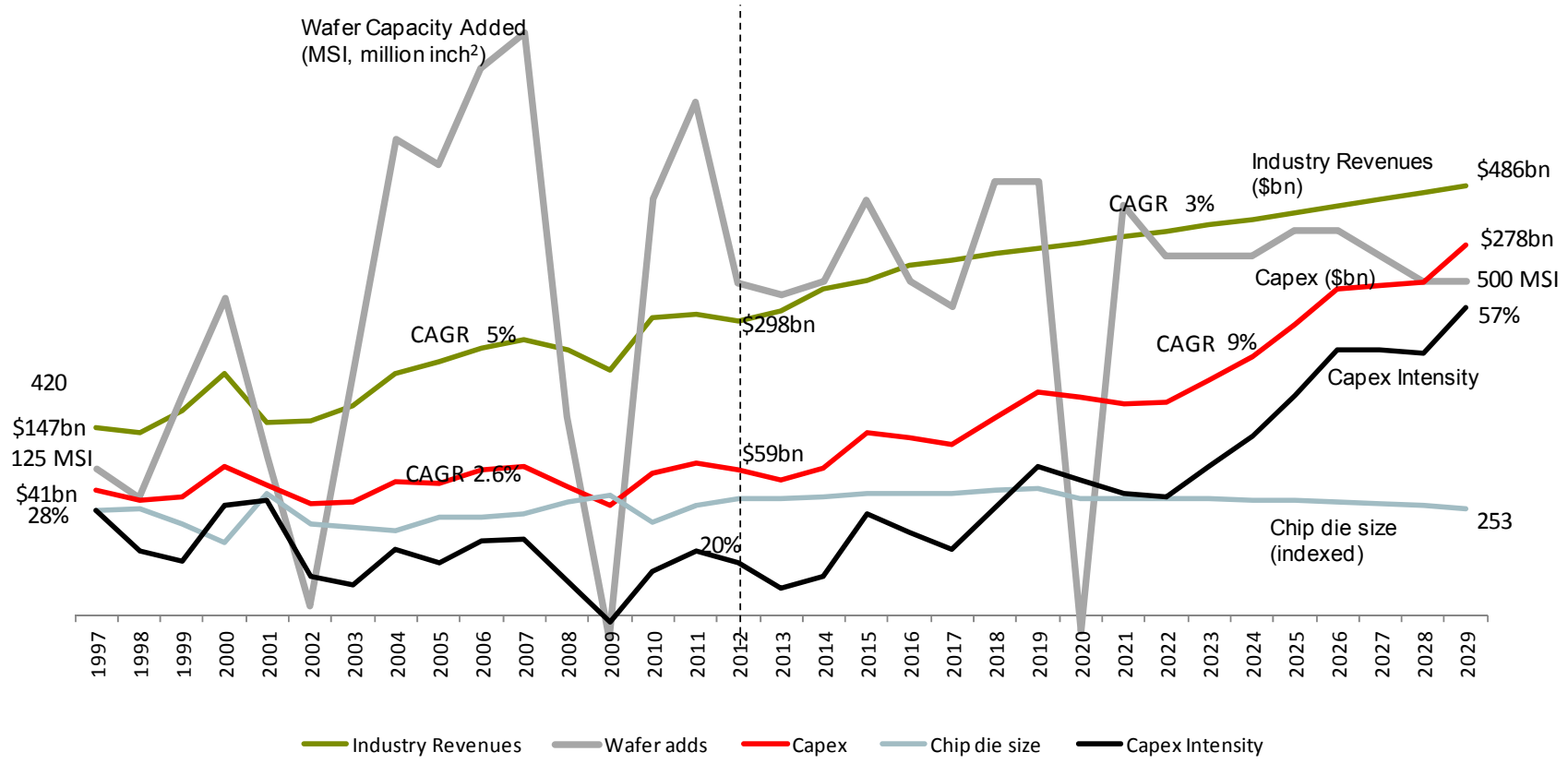
Source: Gartner and Bernstein estimates and analysis.

Exhibit 69 Scenario #1: The Mourning of Moore's Law Structurally Affects End-Demand



Source: Gartner and Bernstein estimates and analysis.

Exhibit 70 Scenario #2: The Mourning of Moore's Law Squeezes Margins

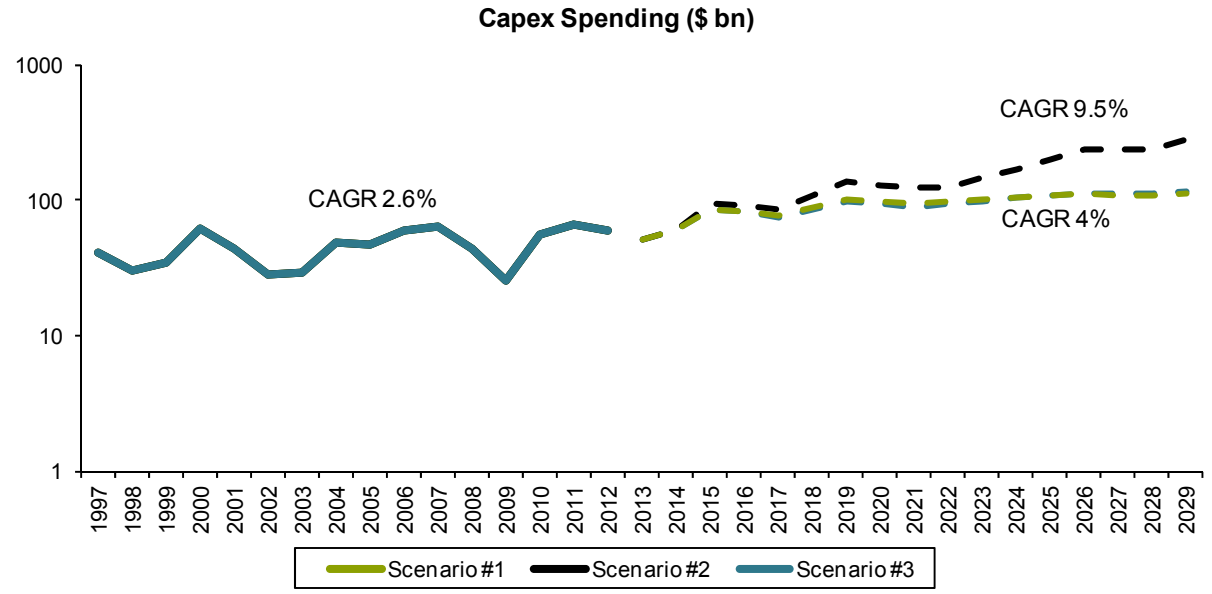


Source: Gartner and Bernstein estimates and analysis.

These trends are summarized in Exhibit 71 and Exhibit 72: we expect capex to grow 4% to ~10% per annum in the next 17 years, versus 2.6% in the last 17 years, and an average capex intensity of 21% to 34% going forward, in line with historical levels.

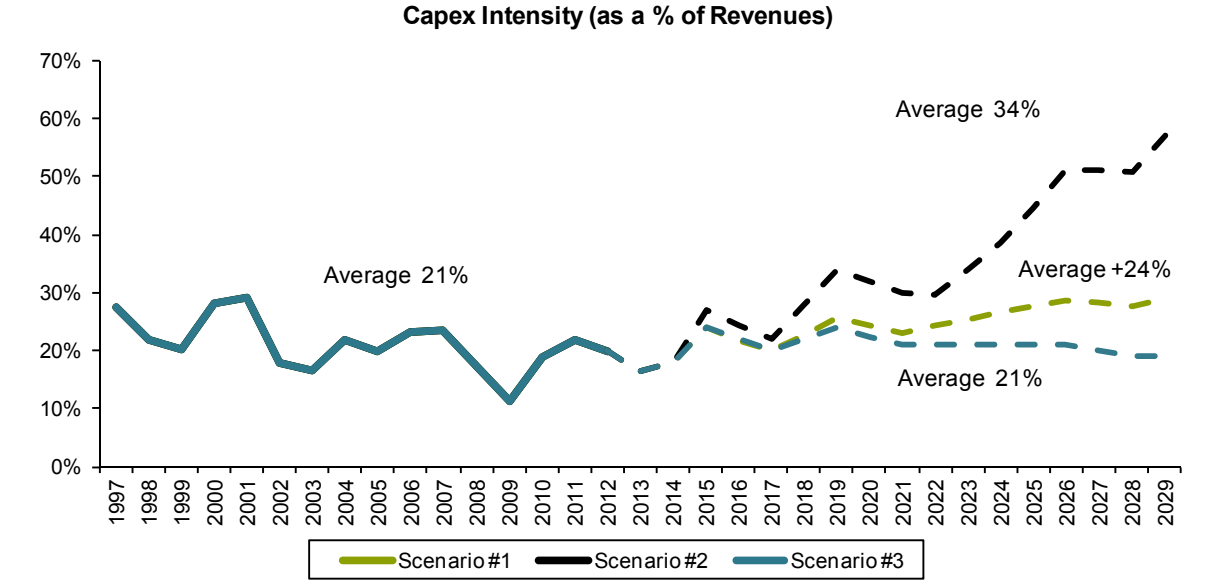
Moreover, with a slowdown in wafer additions, we expect equipment spending to stay stable as a percentage of total capex and therefore growing 4% going forward, versus 2.1% p.a. historically (see Exhibit 73). Our other scenarios would result in even higher (and actually unsustainable) levels of growth (12% p.a.).

Exhibit 71 **We Expect Capex to Grow 4-10% p.a. in the Next 17 Years, vs. 2.6% in the Last 17 Years…**



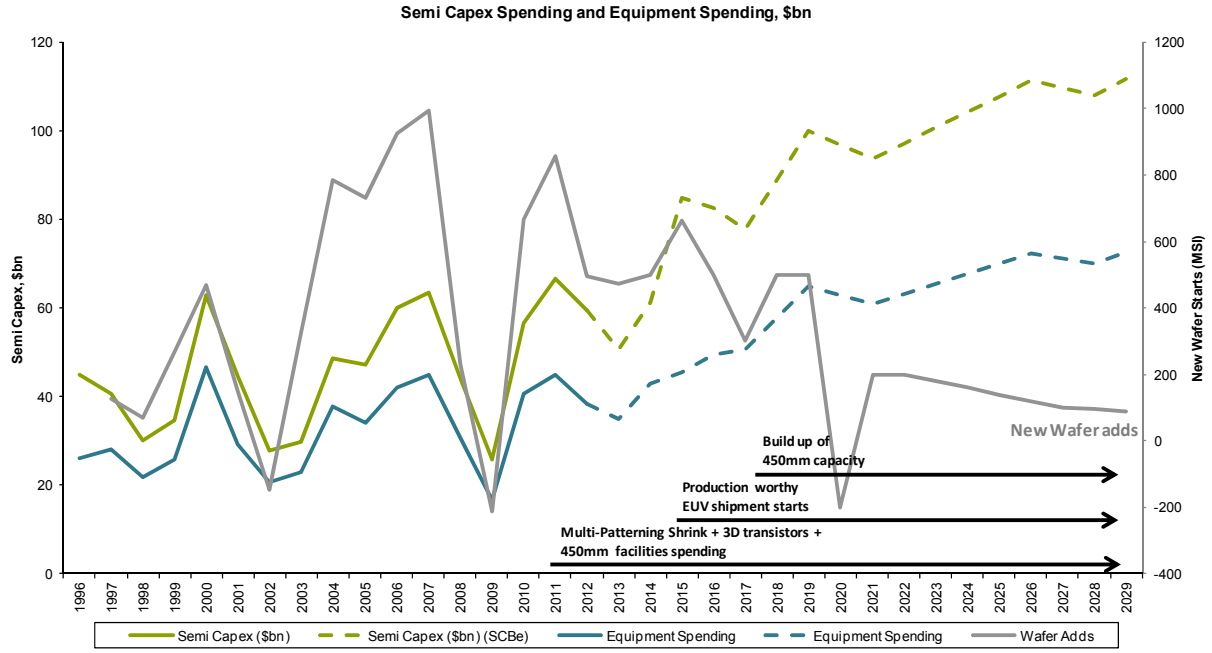
Source: Gartner and Bernstein estimates and analysis.

Exhibit 72 **...and Capex Intensity to Average in a 21-34% Range Going Forward, vs. an Average of 21% in the Past**



Source: Gartner and Bernstein estimates and analysis.

Exhibit 73 **Semi Capex Spending and Equipment Spending Will Continue to Increase Driven by Multi-Patterning, 3D, EUV, 450mm Related Spending**



Source: Bernstein estimates and analysis.

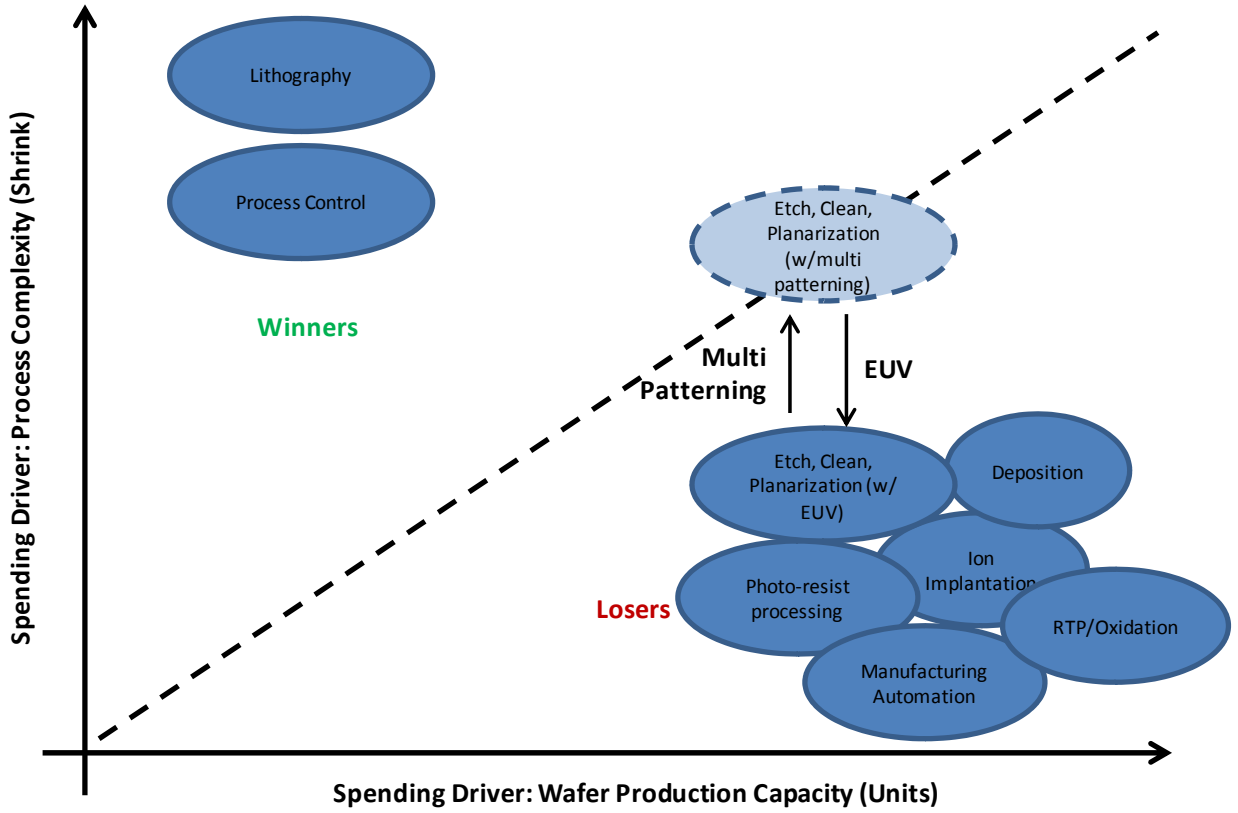
But This Doesn't Imply All Equipment Manufacturers Will Benefit

We summarize our perspective in Exhibit 74**.**

Winning segments are process steps at the origin of the increase in cost per wafer**:** Lithography; Process Control.

Losing segments suffer from the decline in wafer additions we anticipate under the combined effect of increasing costs per wafer and the 450mm migration: Etch, Clean and Planarization; Deposition; RTP/Oxidation; Ion Implantation; also Photo-Resist Processing; Manufacturing Automation.

Exhibit 74 Growth Drivers for Semi-Cap Equipment: Process Complexity and Wafer Additions



Source: Bernstein analysis.

Etch, Clean and Planarization May Benefit Only from a Mild and Temporary Boost

Etch, Clean and Planarization may benefit from a mild and temporary boost, driven by DUV multiple patterning, but will remain challenged in the long run, suffering from a slowdown in wafer additions.

For the 32nm to 22nm transition enabled by multiple patterning, we estimate >50% overall increase in equipment costs (see Exhibit 75 through Exhibit 78). The increase, however, will be unevenly spent across process steps. We estimate Process Control and Lithography-related spending to increase by 70% and 90%, respectively, versus Etch-related spending increasing ~20%. This is mostly because leading-edge equipment used for critical layers in Lithography and Process Control is often a multiple of non-critical equipment. For instance, ASML's ArFi tools have an ASP of ~€40 million versus an average of ~€10 million for rest of the tools. In wafer inspection, leading-edge tools are roughly twice as expensive as less critical tools used for non-critical layers.

While new structures and issues (such as 3D transistors, or high-aspect-ratio requirements of 3D NAND) are likely to increase Etch complexity, the increase in spending on Etch from multiple patterning will likely be temporary. With the introduction of EUV, Etch-related spending comes back down materially. Lithography costs remain high (EUV machine is twice as expensive as ArFi), and Metrology/Process control tools at sub-20nm will also cost more and hence support spending levels (see Exhibit 79).

Exhibit 75 Lithography Costs Increase by ~90% from 30nm to 20nm

	Lithography		
	32nm	22nm	Δ
# of layers	**37**	**40**	8%
- Non Critical Layers	23	21	-9%
- Critical Layers	14	19	36%
# of Cycles/passes	**38**	**52**	37%
- Non Critical Layers	23	21	-9%
- Critical Layers	15	31	107%
Cost per cycle (indexed)			
- Non Critical Layers	100	90	-10%
- Critical Layers	400	450	13%
Total cost (indexed)	8,300	15,840	~91%
- Non Critical Layers	2,300	1,890	
- Critical Layers	6,000	13,950	

Source: Bernstein estimates and analysis.

Exhibit 76 Metrology/Process Control Costs Increase by ~70% from 30nm to 20nm

	Process Control		
	32nm	22nm	Δ
# of layers	**37**	**40**	8%
- Non Critical Layers	23	21	-9%
- Critical Layers	14	19	36%
# of Cycles/passes	**56**	**89**	59%
- Non Critical Layers	35	32	-9%
- Critical Layers	21	57	171%
Cost per cycle (indexed)			
- Non Critical Layers	100	90	-10%
- Critical Layers	150	150	0%
Total cost (indexed)	6,600	11,385	~73%
- Non Critical Layers	3,450	2,835	
- Critical Layers	3,150	8,550	

Source: Bernstein estimates and analysis.

Exhibit 77 Etch Costs Increase by ~20% from 30nm to 20nm

	Etch, Clean, Planarization		
	32nm	22nm	Δ
# of layers	**37**	**40**	8%
- Non Critical Layers	23	21	-9%
- Critical Layers	14	19	36%
# of Cycles/passes	**38**	**52**	37%
- Non Critical Layers	23	21	-9%
- Critical Layers	15	31	107%
Cost per cycle (indexed)			
- Non Critical Layers	100	90	-10%
- Critical Layers	100	90	-10%
Total cost (indexed)	3,800	4,680	~23%
- Non Critical Layers	2,300	1,890	
- Critical Layers	1,500	2,790	

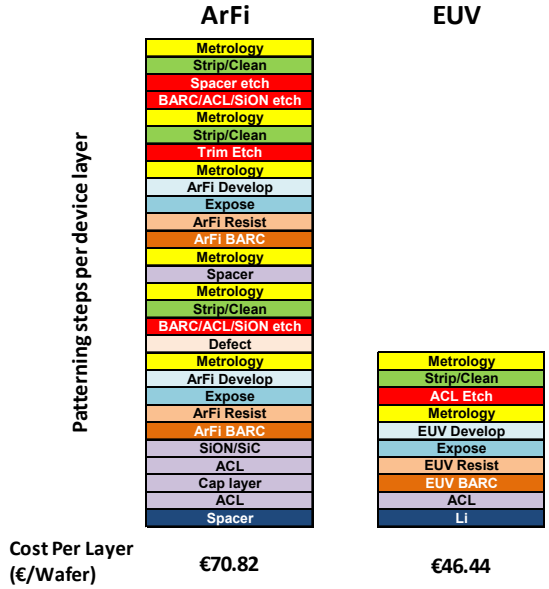
Source: Bernstein estimates and analysis.

Exhibit 78 In the 30 to 20nm Migration, We Estimate the >50% Cost Increase in Equipment Is Mostly Driven by Lithography, Then Metrology and Process Control

	Lithography			Process Control			Etch, Clean, Planarization		
	Δ 32 -> 22nm	% split, 32nm	Cost Impact 32 -> 22nm	Δ 32 -> 22nm	% split, 32nm	Cost Impact 32 -> 22nm	Δ 32 -> 22nm	% split, 32nm	Cost Impact 32 -> 22nm
# of layers									
- Non Critical Layers	-9%	62%	-5%	-9%	62%	-5%	-9%	62%	-5%
- Critical Layers	36%	38%	14%	36%	38%	14%	36%	38%	14%
# of Cycles/passes									
- Non Critical Layers	-9%	61%	-5%	-9%	62%	-5%	-9%	61%	-5%
- Critical Layers	107%	39%	42%	171%	38%	65%	107%	39%	42%
Total cost (indexed)									
- Non Critical Layers	-18%	28%	-5%	-18%	52%	-9%	-18%	61%	-11%
- Critical Layers	133%	72%	96%	171%	48%	82%	86%	39%	34%
		100%	91%		100%	73%		100%	23%
Market Size 2012 ($M)			**6,979**			**3,854**			**7,835**
Weighted average increase			**~60%**						

Source: Bernstein estimates and analysis.

Exhibit 79 **With the Introduction of EUV, Lithography Costs Will Remain High and Metrology/Process Control to Some Extent as Well, But Etch Will Come Back Down Materially – Arfi Spacer -> EUV Simple Layer Illustration**



Spacer->EUV (per layer metrics)	Lithography Δ	Etch Δ	Metrology Δ
# of passes/cycles	-50%	-83%	-67%
Est. Tool Cost	172%	0%	57%
Total Cost	36%	-83%	-48%
Change in Total Costs	-34%		
-o/w Litho	36%		
-o/w non-Litho	-69%		

Note: Spacer based Multiple Patterning to Single Patterning EUV is the most deflationary transition. We expect other transitions (LELE->EUV SP) to be comparatively less deflationary, although directionally identical: increased share of Lithography, significant decrease in Etch, more stable evolution of Metrology.

Source: ASML and Bernstein estimates and analysis.

In addition, we see Wafer-level packaging as a long-term winner as well, for more idiosyncratic reasons: We expect strong growth in Advanced Packaging, TSV, Bump Processing as we believe these techniques will develop as a way to compensate for the higher cost of shrink and shrink limitations specific to Memory. As this is a small segment (<5%) of semi-cap spending, we will not get into a detailed discussion.

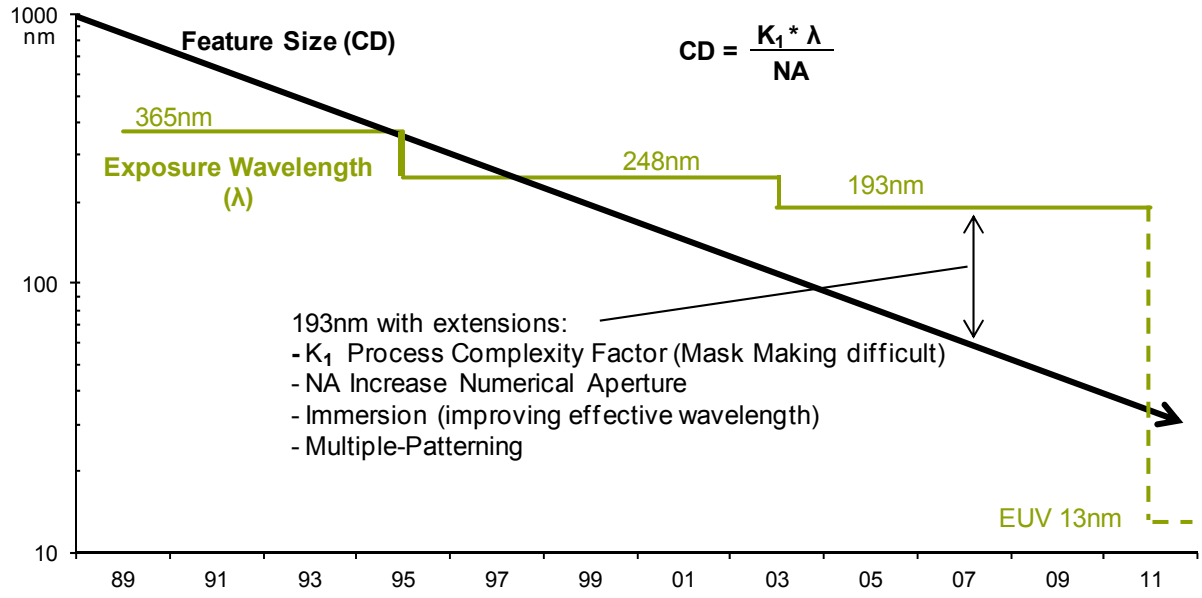
Lastly, we recognize that these main lines of evolution are mostly relevant for Logic manufacturing. In Memory, the perspective is different and will be more widely described in "The Memory Paradigm — Why Scaling Limitations Are Good for Memory Suppliers" chapter in this *Blackbook.* For capital goods, the introduction of 3D structure will have a more widely beneficial impact on equipment manufacturers, multiplying all steps of the process and keeping Lithography and Metrology/Wafer inspection at relatively high levels of resolution.

Lithography: Moore's Law's Most Challenging Bottleneck

Lithography Is the Bottleneck for Shrink, and Will Represent Increasing Share of Capex Going Forward

Lithography is the bottleneck of continued improvement in semiconductor manufacturing. ArF immersion is reaching its physical limits, resulting in increased technological complexity going forward. As the industry goes toward more and more advanced process nodes, physical barriers increase the complexity of Lithography in a step function. Existing leading edge Lithography tools (ArF-immersion) are limited by the wavelength of their light source (193 nm) (see Exhibit 80).

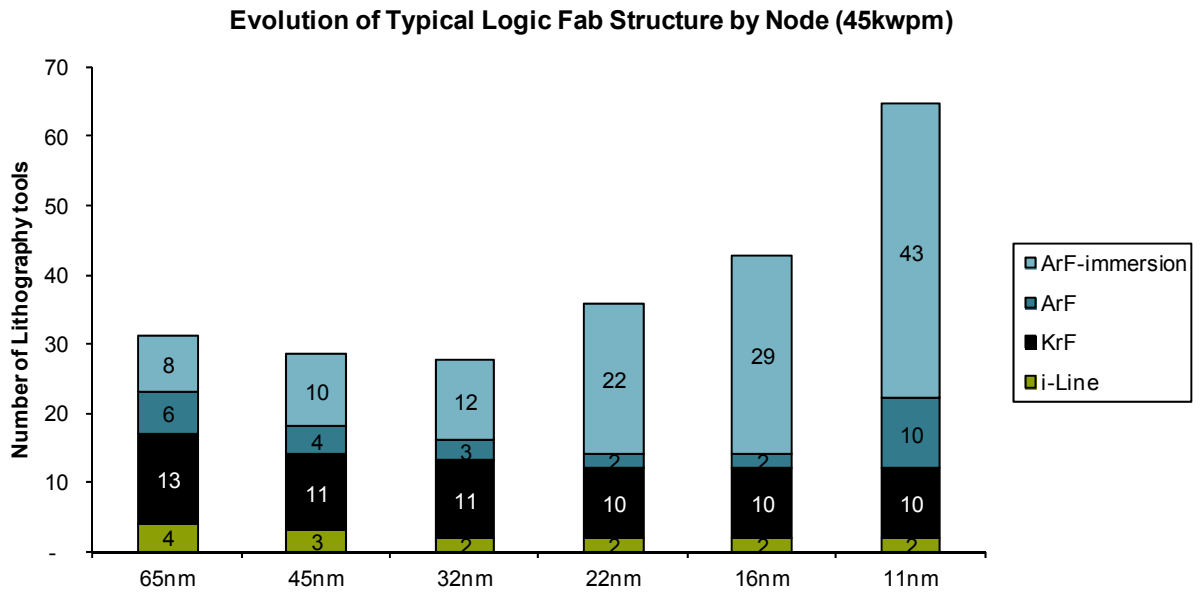
Exhibit 80 **Lithography Is Hitting a Roadblock; Shrinking the Node Now Requires Increasing Process Complexity**



Source: Intel and Bernstein analysis.

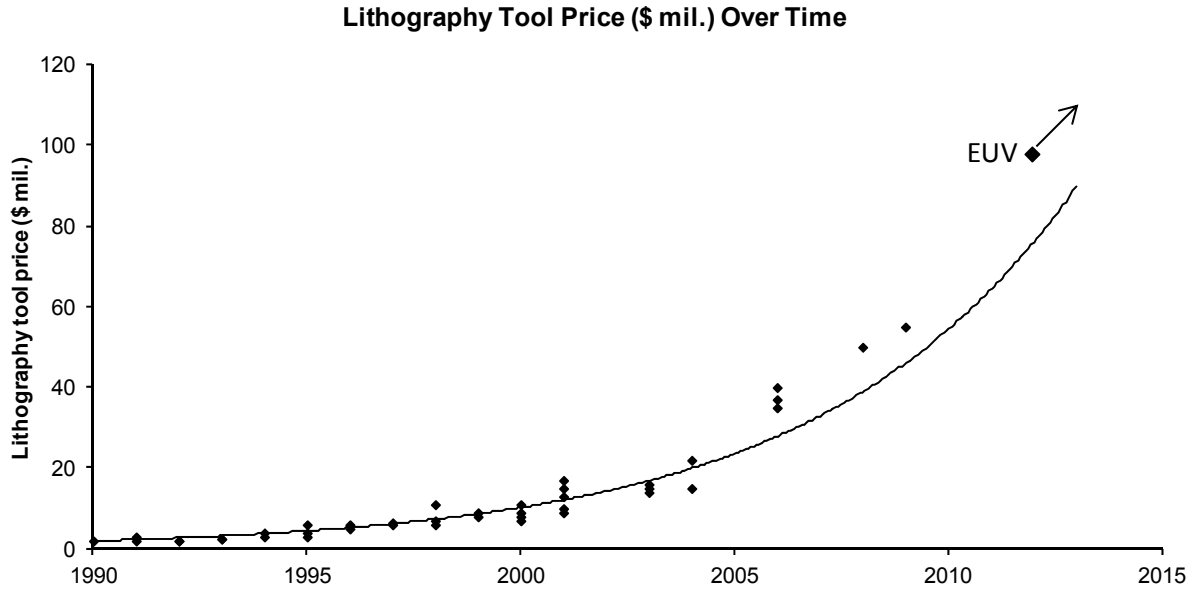
This has meant that Lithography has been increasing as a share of semi capital equipment spending, and at an accelerated pace, over the last 10 years. This trend is driven by the increasing cost of systems involved (KrF->ArF, ArF ->ArFi) and this is set to accelerate further with the introduction of multiple patterning and EUV (see Exhibit 81 and Exhibit 82).

Exhibit 81 **With Double Patterning, the Number of ArF-Immersion Tools Increases Exponentially (Logic Example)**



Source: Bernstein estimates and analysis.

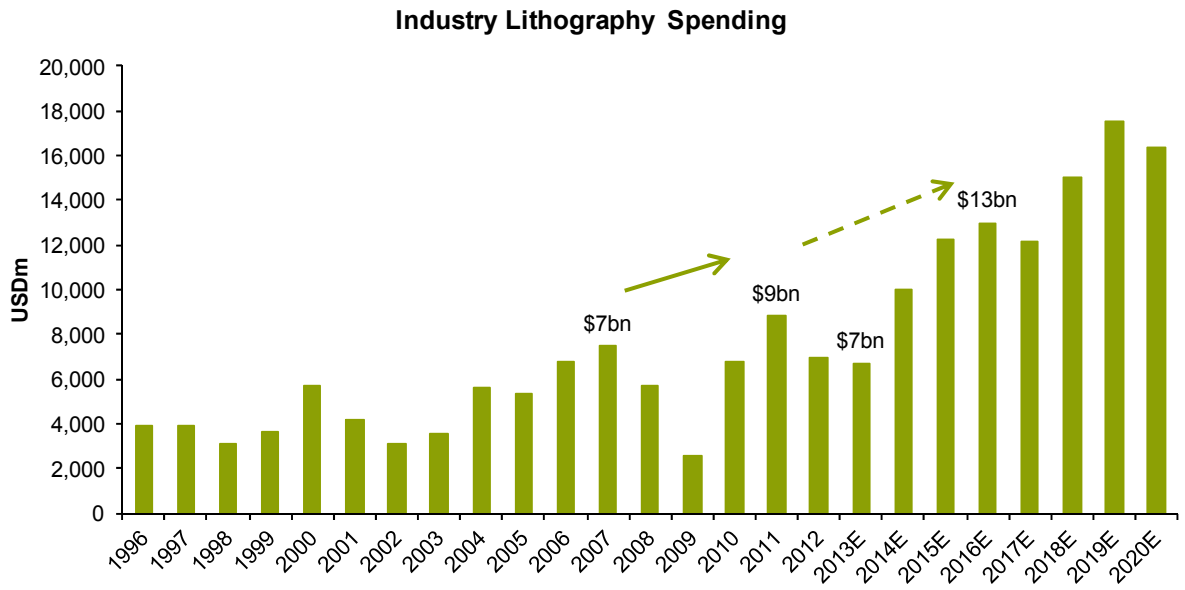
Exhibit 82 **More Advanced Lithography Requires More Expensive Lithography Tools; EUV Tools Come at a Significantly Higher Cost**



Source: Intel and Bernstein analysis.

Our analysis suggests 2013 is actually a trough year for the industry, despite a level of sales likely to end in the same ballpark as 2012. Going forward, the combined effect of multiple patterning and EUV is likely to take Lithography sales to new levels: Lithography revenues moved in the last cycle from $7 billion to $9 billion per year, with a trough at $3 billion, the next one is likely to move between $9 billion and a next peak at $13 billion in 2017, and a trough in the $7 billion region (see Exhibit 83).

Exhibit 83 **Going Forward, the Combined Effect of Multiple Patterning and EUV Is Likely to Take Lithography Sales to New Levels**



Source: Gartner and Bernstein estimates and analysis.

ASML Is Set to Fully Benefit from the Trend

ASML is set to fully benefit from the trend, with no competitor left in the field. Today, ASML already has virtually no competition in the leading edge. We estimate its market share in ArFi over 85% in 2012, and likely 100% in the world excluding Japan and Intel (see Exhibit 84).

Exhibit 84 **We Estimate ASML Had Over 85% Share of the ArFi Lithography Market**

Estimated ASML Market Share in ArFi litho			
Market Units	90	Gartner 4Q12 report	
ASML Units	72	ASML Reported	
Other Units	18		
ASML ASP (€m)	40	ASML Premium (SCBe) =	1.5x
Competitior ASP (€m)	27		
ASML ArFi Market Share	86%		

Source: Bernstein estimates and analysis.

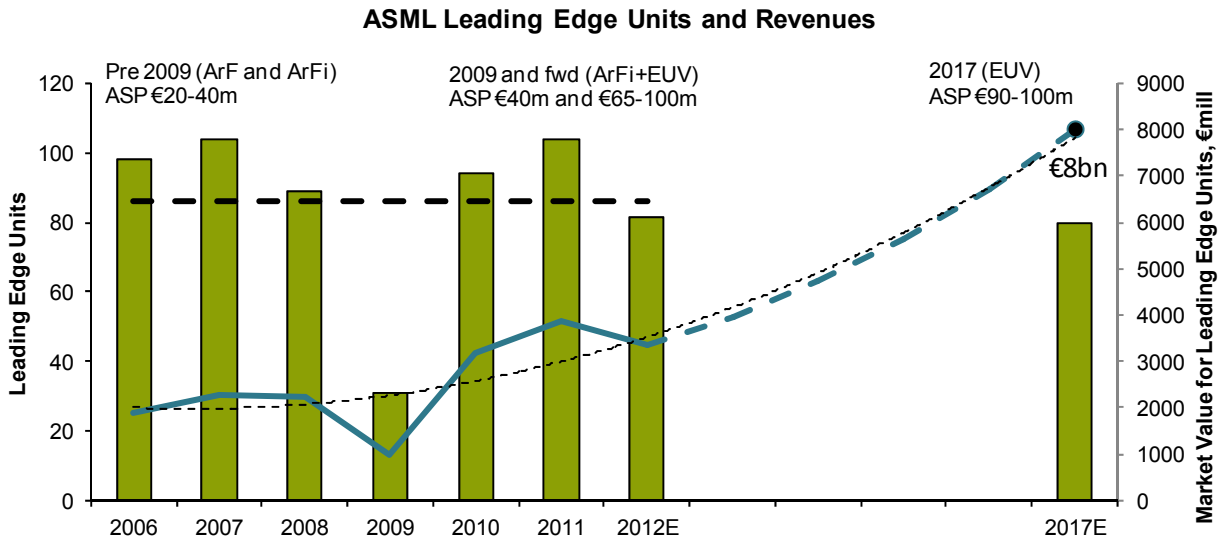
With EUV, ASML's domination goes a step further as we believe there is no competing project for the technology. We believe the company has the potential to more than triple earnings over the next five years (see Exhibit 85 and Exhibit 86).

Exhibit 85 ASML Has a clear Leadership in EUV Development

ASML	Nikon
- Working on 15 improvement projects, including optics, source power and debris management - Expects to reach stability in source power this year - Expected update on E.U.V. roadmap by Sept	- Considers ArFi double patterning as a viable candidate for 16nm, and will focus its development efforts in this area. - Limited focus on E.U.V. - Sees E.U.V. as another candidate, but for the time being, focused on development of the optical systems for the technology
- Already achieving 5-7wph in production machines	
- 4 machines shipped to customers (revenues recognized)	- Expects E.U.V. in volume in 2018-19
- Expect to reach 40wph on E.U.V. by year end, 70wph in 2013, and 125 in 2014.	
- Expect large-scale E.U.V. adoption in 2015	
wph: Wafers per hour	

Source: ASML conference call transcripts, Nikon annual report and Bernstein analysis.

Exhibit 86 ASML's Revenues Should Reach €10 Billion by 2017/18 Based on Shipping ~80 EUV Machines

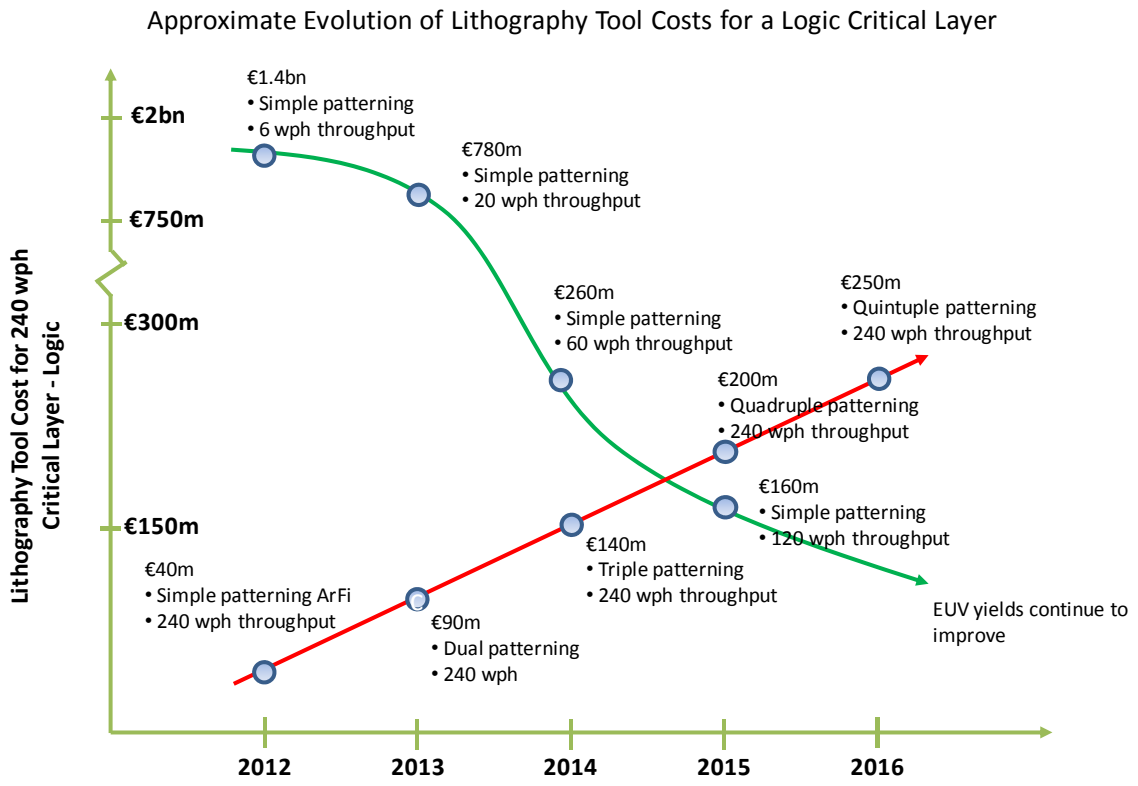


Source: Strategy Analytics and Bernstein estimates and analysis.

The Only Risk to Our Thesis Lies in the Development of EUV Technology, But With Little Impact to ASML's Financial Performance

We nevertheless consider it a limited downside to the recent stock price: ASML has already reached throughput levels (over 40 wafers per hour) that are in the ballpark of what is required for EUV to be economically viable at least for the one or two most critical layers of 10nm logic chips (see Exhibit 87).

Exhibit 87 EUV Is Technically Viable Today and Will Become Fully Viable Economically by 2015



Source: Corporate reports and Bernstein estimates and analysis.

Delays in the technology could still occur, but would have limited impact on ASML's financial performance, as a slower introduction of EUV would mean a longer life expectancy for intensive multiple patterning. A scenario in which EUV would never become viable is highly unlikely. It would have severe impact on the industry, likely stopping shrink at the 10nm or 7nm node, but would still lead to a level of earnings power for ASML that would still justify the recent stock price (see Exhibit 88).

Exhibit 88 **A Scenario in Which EUV Would Never Become Viable Is Highly Unlikely, But Would Still Lead to a Level of Earnings Power for ASML That Would Still Justify the Recent Stock Price**

	2010	2015 High Volume	
	ArFi Only Patterning	ArFi Only Patterning	ArFi + EUV Patterning
Exposures to form Grating	1	1	1
Exposures to form Pattern	1	4	1
Total Exposures	2x	5x	2x
Per Unit Capacity			
Number of typical ArFi machines per unit capacity	1	1	1
Number of typical ArFi or EUV machines	1	4	2
Cost of a typical ArFi Machine for Grating	€34M	€45M	€45M
Cost of a typical ArFi/EUV Machines for Pattern	€34M	€45M	€80M
Equipment Cost to make a Full Pattern	€68M	€225M	€205M
Increase in Lithography Cost		231%	201%

* Assuming the productivity of EUV machines reaches 50% of ArFi in 2015.

Source: Intel and Bernstein estimates and analysis.

Metrology and Process Control: The Other Winners

As Feature Size Shrinks and Complex 3D Transistor Designs Are Introduced, Metrology Spending Grows

As feature size shrinks and complex 3D transistor design are introduced, Metrology requirements increase, increasing the size of the market, through a combination of higher ASP tools and more tools required.

At lower feature sizes, Defect Inspection and Review suffer from low sensitivity and/or inadequate throughput. Defect contrast signal decays aggressively beyond the 22nm node and requires more Process Control (see Exhibit 89). Although technologies like e-beam exist that can detect small defects, the throughput of these tools keeps them limited to R&D labs and for offline use.

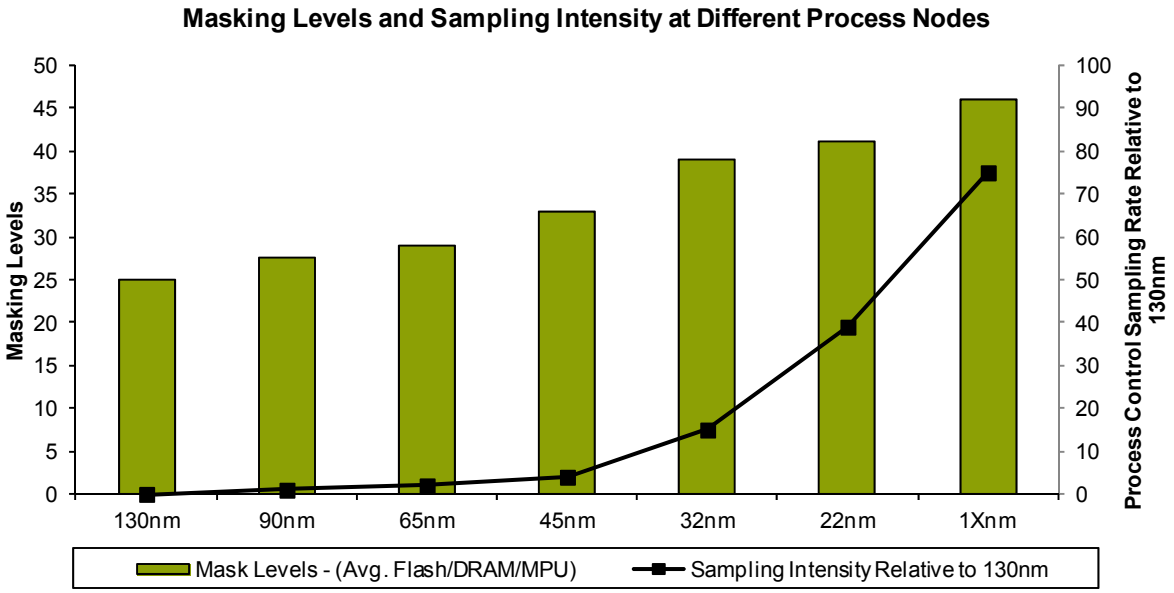
Multiple patterning, the only option to continue to shrink feature size while EUV technology becomes production worthy, requires several times more Metrology. For example, there are three Metrology steps used in a LELE double patterning scheme and seven Metrology steps used in a triple patterning (Double Spacer) scheme (see Exhibit 90). The driver for this increased usage is, of course, the accuracy needed for the overlay as multiple layers are stacked one on top of another.

With FinFETs, the entire 3D structure becomes critical for Process Control, including fin and gate dimensions, profiles and roughness, metal gate undercuts. Similarly, 3D memory includes multiple gate level structures defined by high aspect ratio (HAR) trenches and holes in multilayer stacks. There are major gaps here with in-line, non-destructive metrology with required sensitivity and resolution to image or measure CD, depth, profile, or contamination of such HAR features.

Finally, EUV will bring more complexity to Mask Inspection and Metrology. All potential solutions have a high level of risk involved and are far from ready (see Exhibit 91).

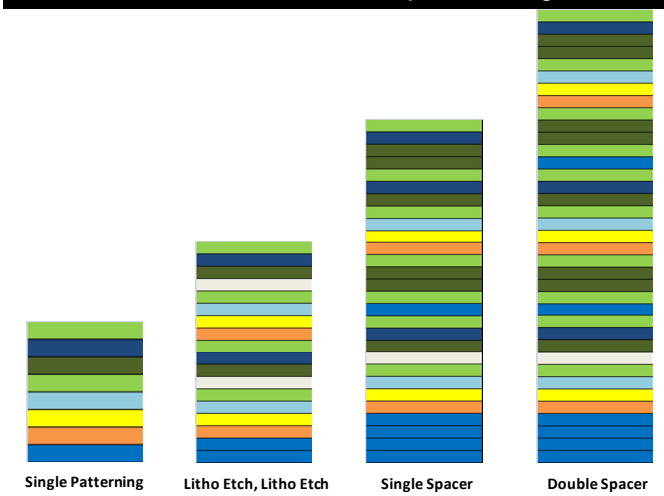
New technology capable of detecting defects or measuring dimensions at lower nodes is ~20-30% more expensive and the above mentioned technological difficulty translates into an increased sampling rate, which means more tools are needed to get the same sampling throughput (see Exhibit 92).

Exhibit 89 **Defect Contrast Signal Decays Aggressively Beyond the 22nm Node and Requires More Process Control**



Source: Nanometrics and Bernstein analysis.

Exhibit 90 **Multiple Patterning Increases the Need for Process Control Several Times**



	Single Patterning	Litho Etch, Litho Etch	Single Spacer	Double Spacer
Strip/clean	1x	2x	3x	3x
Etch	1x	2x	6x	8x
Defect inspection	1x	2x	1x	1x
Metrology	2x	4x	7x	10x
Develop	1x	2x	2x	3x
Expose	1x	2x	2x	3x
Coat	1x	2x	2x	3x
CVD	1x	2x	5x	6x

Source: ASML and Bernstein analysis. (See online version for colors.)

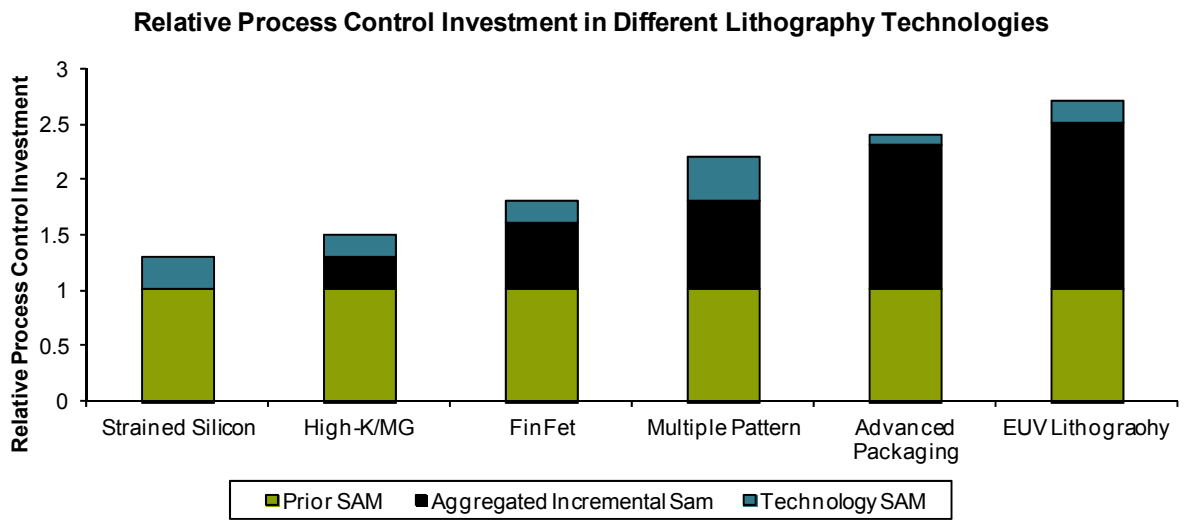
Exhibit 91 **EUV Lithography Will Bring a Lot More Complexity in the Mask Making, Inspection and Metrology; There Are Several Candidate Technologies to Address the Challenges**

		Optical Extension	EUV	Nanoimprint	Maskless Lithography
Patterning & Mask Production	Mask materials	Optimization and Standardization	Very complex substrate stacks	Standard Qz substrate	No mask used
	Data Prep	Very complex data with SMO/ILT/DPL	Minimum data prep for flare correction	No OPC needed	Compatibility with Optical litho
	Pattern Generation	Massive shot counts/writing time	Flat data exposure needed	1x resolution	1x resolution and Throughput
	Processes	CD and defect control	Damage free process/Cleaning	Defect control	Compatibility with Optical litho
	Inspection & Metrology	Very complex feature and spec.	Actinic inspection & metrology	Inspection and repair	Resolution & Data base inspection
Lithography	Throughput	Multiple exposure	Source, resist, mask life	Step & repeat time	Massive parallel beams needed
	Mask cost	Multiple complex masks needed	High substrate and QA cost	Replication usable	No mask used
	Readiness	Ready now	Pilot in 2011?	Tool/Feasibility needed	Tool availability

Note: Slide presented in BACUS in July 2011. (For colors see online version.)

Source: SPIE and Bernstein analysis.

Exhibit 92 **All of the Above Technology Inflexions Lead to Process Control Getting More Complex and More Expensive**



Source: Nanometrics and Bernstein analysis.

The Introduction of New Technologies Also Creates Potential Market Share Shifts

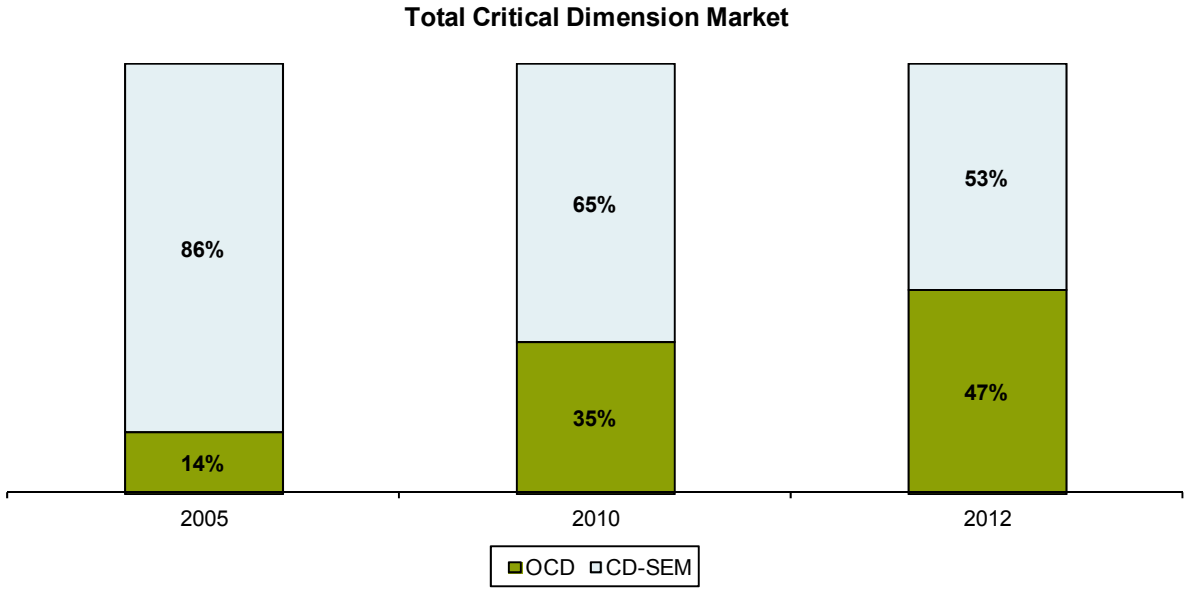
The introduction of new technologies also creates potential market share shifts. For instance, OCD Metrology gained share on CD-SEM Metrology with the introduction of 3D transistors (see Exhibit 93), to the benefit of Nanometrics. OCD is technically superior to CD-SEM as it can do 3D metrology and measures more

parameters at similar high throughput (see Exhibit 94). At lower nodes, CD-SEM may still be tuned but at the cost of potentially destroying the features. Hitachi-High Tech is the industry incumbent in CD-SEM. In 2009, as Intel prepared to roll out tri-gate transistors (3D) at 22nm node, Nanometrics won the company's business. Today, Nanometrics has a 50% market share in OCD. Although KLA-Tencor also makes OCD tools, we believe Nanometrics' proprietary software is likely more advanced.

Another example is the balance between e-beam and optical wafer inspection that could evolve with the introduction of smaller feature size and EUV. With KLA-Tencor controlling ~80% of optical wafer inspection and Hermes Microvision ~85% of e-beam inspection, this could turn into significant share shifts (see Exhibit 95). In terms of resolution, electrical defect, sensitivity, e-beam inspection is superior to optical inspection. However, this comes at the cost of throughput and we therefore find it difficult to call what the balance will be between the two technologies. We believe Optical tools will remain the standard for online Metrology and e-beam will grow in offline uses, for deeper inspection of wafer samples. EUV mask inspection will also likely be an opportunity for e-beam.

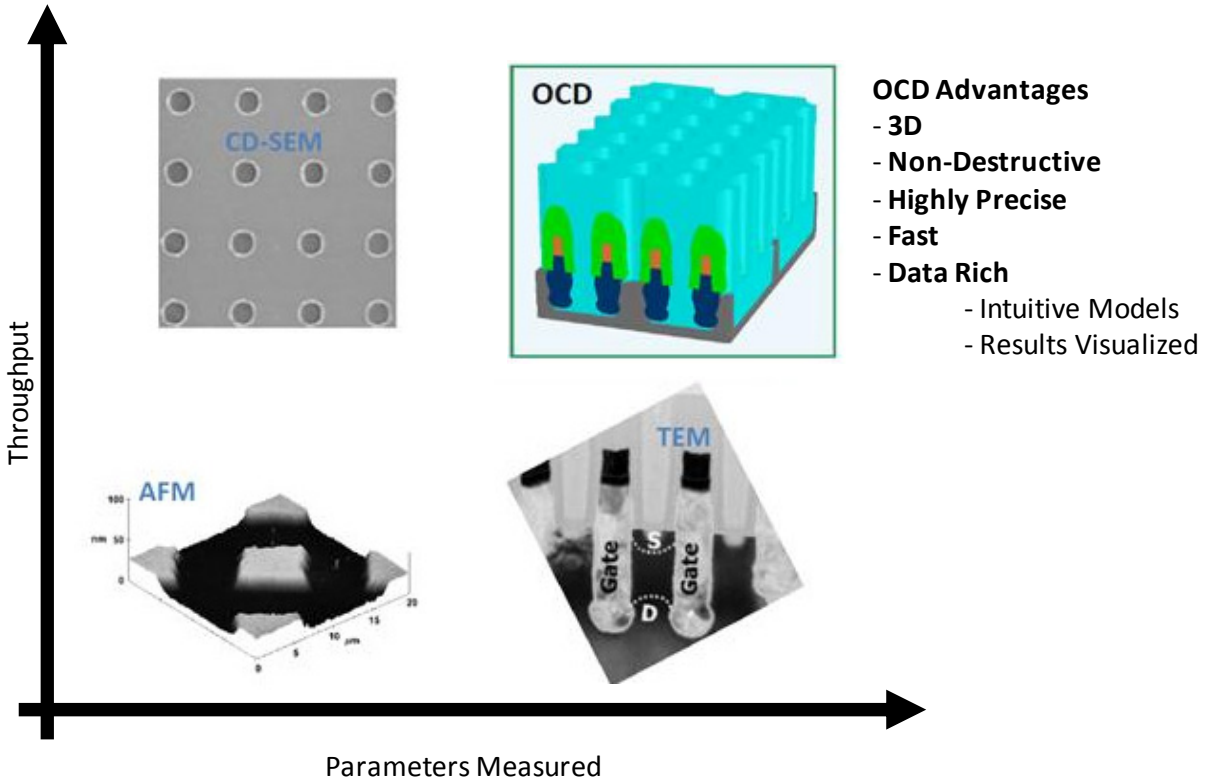
Lastly, we see a significant portion of growth in Metrology driven by Lithography overlay, with the introduction of multiple patterning and more generally smaller critical dimensions. We see here a material chance for ASML taking some share of spending, with its integrated "holistic Lithography" offer, combining Metrology and Lithography tools.

Exhibit 93 **Over the Past Three Years, OCD Has Grown to Almost Half of the Critical Dimension (CD) Metrology Market**



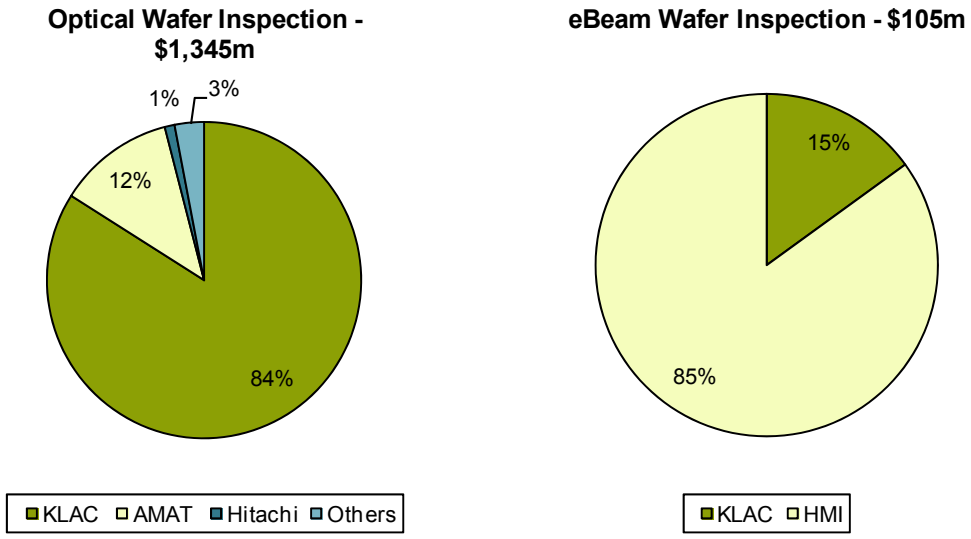
Source: Gartner, VLSI and Nanometrics.

Exhibit 94 **OCD Is Particularly Suitable for 3D Metrology, Replacing CD-SEM, Which Can Only Read in 2D**



Source: Nanometrics and Bernstein analysis.

Exhibit 95 **While KLA-Tencor Dominates Optical Wafer Inspection, Hermes Microvision Dominates E-Beam Inspection Market**



Source: Gartner and Bernstein analysis.

Other Manufacturing Steps: Less Wafer Starts Is a Problem

In most other manufacturing steps, we actually see challenging times ahead, as we believe their primary economic driver is the number of wafers produced, whose growth we see abating under the combined effect of the growing cost per wafer and the migration to 450mm fabs.

We do not want to discount the significant engineering challenges that other process steps (Deposition, Etch, Clean, CMP, RTP, etc) are continuing to face in ensuring the long-term viability of semiconductor manufacturing. We outline a few of the challenges facing these steps below.

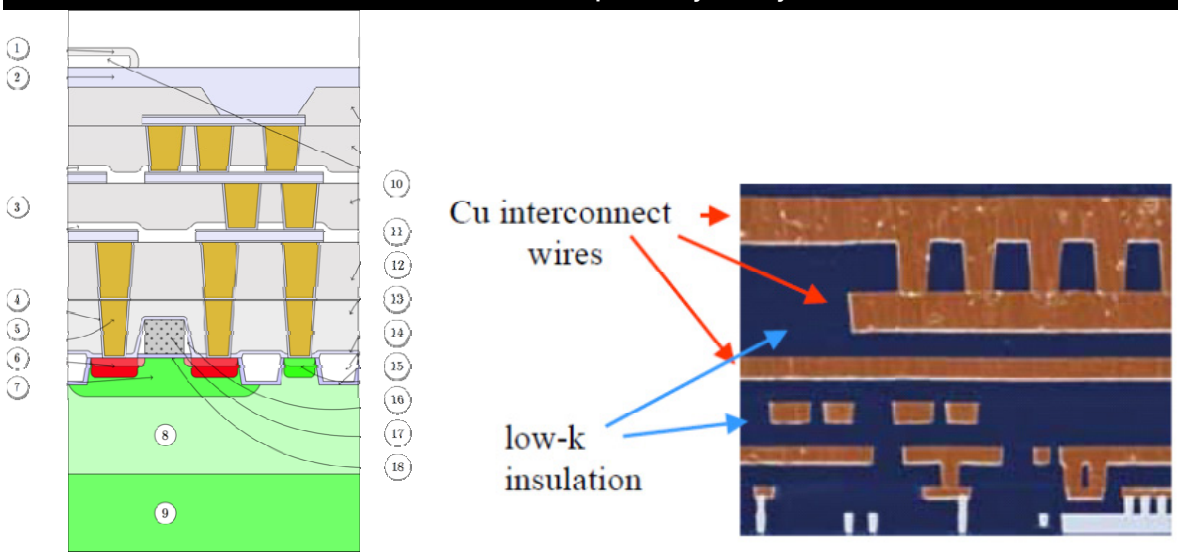
Deposition (PVD, CVD, ALD, ECD)

Deposition (selective formation of materials in a thin film on the wafer surface) has several mechanisms and applications in semiconductor manufacturing. PVD ("physical vapor deposition," also know as sputtering) is used to deposit metals and other non-reactive films (argon ions strike a target made of the film to be deposited, knocking off atoms that attach themselves to the wafer, useful for Cu seed layers). CVD ("chemical vapor deposition") uses chemically reactive gases that react with each other and the wafer surface to grow a thin film. A variation is PECVD ("plasma-enhanced chemical vapor deposition) which uses a plasma to break apart a precursor gas into reactive components that form the deposited film (often used for low-k dielectrics). ALD ("atomic layer deposition") deposits a film one atomic layer at a time (useful to deposit very thin high-k oxides, and sometimes thin barrier layers). And ECD ("electrochemical deposition") is used to plate the copper that forms the metal wires (interconnects) on an integrated circuit.

The industry is wrestling with the need to deposit films with new chemistries, thermal responses, and mechanical properties. On the front end (transistor fabrication), developing and depositing new high-k dielectric materials with manufacture-capable thermal properties is becoming a huge issue as the equivalent oxide thickness (EOT) of these layers approaches 0.7 nm.

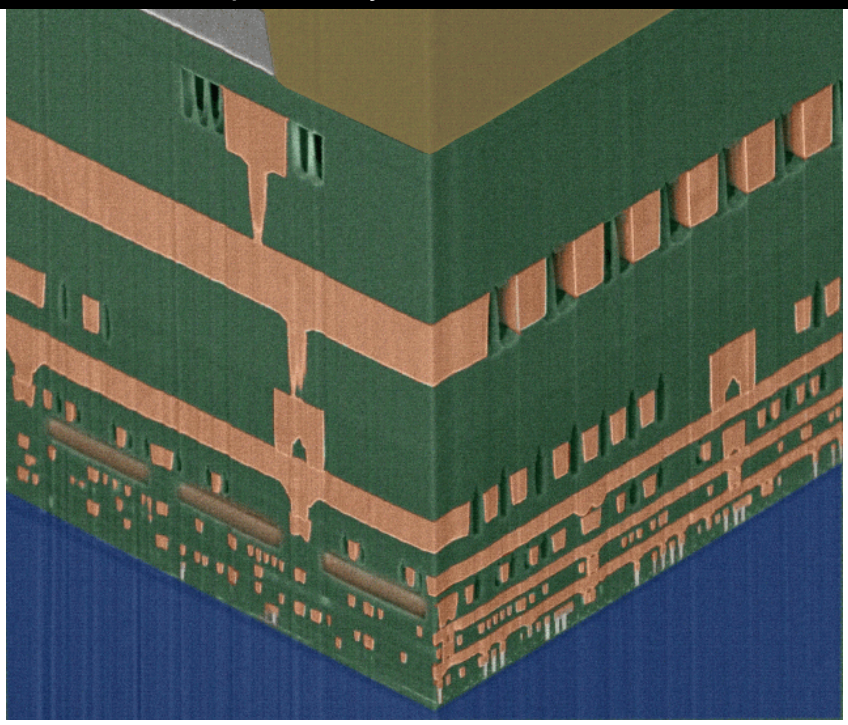
On the back end, the industry has already made the move to depositing low-k dielectric materials, rather than silicon dioxide, for insulating between metal wiring (lower dielectric constants lower the delay associated with the circuits) (see Exhibit 96). As "nothing" has the lowest dielectric constant available porous materials have increasingly found use, but come with new difficulties including roughening, unwanted diffusion of reactants into the pore structure, and poor mechanical structure. "Air-gaps" (taking the concept of porous materials to the ultimate conclusion) are now being considered as well, with associated issues in selectively building up the structures in a uniform and mechanically sound way (see Exhibit 97).

Exhibit 96 **Metal Interconnects Separated by Interlayer Dielectric Materials**



Source: Wikimedia Commons.

Exhibit 97 **"Air Gaps" as Interlayer Dielectrics**



Source: IBM.

Etch[2]

Etching involves selective removal of materials, typically through the use of a plasma process, and is a critical step in forming the structures that make up both the transistors themselves, and the morass of wiring (interconnects) that connect them together.

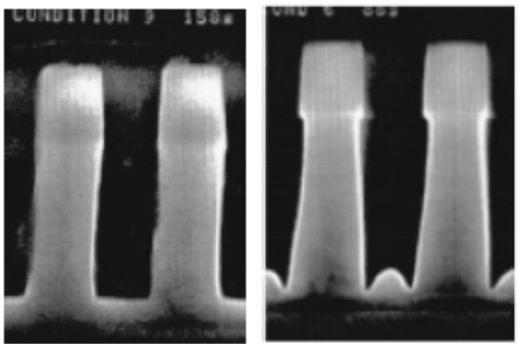
[2] For those who might be interested (or are simply masochistic) a detailed discussion of semiconductor etching challenges can be found in the Ph.D. thesis of one of the authors, located at: http://dspace.mit.edu/bitstream/handle/1721.1/28843/60386212.pdf?sequence=1.

As structures get more complex, and material and electrical requirements more challenging, etch is facing a variety of issues.

Maintaining proper uniformity of etched features becomes increasingly difficult. Features that are different sizes etch at different rates (smaller features can tend to etch slower, known as RIE lag, or aspect-ratio dependent etching); and patterns in low-density portions of the wafer can etch faster than in high-density areas (known as microloading).

Ideal Etch profiles have straight, smooth sidewalls. Maintaining profile control is an increasing issue as feature sizes shrink (issues with taper, bowing, and microtrenching artifacts become much more pronounced) (see Exhibit 98). New tri-gate and 3D structures are also making profile control increasingly important.

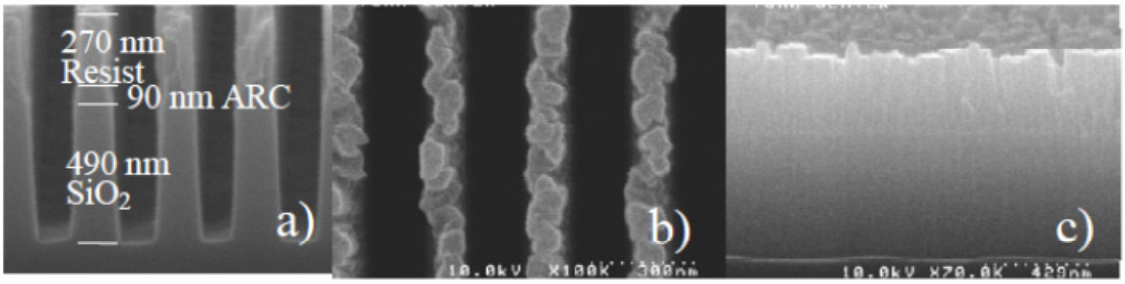
Exhibit 98 **Examples of Straight Etch Profiles, and Profiles With Artifacts (Taper, Bowing, and Microtrenching)**



Source: Stacy Rasgon.

Roughness on feature sidewalls is a huge issue, as it creates variation in transistor critical dimensions (essentially resulting in transistors with varying sizes along their length) as well as interfering with the deposition of materials inside the features without leaving voids (see Exhibit 99).

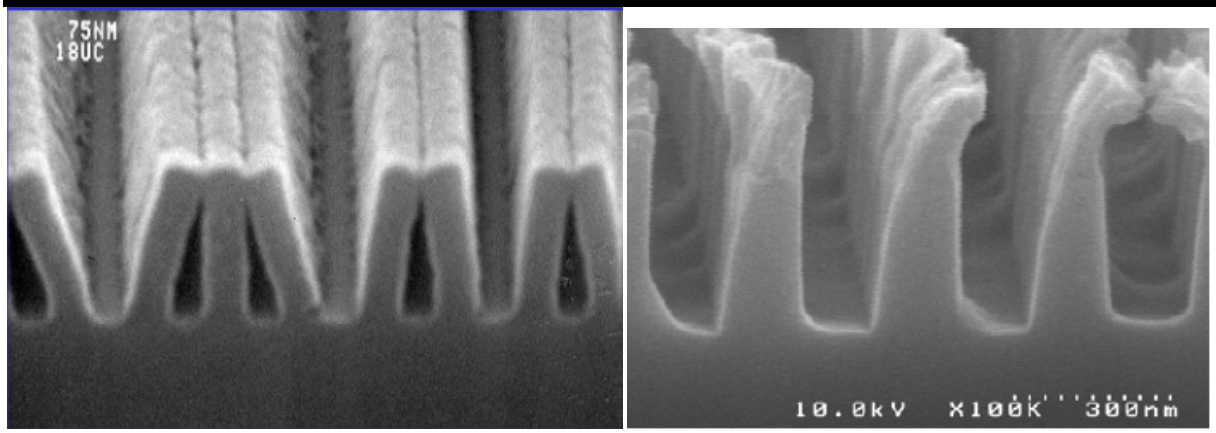
Exhibit 99 **Example of Sidewall Roughening and Striation After Etching (Cross-Sectional, Top-Down, and Sidewall Views)**



Source: Stacy Rasgon.

Interaction with the photoresist (which acts as a protective layer preventing etching of the covered surface) becomes increasingly difficult as feature sizes shrink. Making smaller, thinner features requires a thinner photoresist coating, with pattern collapse a huge issue otherwise. However, thinner resists also means less material present to protect the underlying surface, thus requiring a higher resistance to etching (e.g., a higher etch selectivity vs. the underlying etched layer) (see Exhibit 100).

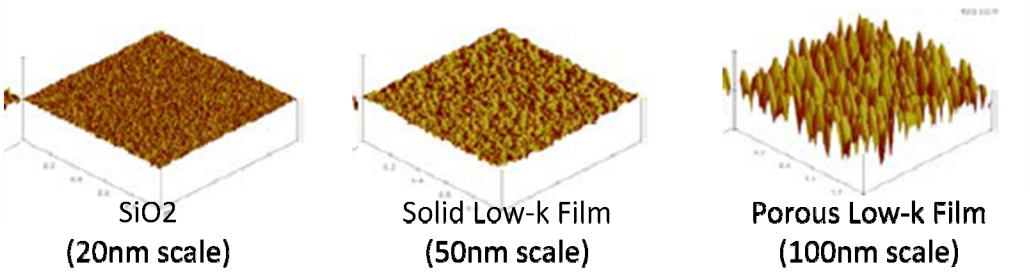
Exhibit 100 **Examples of Photoresist Collapse (Printed Lines Too Tall and Thin) and Twisting (During Etch) Due to Inadequate Selectivity**



Source: Stacy Rasgon.

Etching of low-k dielectrics is also challenging. Typical removal of resist residue has used an oxygen plasma, which tends to strip out the low-k components ("low-k damage") and requiring development of new stripping processes with lower damage rates. Additionally, porous low-k materials have their own sets of issues, including diffusion of etchants and polymers into the pore structure (see Exhibit 101).

Exhibit 101 **Roughening of Porous Low-K Films Due to Etching in a Polymerizing Plasma**



Source: Stacy Rasgon.

CMP (Chemical Mechanical Polishing) or "Planarization"

Older process technology utilized aluminium wiring on chips, which could be easily patterned and etched. However, increases in current density led to "electromigration" (essentially holes opened up in aluminium wires due to the "force" of the current driving through it) necessitating a replacement with copper (also conveniently of a lower resistivity, useful for lowering circuit delay). However, copper cannot be etched (it forms no volatile products), necessitating a new removal mechanism. Enter chemical mechanical polishing, where a combination of a chemically reactive slurry and mechanical agitation (using a brush or pad) removes the material and "planarizes" the surface.

Given new materials, CMP slurries are increasingly requiring selection or tuning of the chemistry and abrasive particles to meet the material at hand. Use on less mechanically stable films (e.g., porous, or even air gaps) is highly challenging. And, as layers get thinner, end-point detection is becoming increasingly difficult, e.g., knowing when to stop.

Cleaning

Almost every step in semiconductor manufacturing requires cleaning to remove residues, contaminants, and anything that could serve as a "killer" particle. Today wet cleans using a variety of aqueous chemicals are used.

Given that the size of "killer" particles is now approaching levels where they cannot be detected, the importance of robust cleaning processes is increasingly critical. Additionally, as layers become thinner, cleaning without roughening or damaging the surface, as well as ensuring there is no incremental material removal during the clean, are huge issues.

The industry is loath to move away from wet cleans; however, new methodologies currently under investigation include megasonics, cryogenic aerosol (or CO2 "Snow Gun"), and dilution of solvents, as well as more esoteric methods like lasers and electrostatics.

Overall, While Chemistries and Mechanisms May Be Changing, the Basic Nature of Many of These Processes Remains Relatively Stable

We do not believe that these processes are going through technological shifts materially changing the trajectory of equipment costs and number of equipments required.

Some process steps (Etch, Deposition, etc.) do benefit from the ongoing development of multiple patterning, as process steps increase with the number of patterns, but for critical layers only (see Exhibit 90). For instance, examining the setup between 32nm and 22nm Logic, while the number of Etch exposures increases at the same rate as Litho exposures, the tools do not cost exponentially more, resulting in a milder increase in spending for Etch. In the medium term, with the introduction of EUV, these process steps will on the contrary be under pressure, as single EUV exposures will replace multiple patterns (see Exhibit 75 through Exhibit 79 earlier in the chapter).

Similarly, we don't believe that volumes or unit costs of equipments for other processes (RTP/Oxidation, Ion Implantation, Manufacturing Automation, etc.) will shift trajectory going forward. With the coming slowdown in wafer addition, growth in these segments may well come under pressure.

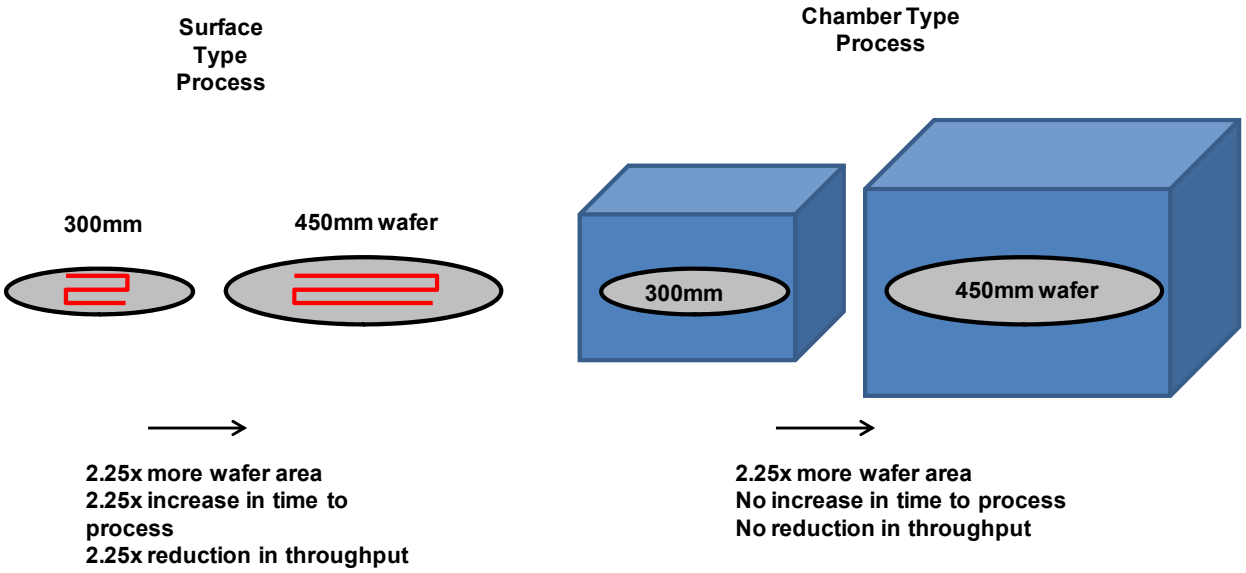
We Believe the Introduction of 450mm Fabs Will Increase the Gap Between Winners and Losers

The introduction of 450mm fabs will, we believe, increase the gap between winners and losers (see Exhibit 102).

Lithography and Process Control are in essence ***"surface"*** steps, in which the surface of the wafer is processed with a limited active surface at a time. In other words, a twice larger wafer requires twice longer processing — or twice more machines to keep a throughput unchanged. As such, the introduction of 450mm wafers will not have any deflationary impact on these steps.

On the contrary, Deposition, RTP/Oxidation, Ion Implantation, Manufacturing Automation, Photo-resist processing, Etch, Clean and Planarization are ***"chamber"*** steps, in which the wafer is processed in one go. In other words, twice larger wafers imply twice fewer tools for the same surface of silicon processed. The development of 450mm wafer fabs will therefore have a deflationary effect on these steps.

Exhibit 102 The Transition from 300mm to 450mm Doesn't Impact "Surface Steps" Such as Lithography as Throughput Reduces Proportionally, But Negatively Impacts "Chamber Steps" Such as Etch and Deposition, as Throughput Is Unchanged



Source: Bernstein estimates and analysis.

Conclusion: How to Play the Theme?

In sum, we expect Lithography and Process Control to grow at a much faster rate than the overall semi-cap market: 8% p.a. and 7% p.a. respectively in the long term, versus 4% p.a. for semi-cap equipment spending. As a reference point, these long-term growth rates in the past have been 4%, 3.6% and 2.1%, respectively. We expect all other process steps to experience only anaemic growth: 1.4% p.a. going forward versus 1.6% p.a. in the past.

In our coverage, **ASML** is a structural winner and remains a top pick.

We do not cover other names in the space but provide in Exhibit 104 through Exhibit 109 screening tools based on the segment exposure of semi-cap manufacturers, the relative attractiveness of these segments with regards to the mourning Moore's Law trend and the competitive intensity of the segment. We also provide a valuation screening of the space and screen it against our attractiveness mapping. These analyses are available on request for investors willing to investigate further related investment opportunities.

- Exhibit 103 shows our relative long-term growth expectation for semi-cap sub-segments and the related attractiveness index we assign to each of them.
- Exhibit 104 shows the concentration index of semi-cap sub-segments and the related attractiveness index we assign to each of them.
- Exhibit 105 maps semi-cap manufacturers against industry sub-segments and segmental market shares.
- Exhibit 106 assigns an attractiveness rating to each company, based the combination of analyses exposed in Exhibit 103 through Exhibit 105.
- Exhibit 107 and Exhibit 108 map this attractiveness quantitative screening against the company's recent valuation (EV/Sales and EV/Ebit).
- Lastly, Exhibit 109 brings together in a single view this screening analysis with in addition a summarized perspective of the market share shifts we see as possible outcomes of the mourning of Moore's Law.

KLA Tencor, Hermes, NuFlare, Rudolph, and Nanometrics are "the winning group" and appear to stand to benefit the most from the mourning of Moore's Law. For most other semi-capital equipment players (**Tokyo Electron**,

Dainippon Screen, Kulicke & Soffa, BE Semiconductor, Hitachi Kokusai Electric, and Mattson Technology, AMAT, LAM research, **Advantest, Teradyne and LTX-Credence)** mourning Moore's Law equates to some secular headwind and we note that these companies trade at a wide range of multiples across several key valuation metrics.

Exhibit 103 **We Rate the Attractiveness of Semi-Cap Sub-Segments in Terms of Growth, Based on Our Analysis of the Mourning of Moore's Law**

Process Sub-Segment	LT Growth Rate	Moore's Law Attractiveness
Lithography	8%	100%
Photoresist processing	1%	11%
Deposition	1%	18%
Etch, Clean and Planarization	1%	11%
Ion Implanter	0%	-1%
RTP and Oxidation/Diffusion	0%	-1%
Process control	7%	86%
Manufacturing Automation and Control	1%	7%
Packaging and Assembling	4%	49%
Test Equipment	-4%	-52%

Source: Bernstein estimates and analysis.

Exhibit 104 **We Rate the Attractiveness of Semi-Cap Sub-Segments in Terms of Competition Intensity**

Process Sub-Segment	Industry Concentration (HHI Index)	Industry Attractiveness
Lithography	66%	100%
Photoresist processing	74%	112%
Deposition	20%	30%
Etch, Clean and Planarization	19%	29%
Ion Implanter	50%	75%
RTP and Oxidation/Diffusion	27%	40%
Process control	33%	50%
Manufacturing Automation and Control	11%	17%
Packaging and Assembling	5%	8%
Test Equipment	33%	49%

Source: Bernstein estimates and analysis.

Exhibit 105 We Map Below Major Capital Equipment Players Against Losing and Wining Segments of the Industry, With Their Revenue Exposures (Lower Left of the Cell) and Their Market Shares (Upper Right of the Cell) by Segment

Share of Revenue \ Market Share	Total Capital Eqpt 100%	Lithography 18%	Photoresist processing 4%	Deposition 16%	Etch, Clean and Planarization 20%	Ion Implanter 3%	RTP and Oxidation / Diffusion 2%	Process control 10%	Manufacturing Automation and Control 3%	Other wafer eqpt 1%	Packaging and Assembling 16%	Test Equipment 6%
ASML Holding NV	14%	100% / 80%										
Applied Materials Inc.	14%			44% / 39%	29% / 20%	13% / 70%	5% / 40%	9% / 12%				
Tokyo Electron Limite	11%		35% / 85%	18% / 12%	42% / 22%		5% / 26%					
KLA-Tencor Corporati	6%							100% / 55%				
Lam Research Corpor	5%			26% / 12%	74% / 27%							
Dainippon Screen	4%		12% / 11%		88% / 18%							
Teradyne	3%											100% / 40%
Nikon	3%	100% / 15%										
Aixtron	2%			100% / 12%								
ASM International	2%						2% / 3%				98% / 15%	
Kulicke & Soffa	2%										100% / 12%	
Disco	2%										100% / 10%	
Hitachi High-Technolo	1%							100% / 12%				
BE Semiconductor	1%										100% / 7%	
SEMES	1%		14% / 3%		86% / 4%							
Tokyo Seimitsu	1%										100% / 5%	
Daifuku	1%								100% / 23%			
Muratec	1%								100% / 23%			
NuFlare Technology	1%	100% / 3%										
Advantest	3%											100% / 46%
LTX-Credence	0%											100% / 6%
Brooks Automation	0%								100% / 11%			
Nanometrics	0%							100% / 4%				
Hitachi Kokusai Electr	0%						100% / 19%					
Rudolph Technologies	0%							100% / 3%				
Nissin Ion Equipment	0%					100% / 9%						
Mattson Technology	0%						100% / 3%					
Veeco	2%			100% / 10%								
Hermes Microvision	0%							100% / 1%				
Others	19%	2% / 2%	0% / 1%	14% / 16%	12% / 10%	3% / 21%	1% / 8%	7% / 13%	7% / 44%	6% / 100%	44% / 52%	3% / 8%

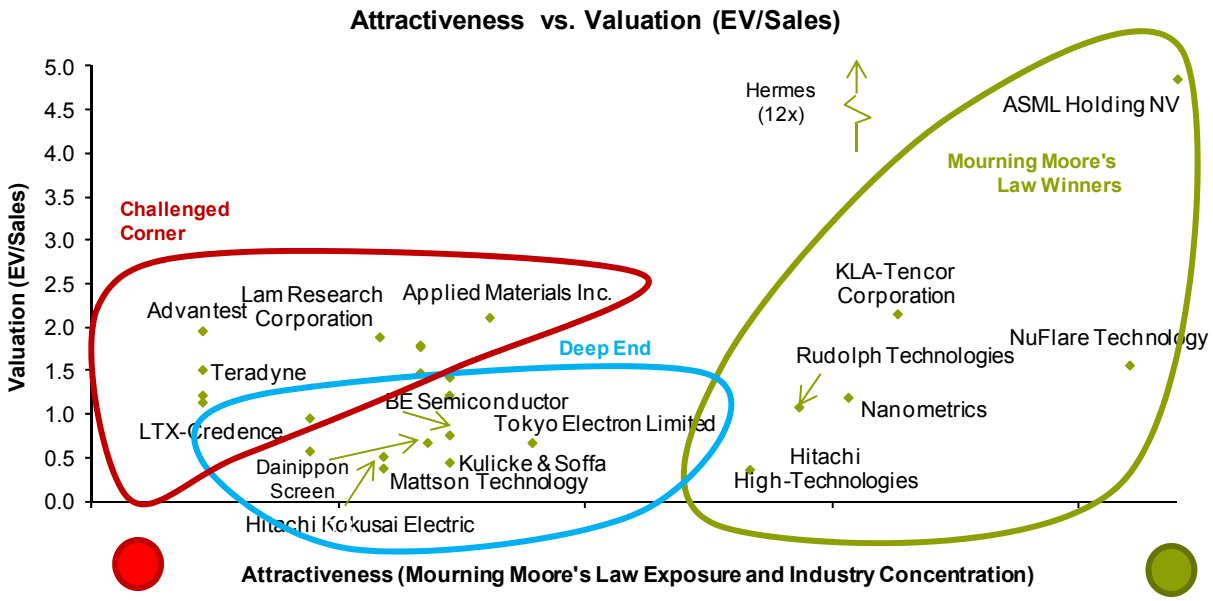
Source: Gartner and Bernstein estimates and analysis.

Exhibit 106 **We Summarize "Attractiveness" of These Companies and Find ASML, KLA Tencor, Hermes, NuFlare, Rudolph and Nanometrics Are the Best Positioned**

Company Name	Exposure to Industry Concentration (HHI Index)	Moore's Law Exposure	Attractiveness Rating
ASML Holding NV	66%	100%	166%
Applied Materials Inc.	25%	22%	48%
Tokyo Electron Limited	39%	10%	49%
KLA-Tencor Corporation	33%	88%	121%
Lam Research Corporation	19%	10%	29%
Dainippon Screen	25%	10%	35%
Teradyne	33%	-47%	-14%
Nikon	66%	16%	82%
Aixtron	20%	16%	36%
ASM International	6%	44%	49%
Kulicke & Soffa	5%	44%	50%
Disco	5%	44%	50%
Hitachi High-Technologies	33%	68%	101%
BE Semiconductor	5%	44%	50%
SEMES	27%	10%	36%
Tokyo Seimitsu	5%	44%	50%
Daifuku	11%	7%	18%
Muratec	11%	7%	18%
NuFlare Technology	66%	90%	157%
Advantest	33%	-47%	-14%
LTX-Credence	33%	-47%	-14%
Brooks Automation	11%	7%	18%
Nanometrics	33%	83%	116%
Hitachi Kokusai Electric	27%	-1%	25%
Rudolph Technologies	33%	73%	106%
Nissin Ion Equipment	50%	-1%	48%
Mattson Technology	27%	-1%	25%
Veeco	20%	16%	36%
Hermes Microvision	33%	78%	111%
Others	15%	35%	50%

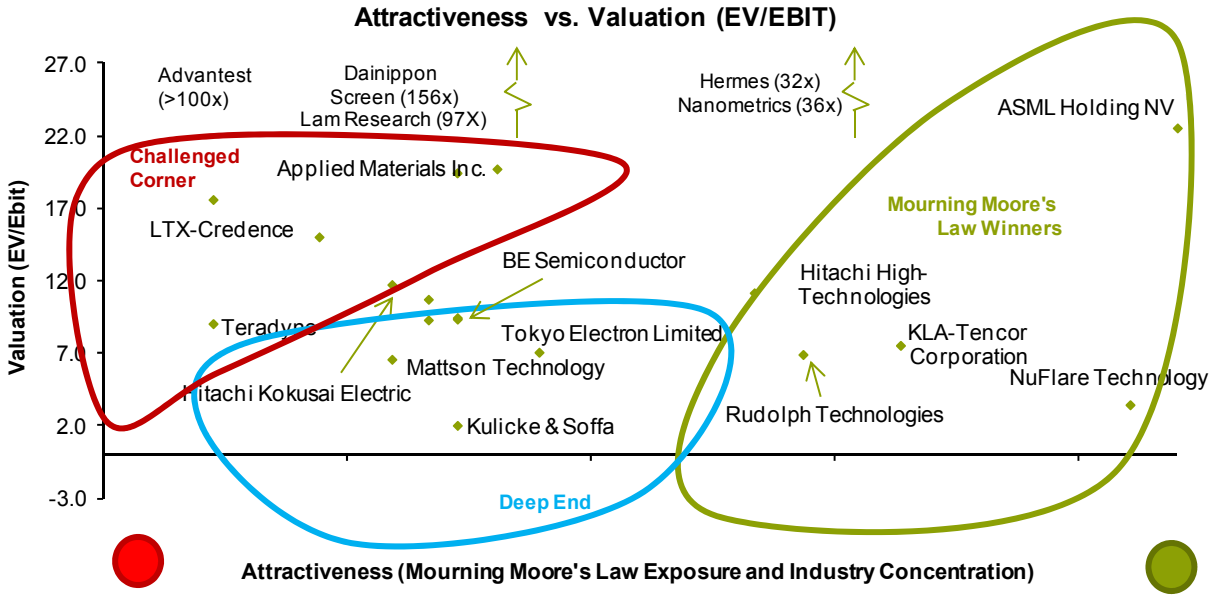
Source: Bernstein estimates and analysis.

Exhibit 107 **We Identify Three Groups in the Semi-Cap Space: Deep End, Challenged Corner and Mourning Moore's Law Winners (I)**



Source: Bloomberg L.P. and Bernstein estimates and analysis.

Exhibit 108 **We Identify Three Groups in the Semi-Cap Space: Deep End, Challenged Corner and Mourning Moore's Law Winners (II)**



Source: Bloomberg L.P. and Bernstein estimates and analysis.

Exhibit 109 Summary of Key Metrics

	Ticker	Name	Market cap (USD M)	Business description	Mourning Moore's law exposure	Segment concentration index	Technological shift risk	EV/Sales Relative to Peers	EV/Sales Relative to history	EV/EBIT Relative to Peers	EV/EBIT Relative to history
Mourning Moore's Law Winners	ASML NA Equity	ASML	30,301	Market share leader in Lithography eqpt	100%	66%	Low. EUV is the most advanced Next Gen Lithography Technology.	96%	92%	68%	91%
	6256 JQ Equity	NuFlare Techn.	918	Market share leader in Mask writing eqpt	90%	66%	Low. E-beam writers have the best resolution.	68%	93%	4%	41%
	KLAC US Equity	KLA-Tencor	8,810	Market share leader in Process control	88%	33%	Material. Some Risk from e-beam inspection and from ASML for overlay metrology.	92%	17%	20%	16%
	RTEC US Equity	Rudolph Technologies	368	Process control equipment maker. Expanding into advanced packaging eqpt	73%	33%	Low. Macro inspection resolution is generally high (less critical). Packaging segment doesnt move as fast as Moore's law.	36%	17%	12%	8%
	NANO US Equity	Nanometrics	324	Metrology equipment maker, specializing in OCD equipment	83%	33%	Positive. Favorable exposure to OCD wafer inspection technology (share gainer). Proprietary algorithms differentiate Nanometrics position.	44%	28%	80%	8%
	8036 JT Equity	Hitachi High-Tech	3,374	Process control equipment maker.	68%	33%	High. Exposed to CD-SEM wafer inspection technology (losing share to OCD).	0%	83%	44%	72%
	3658 TT Equity	Hermes Microvision	1,969	Process control equipment maker, specializing in E-beam inspection tools.	78%	33%	Positive. Ebeam inspection are the most advanced and can only structurally gain share.	100%	91%	72%	43%
Deep End	8035 JT Equity	Tokyo Electron Ltd	9,094	#1 or #2 eqpt maker for Photoresist processing, etch, RTP	10%	39%	Low. Photoresist and Etch are getting incrementally challenging but no major technology transitions. ALD growing fast.	20%	5%	16%	23%
	7735 JT Equity	Dainippon Screen	1,286	Etch, Clean Planarization eqpt maker	10%	25%	Low. Etch is getting incrementally challenging but no major technology transitions. ALD growing fast.	24%	38%	96%	100%
	KLIC US Equity	Kulicke & Soffa	839	#2 player in die level manufacturing equipment	44%	5%	Low. Packaging and Assembling segment usually doesnt move as fast as Moore's law.	8%	7%	0%	5%
	BESI NA Equity	BE Semiconductor	367	#4 player in die level manufacturing equipment	44%	5%	Low. Packaging and Assembling segment usually doesnt move as fast as Moore's law.	28%	61%	36%	56%
	6756 JT Equity	Hitachi Kokusai Electric	1,217	#3 player in RTP/Oxidation and diffusion	-1%	27%	Low.	12%	77%	48%	100%
	MTSN US Equity	Mattson Technology	94	Small player in RTP/Oxidation and diffusion	-1%	27%	Low.	4%	16%	8%	3%
Challenged Corner	AMAT US Equity	Applied Materials Inc.	17,281	Diversified semicap eqpt maker, exposed to chamber process steps	22%	25%	Low. Etch is getting incrementally challenging but no major technology transitions. ALD growing fast.	88%	26%	64%	67%
	LRCX US Equity	Lam Research Corp.	7,400	Market share leader in Etch, Clean Planarization eqpt	10%	19%	Low. Etch is getting incrementally challenging but no major technology transitions. ALD growing fast.	80%	38%	92%	90%
	TER US Equity	Teradyne	3,129	Leading player in test equipments	-47%	33%	Low.	64%	34%	24%	33%
	6857 JT Equity	Advantest	2,937	Leading player in test equipments	-47%	33%	Low.	84%	32%	100%	100%
	LTXC US Equity	LTX-Credence	276	Small test equipment manufacturer	-47%	33%	Low.	40%	29%	56%	61%

Source: Bernstein estimates and analysis.

Intel: Their Eyes Are Bone Dry, But Will Investors Have to Cry?

In this chapter, we discuss the implications of a market moving from a performance to power focus on Intel (which has been, of course, the king of performance). In fact, we believe Intel has a credible path forward in an industry becoming more concerned with power efficiency, leveraging a tremendous manufacturing and technology advantage to finally deliver products that could eventually be best-in-class on the metric (and, conceivably, disrupt the existing foundry ecosystem, which will be discussed in more detail in the following chapter).

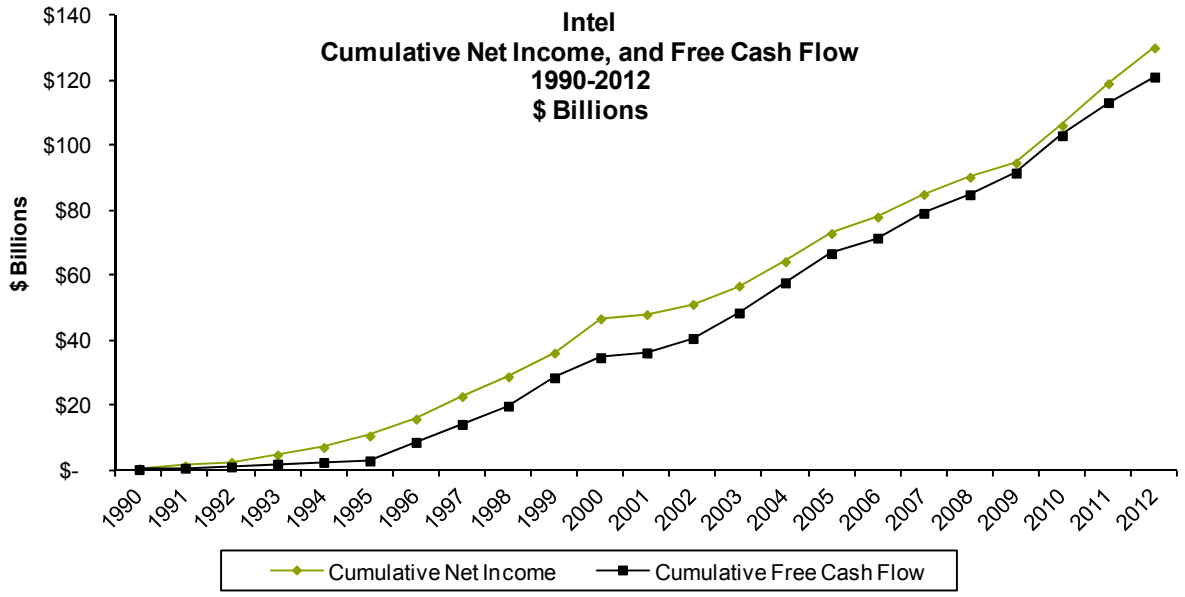
Unfortunately, Intel is also facing a transformation of its business model, as new markets driving this growth cannot support the pricing Intel enjoys in the performance-hungry (but declining) traditional PC space. This is resulting in a bifurcation — heavy investments are required today to win tomorrow's new market, but which come in conjunction with a deteriorating core business right now, and new business (once one) will inherently be lower return than today's deteriorating core. We believe Intel's current path is absolutely the right one for the company in the long term, but likely to be painful for the stock during the multi-year transition period.

Intel Is Negotiating a Transition from Performance-Focus to Power Efficiency…

As the Focus of Technology Transitions from Performance to Power Efficiency, Intel Can Likely Remain Advantaged

Of all the semiconductor companies in the industry, not one has benefitted from the steady progression of Moore's Law more than Intel (named for, of course, its founder Gordon Moore). Over the course of more than 40 years in business, the company has generated huge amounts of value; since 1990 the company has cumulatively produced more than $130 billion in net income, and more than $120 billion in free cash flow (see Exhibit 110) as its technology superiority led increasingly to market dominance.

Exhibit 110 Intel's Leadership Has Resulted in Significant Value Creation



Source: Capital IQ and Bernstein analysis.

The rise of the personal computer sparked a revolution in consumer-based performance computing offerings, and the company capitalized. It migrated out of rapidly commoditizing DRAM to a high-value performance based offering that generated huge benefits. The company became over the following decades the preeminent player in personal computing as the WinTel "monopoly" took hold, with a fast-growing market where consumers and enterprises were more than willing to pay for increased performance at every generation (supporting average selling prices for microprocessors well in excess of $100 apiece).

Last decade, Intel further formalized its Moore's Law progression with the advent of "Tick-Tock," a more refined mechanism for technology transitions that sought to de-risk (as much as possible) the process while still introducing new products and improvements on an annual basis. Namely, the company tries to focus on either an architectural or technology (node) transition (but not both) at any given moment. The "Tick" represents a node shrink (with similar micro-architecture); the "Tock" represents a micro-architecture shift while leaving process technology unchanged. With the advent of this methodology the technology gap Intel has shown versus competitors (namely, the foundries) has continued to widen over the last five to 10 years, with Intel introducing new materials and techniques (strained silicon, high-k metal gate, and now tri-gate) years before most other players.

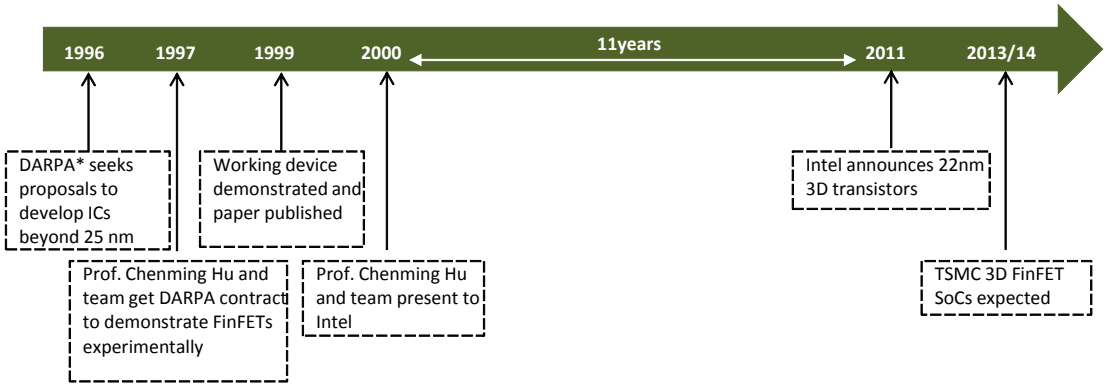
But, as Computing Horsepower Has Become Closer and Closer to "Good Enough," and New Mobile Applications Have Made Battery Life a Priority, Intel Has Been Forced to Renew Attention on Power

Each Moore's Law transition generates a transistor budget that can be spent on either performance (double the transistors on the same die size) or cost (the same number of transistors on a smaller die size) or some mix of the two. At the same time, power burn per transistor drops (though other issues, such as leakage, rear their heads and necessitate new, innovative, and non-classical solutions). However, we have been reaching the point over the last few years where incremental performance has not been enough to offset inherent power liabilities.

Indeed, at one point not so long ago we were looking at the prospect of chips burning through calculations at 5 GHz or more. Unfortunately, they were also ready to burn through the computer (and our laps) given the power requirements. Thus, over the last few years Intel has been forced to turn much more attention to the power efficiency of its offerings.

The writing has been on the wall for some time on this front, particularly for traditionally fabricated transistors (indeed, classical transistor scaling broke down quite some time ago). Thus, Intel recognized something special had to be done in order to bring its offerings to a power footprint that would 1) enable notebook form factors with truly acceptable battery life, and 2) be capable of (finally) attacking new mobile markets that had historically been shuttered to the company given the power characteristics of its products. Hence, in 2011 Intel became the first semiconductor company to successfully commercialize three-dimensional (or "tri-gate") transistors in high volume manufacturing, following more than a decade of development (see Exhibit 111).

Exhibit 111 Intel Had Been Working on 3D Transistors for More Than a Decade Before Its Launch in 2011

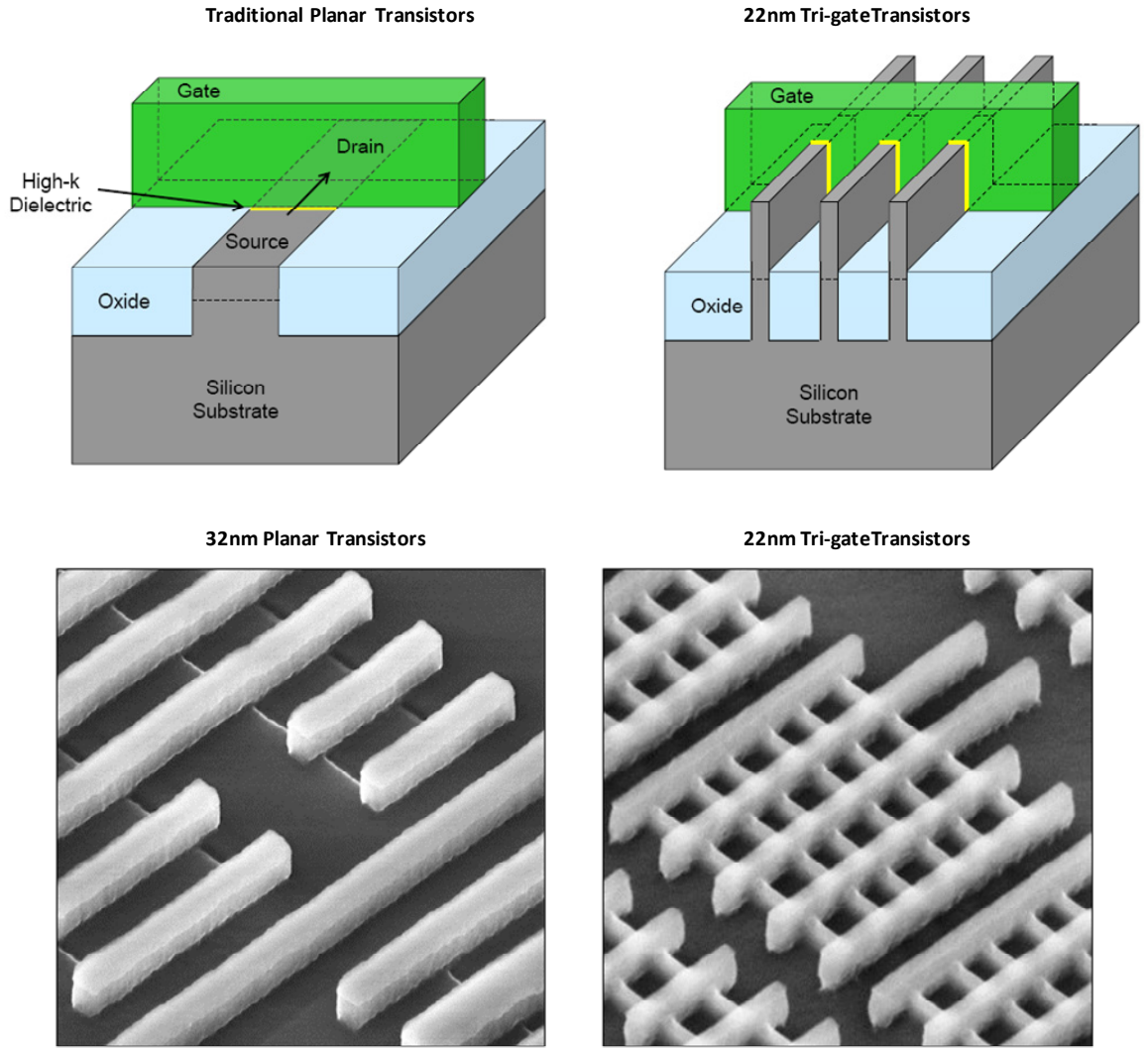


Note: DARPA – Defense Advanced Research Projects Agency.

.Source: IEEE Spectrum, corporate reports and Bernstein analysis.

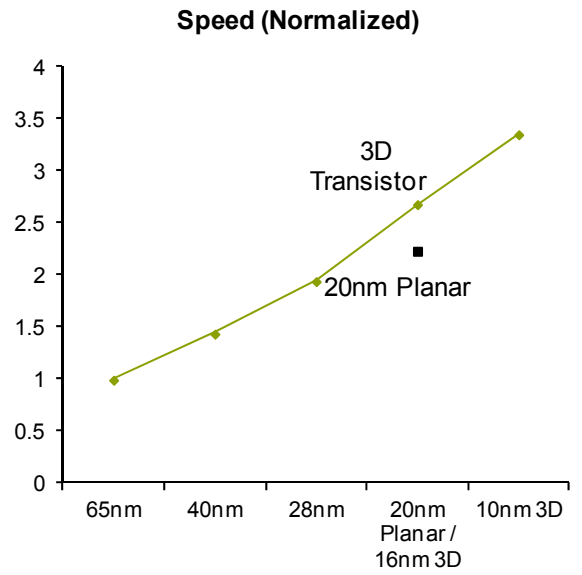
Tri-gate transistors (see Exhibit 112) exhibit a structure in which the traditional source-channel-drain is lifted out of the substrate surface, allowing the gate structure to "wrap around" it on three sides, providing much better control of the electrical characteristics. Three-dimensional transistor structures can drive ~20% better performance, or 20-30% lower power, at the same technology node (see Exhibit 113 and Exhibit 114). Given Intel is combining tri-gate introduction with an actual node shrink (moving from 32nm planar to 22nm trigate), it can deliver >50% reduction in active power for the same performance (see Exhibit 115).

Exhibit 112 **Intel's Trigate Transistor Design (3D Architecture) Reduces Gate Delay Current and Operating Voltage**



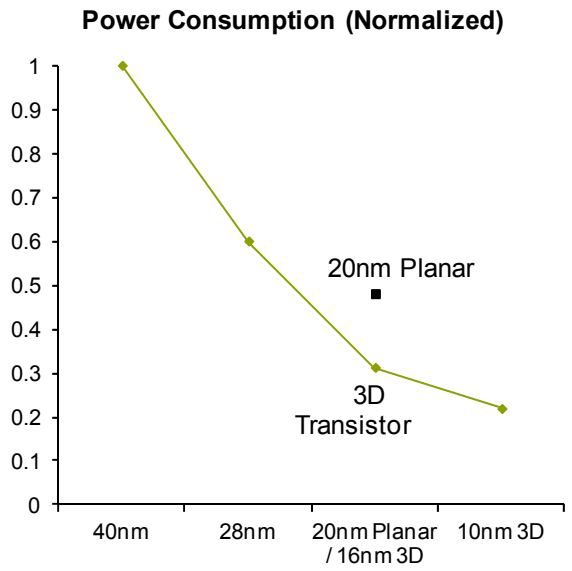
Source: Intel and Bernstein analysis.

Exhibit 113 The 3D Transistor Delivers 10-20% Faster Speed Than the Planar Version at the Same Node…



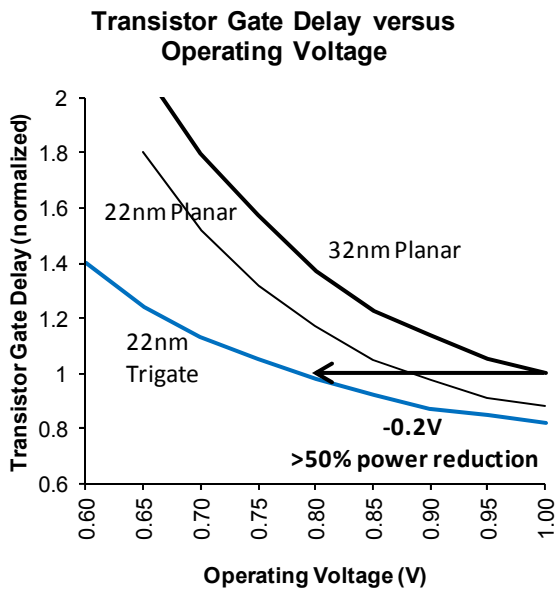
Source: TSMC and Bernstein estimates and analysis.

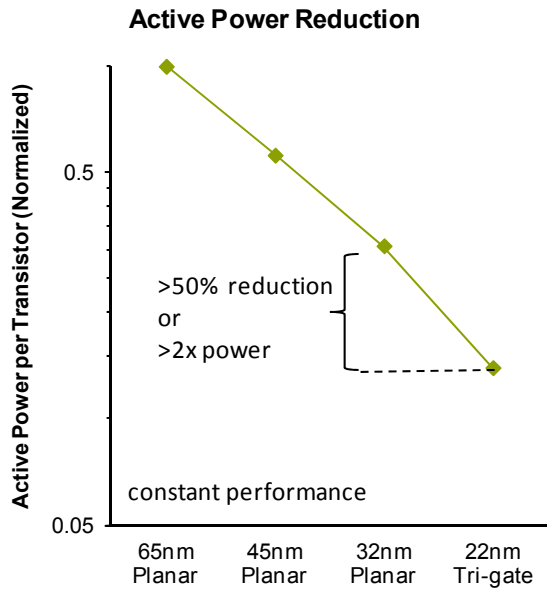
Exhibit 114 …or 20-30% Lower Power Consumption



Source: TSMC, Xilinx and Bernstein estimates and analysis.

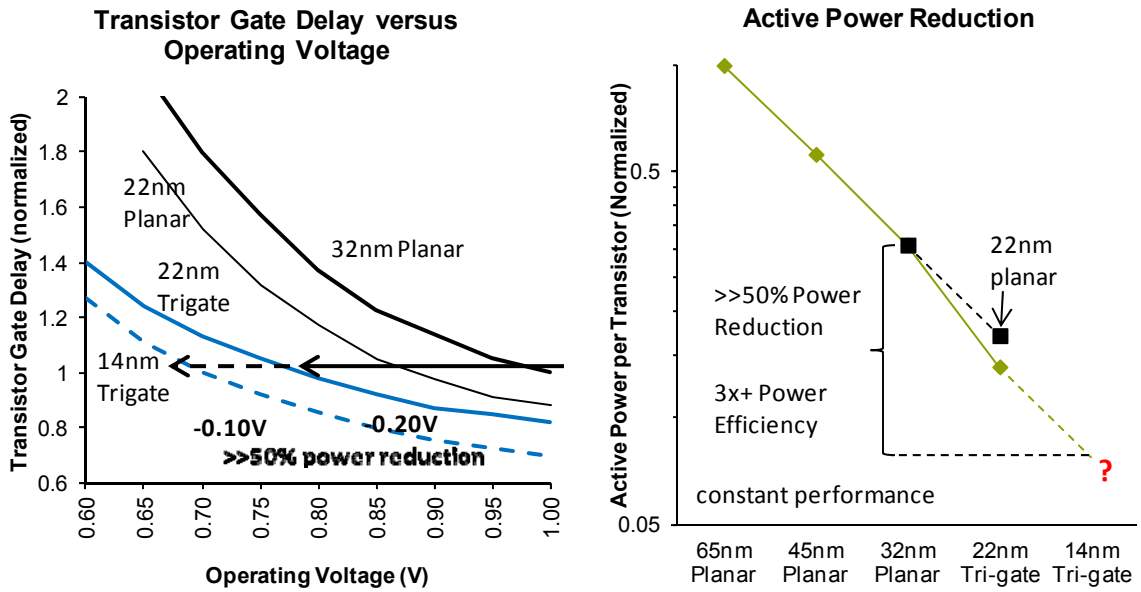
Exhibit 115 The Combination of a Node Jump and the Migration to Tri-Gate Delivers a Reduction in Power of Above 50%





Source: Intel and Bernstein analysis.

Exhibit 116 **At 14nm and With Three-Dimensional Transistors, We Estimate Intel Would Be in a Position to Produce Chips Three Times More Power Efficient Than at 32nm**



Source: Intel and Bernstein estimates and analysis.

Exhibit 117 **Pros and Cons Between 3D Transistor and Planar**

	3D Transistor	Planar Transistor
Pros	• 10-20%[1] better performance • ~20-30%[2] lower power consumption	• Cheaper • Better ecosystem readiness • Possibly better yield
Cons	• Costlier by 2-3% process cost according to Intel • Require additional ecosystem support • Potential yield challenge	• Weaker performance • Higher power consumption

Note: 1) Please see http://www.realworldtech.com/page.cfm?ArticleID=RWT050511195446&p=2; (2) Please see http://www.monolithic3d.com/2/post/2011/8/will-trigate-play-an-important-role-in-the-intel-armtussle.html for technical details of power saving calculation.

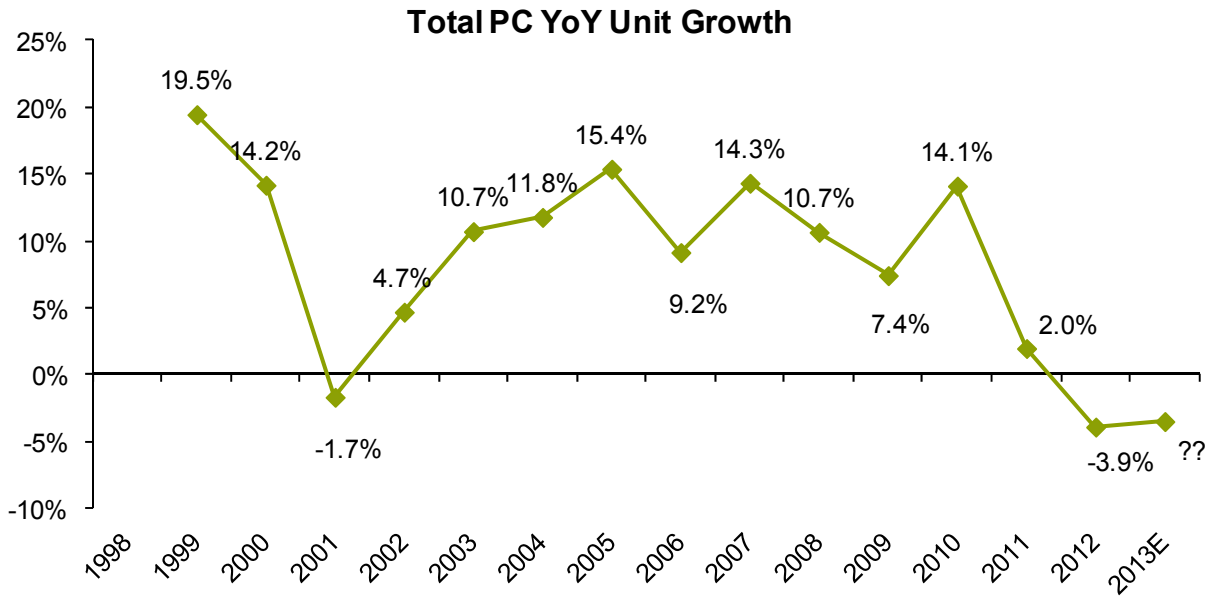
Source: Bernstein research.

...But Driven by Core PC Market Stagnation and Mobility Growth

Intel's Core Business Is at Significant Risk of Being Replaced by New Mobility Markets

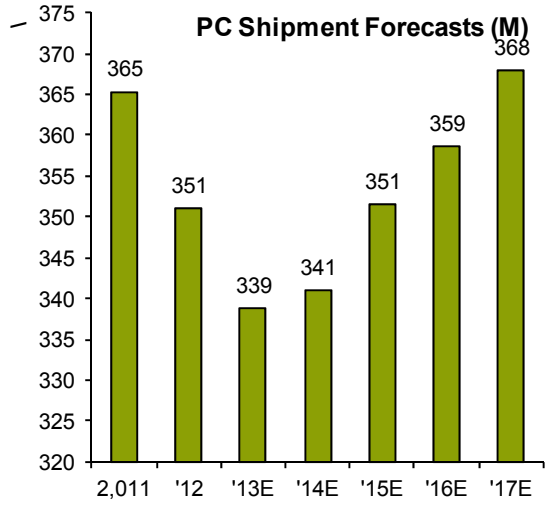
A move toward power efficiency as *the* design point cannot come soon enough, as Intel is facing a scenario in which its core business, long a source of incredible profit generation, may be slowing (or worse); indeed, 2012 marked the first time since the dot-com crash that personal computers posted negative year-over-year growth (see Exhibit 118), and current third-party forecasts do not point to this trend reversing anytime soon (see Exhibit 119 and Exhibit 120).

Exhibit 118 PC Market Posted Negative YOY Growth in 2012 With 2013 Expected to Be Negative as Well



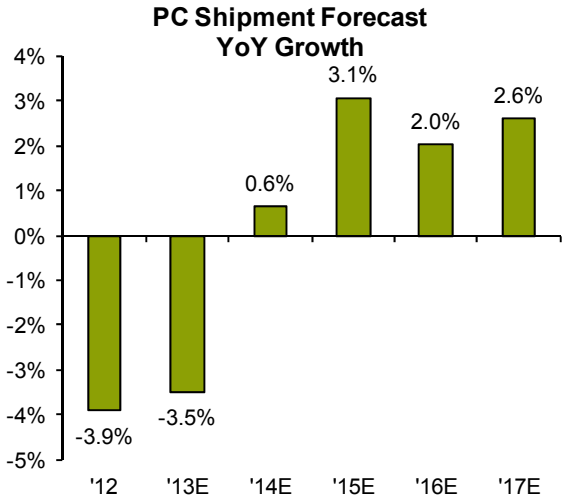
Source: Gartner and Bernstein analysis.

Exhibit 119 Current Forecasts Do Not Foresee Any Returns to Robust PC Industry Growth...



Source: Gartner and Bernstein analysis.

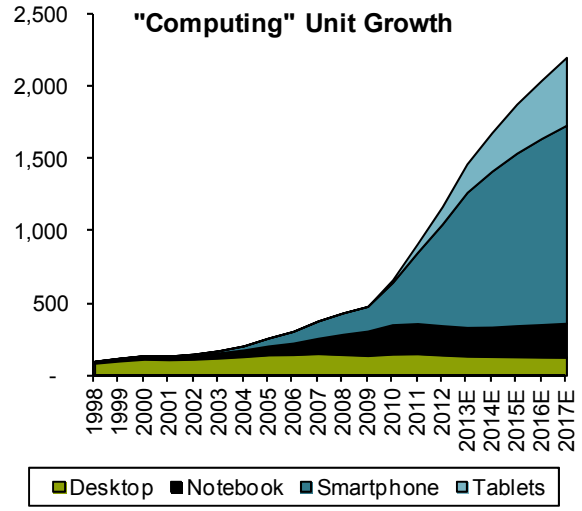
Exhibit 120 ...With Several Years of Negative Growth Forthcoming



Source: Gartner and Bernstein analysis.

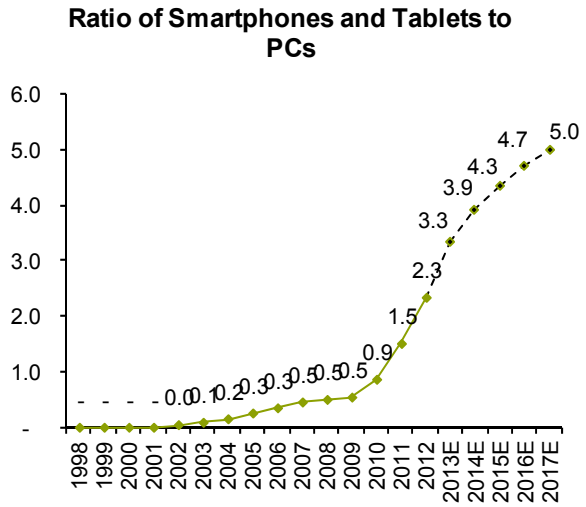
The very definition of a "computing device" is shifting, with new form factors already hugely outpacing traditional PCs in terms of sheer unit growth. While PCs have formed a reasonably stable ~350 million unit market for several years, growth in smartphones and tablets has been truly explosive. In fact, it is likely that next year "non-traditional" computing platforms such as these will out-ship traditional PCs by a factor of more than three to one (see Exhibit 121 and Exhibit 122). And lest one think this is strictly a smartphone phenomenon, even tablets are forecast to approach, and soon exceed, PC shipments all on their own (see Exhibit 123).

Exhibit 121 While the PC Isn't Necessarily Dead…



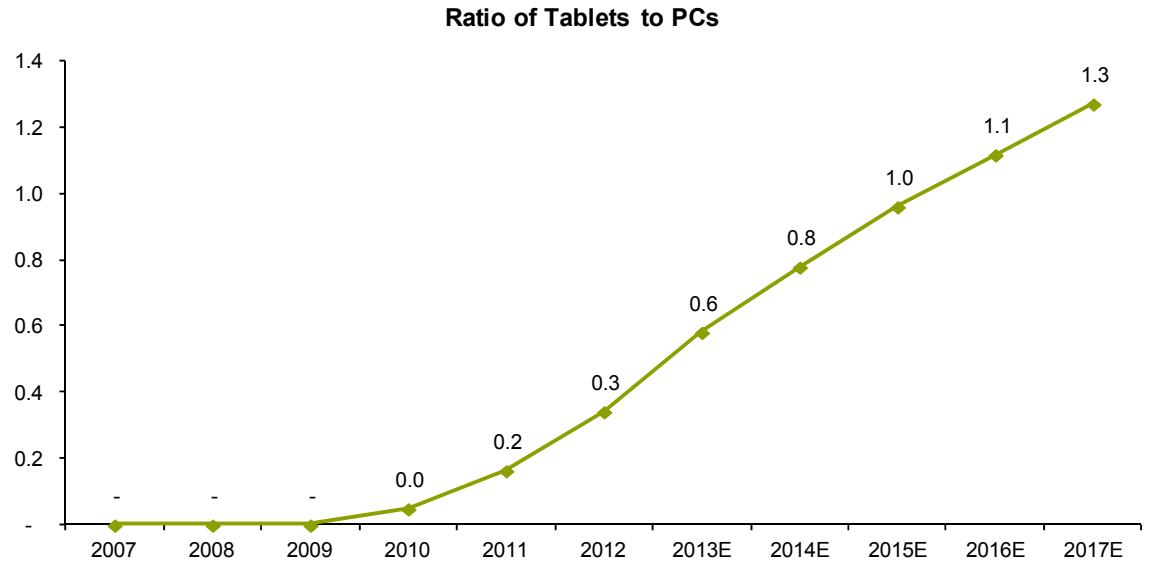
Source: Gartner, Strategy Analytics and Bernstein estimates and analysis.

Exhibit 122 ...Smartphones and Tablets Are an Increasing Percentage of "Computing" Unit Growth



Source: Gartner, Strategy Analytics and Bernstein estimates and analysis.

Exhibit 123 Ratio of Tablets to PCs is Expected to Increase Rapidly in the Next Five Years



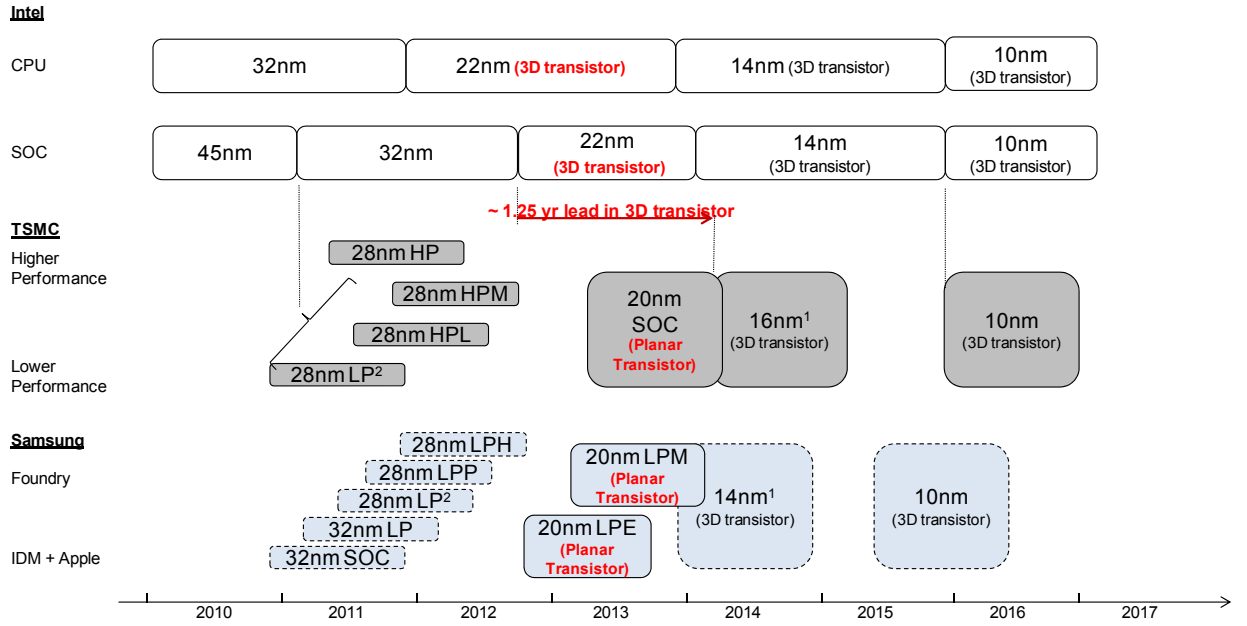
Source: Gartner, IDC, Strategy Analytics and Bernstein analysis.

However, Intel's Efforts Are Already Allowing Delivery of Products That, in Theory, Could Be Competitive (or More Than Competitive) on Power

But, Intel is not taking the shift in its markets lying down. It continues to widen its technology gap to the rest of the industry, and despite efforts by competitors to catch up the gap appears to be widening (see Exhibit 124), finally allowing it to drive the improvements in power efficiency needed to attack new mobile markets. In fact, Intel's current offerings for the smartphone market (built on a 32nm planar process) are already quite respectable in terms of power (not the best, but not the worst — see Exhibit 125 through Exhibit 128). Additionally, Intel is accelerating its Atom SoC roadmap, pushing three nodes in three years to bring Atom much closer to the edge of the Moore's Law efforts in an attempt to accelerate the power-

savings inherent in its new technology (note that the first 22nm tri-gate Atom products, code-named "Baytrail," are expected to hit the market this year).

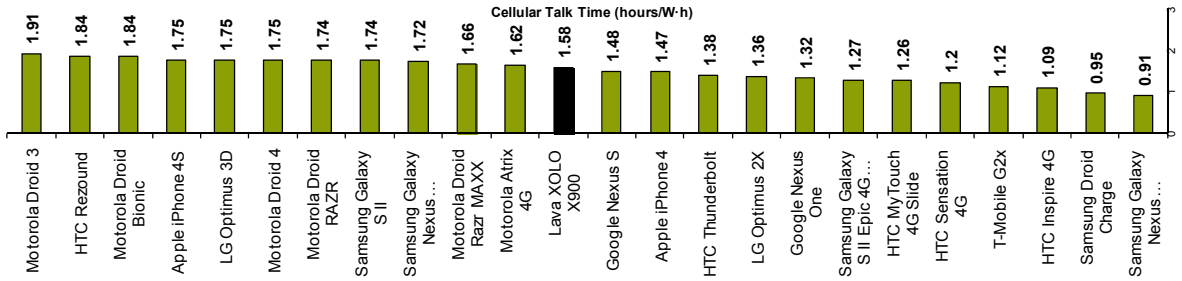
Exhibit 124 **TSMC and Intel Plan to Reach the 22/20nm Node Late This Year and the 16/14nm Node in 2014/2015**



Note: Dotted line refers to SCB estimate. Solid line is company reported. 1. TSMC's 16nm, GlobalFoundries' 14XM and Samsung's 14nm are all "3D transistor version of 20nm." They are similar technologies and deliver comparable performance. 2. Poly/SiON flavor

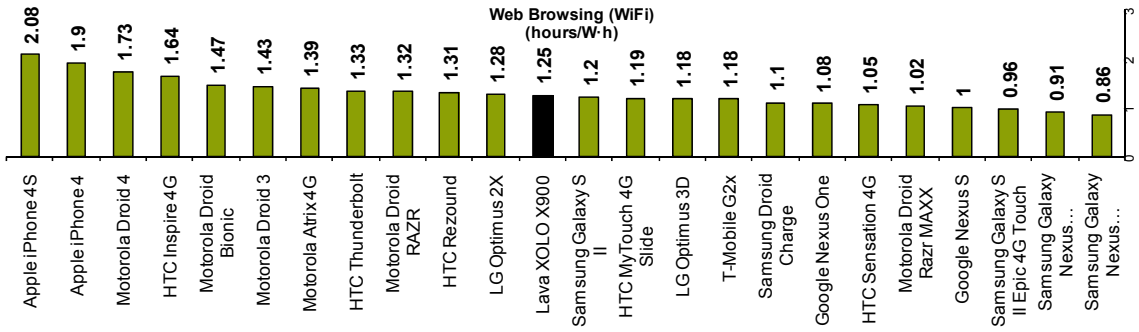
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 125 **Intel's Current Smartphone Products Offer "Respectable" Power Efficiency — Cellular Talk Time**



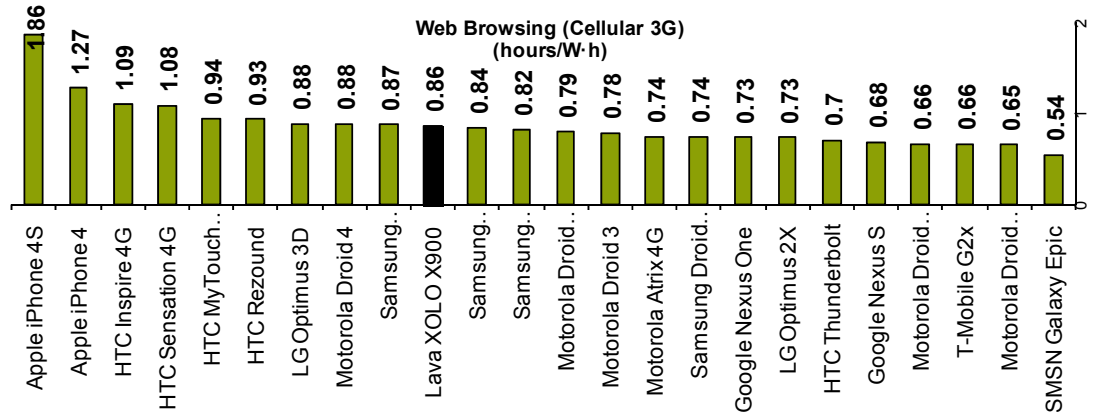
Source: Anandtech and Bernstein analysis.

Exhibit 126 **Intel's Current Smartphone Products Offer "Respectable" Power Efficiency — WiFi Web Browsing**



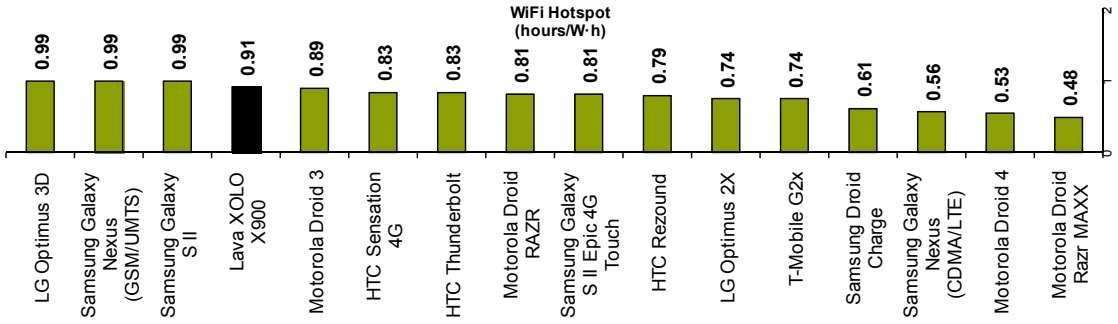
Source: Anandtech and Bernstein analysis.

Exhibit 127 **Intel's Current Smartphone Products Offer "Respectable" Power Efficiency — Cellular Web Browsing**



Source: Anandtech and Bernstein analysis.

Exhibit 128 **Intel's Current Smartphone Products Offer "Respectable" Power Efficiency — WiFi Hot Spot**



Source: Anandtech and Bernstein analysis.

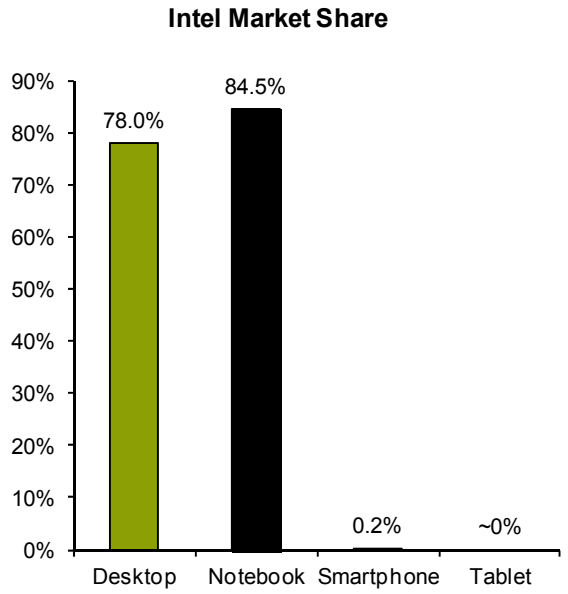
However, the Inherent Business Model Shift Does Not Play in Intel's Favor

However, while Intel can undoubtedly be competitive in new growth markets (and market share, still hovering close to zero, leaves lots of room for unit upside; see Exhibit 129), the shift from a performance-based business to one focused on power efficiency has one large inherent disadvantage versus Intel's core business — namely price. While the theoretical unit volume of smartphones and tablets could be 3x or more of Intel's traditional PC TAM, typical price points for the processors

in these devices are perhaps one-fifth of Intel's normal notebook ASP (see Exhibit 130).

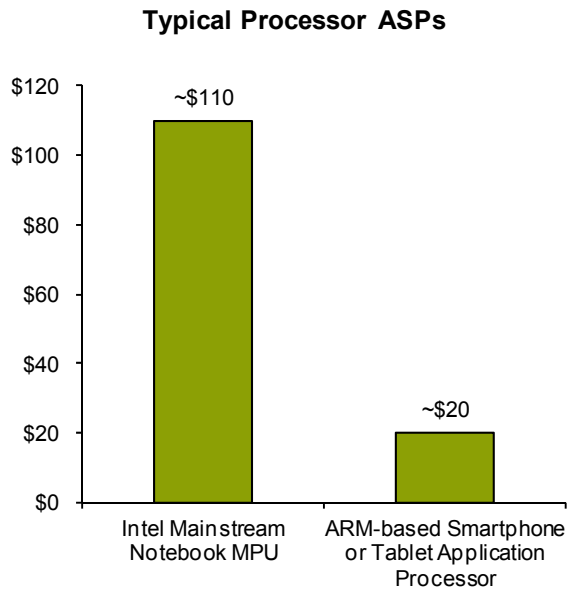
To wit, Intel's current (mostly performance-based) core business enjoys remarkable economics, but likely is not going to grow much anymore (indeed, many fear the opposite); new (power-sensitive) markets could offer (in theory) enormous unit growth potential, but will come at much lower ASPs. This implies a need to take enormous amounts of share to move the needle.

Exhibit 129 Intel's Share in New Growth Markets Is Close to Zero, Creating Significant (Theoretical) Opportunity for Unit Upside



Source: Mercury Research, Strategy Analytics, IDC and Bernstein estimates and analysis.

Exhibit 130 Processor ASPs for Tablets and Smartphones Are Perhaps One-Fifth of Intel's Notebook Chips



Source: Mercury Research and Bernstein estimates and analysis.

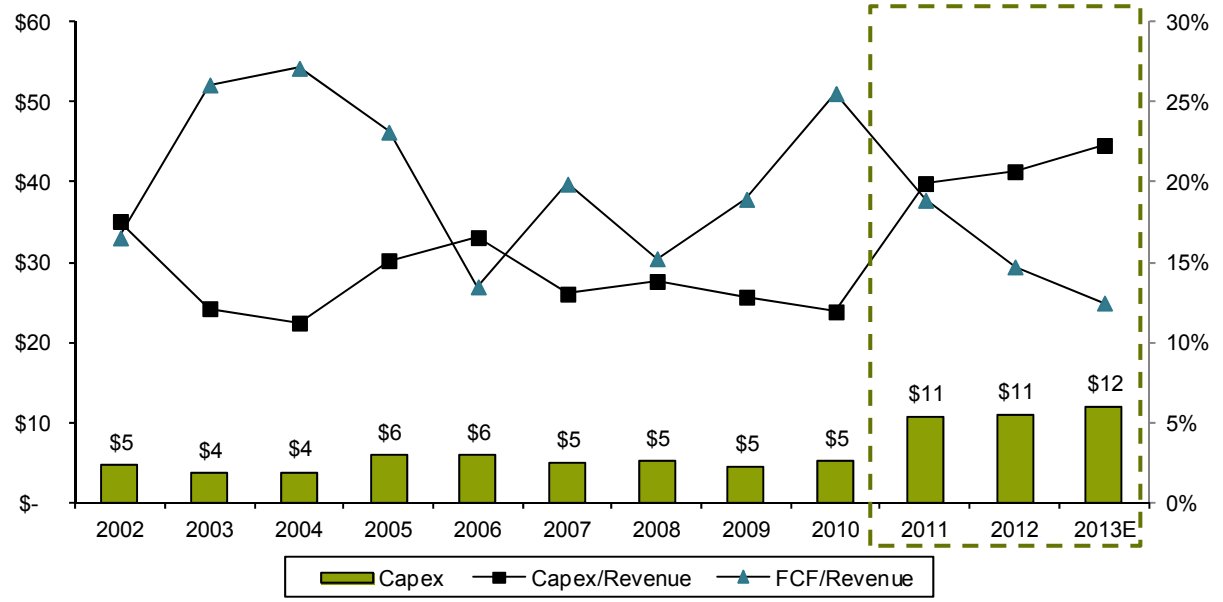
The Required Transformation to Cope With New Market Realities Is Likely to Be Painful for Intel

Given the economics of new "growth" mobile markets, focused on power, are not nearly as good as what Intel enjoys in its core, Intel is facing a dilemma — hunker down and protect the core, or go all-in to new opportunities at the risk of lower returns and (potentially) exacerbating cannibalization?

While the former may work out well in the short term, we believe it likely would be signing a longer-term death warrant; in our opinion (and likely Intel's as well, given its recent behavior) the latter strategy appears to be the one to pursue. Namely, to take the kind of share that will be required to move the needle, Intel needs products that are not just competitive with, but are rather massively better than anything the competition can deliver on both performance *and* power. And, if the company is to earn decent margins selling huge volumes of $20 chips, it will need a cost position to match (particularly as cost reduction inherent in Moore's Law slows over the coming years), hence, a move to 450mm wafers. All together, these needs imply investment, lots of it, as the company continues to drive the technology gap to the competition ever wider.

Indeed, we believe this has already begun. Capital expenditure has surprised to the upside for each of the last three years (coming in at well over $10 billion per year, more than double the historical run-rate). At the same time, free cash flow has declined both on an absolute basis and as a percentage of revenue, reaching levels not seen in over a decade (see Exhibit 131).

Exhibit 131 **Intel's Capital Intensity Has Accelerated in Recent Years, Depressing Free Cash Flow as the Company Invests in Capacity and Technology**



Source: Corporate reports and Bernstein estimates and analysis.

We believe this heavy level of capital investment must continue given the market (and current competitive positioning) that Intel is faced with.

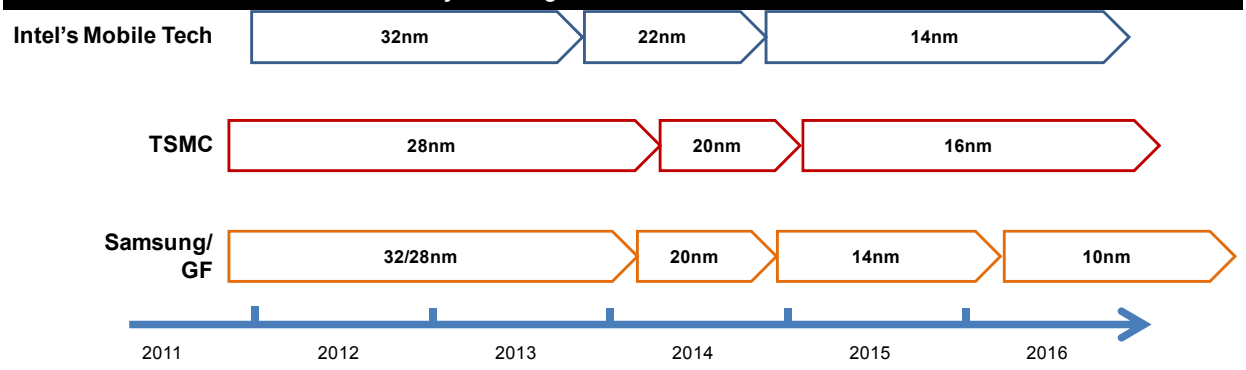
Heavy Investment Is, However, Resulting in an Ever-Widening Technology Gap to Competitors

Intel's Technology Lead Is Manifesting in Better Performance and Cost Trajectories vs. the Foundry Competition

Intel's introduction of tri-gate in 2011 appears to have taken the foundry industry by surprise (at least, most roadmaps at the time from competitors did not include the incorporation of 3-D transistors so early, typically defaulting to some flavor of FD-SOI instead). However, given Intel's successful adoption of the technology into high-volume manufacturing, most competitors have now slotted their own versions of 3-D into their roadmaps at a fairly rapid place.

However, it does appear that not all tri-gates are made equal. For example, most of Intel's foundry competitors are not really attempting to incorporate a shrink and introduction of 3D simultaneously. For example, while TSMC's "16nm Finfet" follows its "20nm planar" process on the roadmap, the "16nm" part is a bit of a misnomer — it is simply replacing its planar transistors with 3D versions, keeping the pitch unchanged. Thus, at the 22/20nm node Intel has performance and power savings versus TSMC, and while die size would technically be larger than TSM's 20nm, it isn't shipping that one yet. When both companies make the transition to the 16/14nm node, assuming the foundries don't misstep on their roadmap performance and power may be on par, Intel is likely to maintain a cost advantage (see Exhibit 132). In general we see the cost savings portion of Moore's Law slowing for most participants over time, but the foundries encountering it first, given an inability to manage both shrink and 3D introduction simultaneously (see Exhibit 133).

Exhibit 132 Summary of Changes in Performance and Cost Difference for 22/20nm and 16/14nm

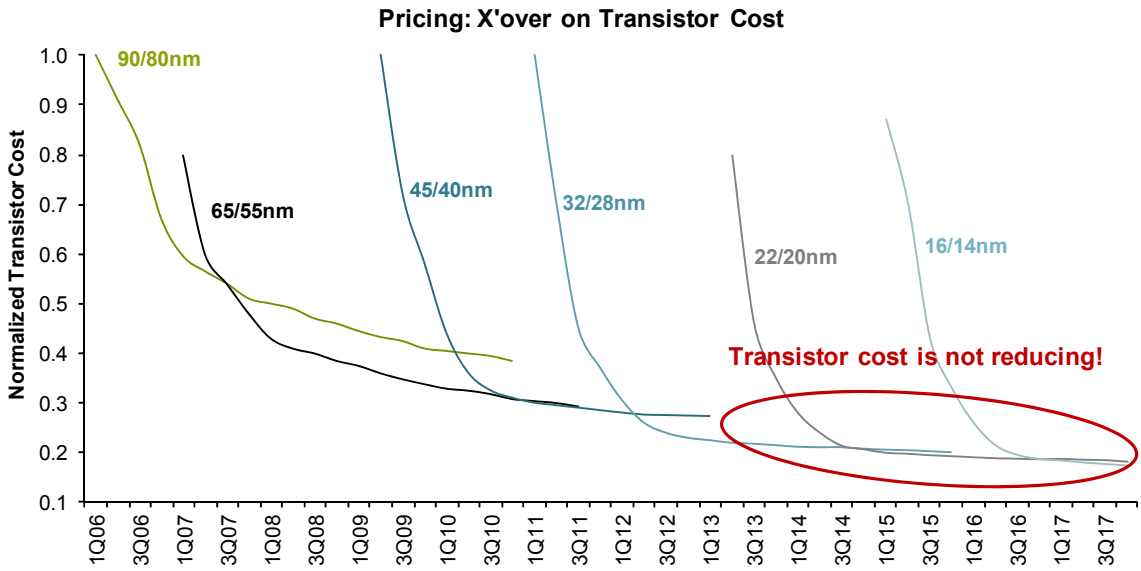


	22/20nm node	16/14nm node
Performance	Intel better by 10-20%	Intel better by 20-30%
Power Consumption	Intel better by 20-30%	Intel better by 20-30%
Die area [2]	TSMC smaller by 36%	Intel smaller by 23%

Note: 1. The left edge of the box is beginning of mass production; 2. Die area is estimated based on metal pitch.

Source: Bernstein research.

Exhibit 133 Transistor Cost Reductions Also Seem to Be Plateauing



Source: Nvidia and Bernstein analysis.

Intel Is Now Seeking to Increasingly Monetize Its Significant Process Technology Advantage More Directly Against Foundry Competitors

Beyond using new low-power capabilities to gain a foothold in new growth markets, Intel appears to now be taking a more direct route to monetizing its increasing technology advantage (we believe both for financial upside, as well as for the possibility of sowing disruption against the competition's own technology efforts). In fact, it is now seeking to directly target foundry business as a most transparent mechanism to benefit from its technology leadership.

As Moore's Law becomes more difficult, we are now seeing more direct competition in general between IDMs and foundries. Both sides have already fired opening salvos (e.g., Apple moving from Samsung to TSMC, Altera moving from

TSMC to Intel), and we expect this to intensify. In particular, Intel has the potential to drive, in the long term, significant disruption to the status quo.

Intel has been engaged in early foundry efforts with a variety of small customers (e.g., Achronix, Tabula, Netronone). Many of these initial efforts were likely more about learning the ins and outs of running a foundry business (the "Crawl" part of a "Crawl, Walk, Run" strategy), and speculation has been rampant for some time that it would seek to broaden its efforts. And of course, it did, announcing in February the addition of its first "major" customer, Altera, for whom it will make high-value, high-performance FPGAs.

Initial Foundry Efforts Appear to Be "High-Value, Low-Volume" Efforts With No Competitive Issues (e.g., "Strategic" Foundry); Ecosystem Disruption Is Likely to Be a Far Bigger Benefit Than Direct Financial Upside

Many IDMs acting as a foundry eventually encounter at least two problems — namely, enabling the competition, and competing with customers. So far Intel has been crystal-clear on the point — it does not intend to offer the benefits of its process technology leadership in scenarios where a competitive issue could arise. To that end, Intel's initial foundry efforts have been characterized by "high-value, low-volume" efforts where no competitive issue exists (see Exhibit 134). This makes significant sense — low volumes imply that Intel does not need to build capacity to satisfy such demand, and high value implies a significant amount of profit pool to spread across both parties (with both components likely securing decent economics for Intel). Of course, the low volume nature implies that these businesses are unlikely to move the needle significantly for Intel anytime soon (if ever).

But, they don't necessarily need to — in particular going after customers like Altera is telling — FPGAs were historically one of the first product types to ramp leading edge at the foundries. By picking off high-value leading-edge customers from TSMC and the foundry ecosystems, Intel makes it incrementally harder for them to ramp their own leading-edge processes. In fact, we believe the intangible benefits enjoyed by disrupting the competition at the leading edge are likely as much, if not more, important than financial upside stemming from the deals.

Exhibit 134 — Intel's Announced and Existing Foundry Partners Are FPGA and Similar Players, With Limited Volume, High Value per Part, and Limited to No Competitive Issues

Announced/Existing Foundry Partners	Potential Partners
Archonix	Cisco
Tabula	Apple?
Netronome	
Altera	
Microsemi	

Source: Corporate reports and Bernstein analysis.

However, the Majority of Industry Leading-Edge Volume Is in Mobile SoC — a Consequent Move Into "High Volume" Foundry Carries Business/Strategic and Financial Considerations

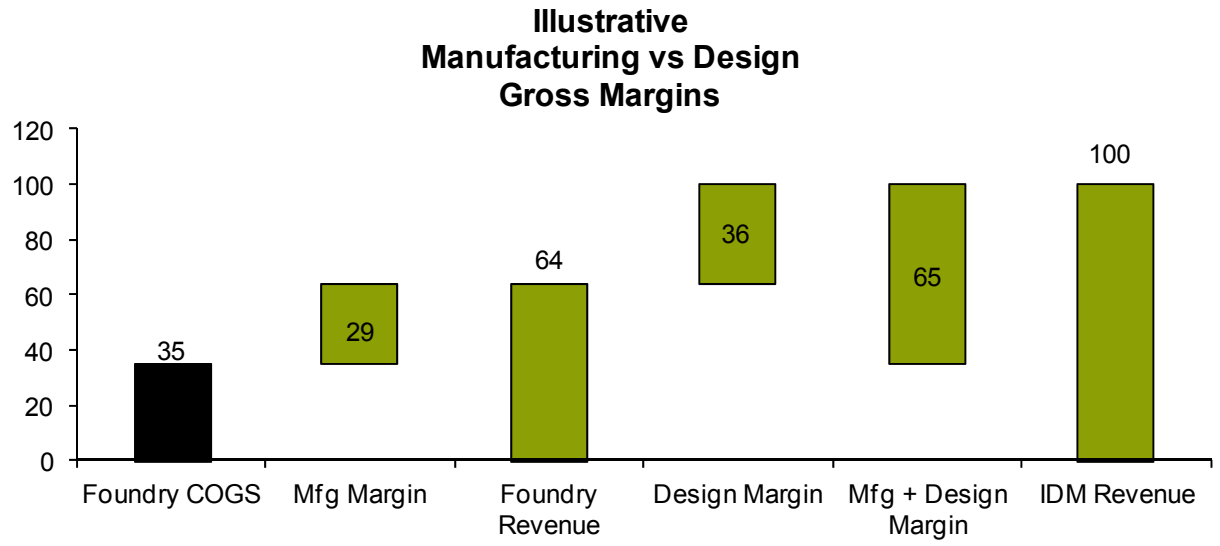
Low-volume, high-value "strategic" foundry should have good economics for Intel, but the lack of scale implies it is highly unlikely to ever move the needle materially for it. In fact, the majority of pure-play leading-edge foundry volume today is devices such as mobile SoCs. A consequent move into the "high volume" foundry space would have the potential to drive more upside for Intel (as well as far more disruption to the overall foundry ecosystem). However, it carries significant business/strategic as well as financial considerations that make us believe it is not on the table, at least for now.

In terms of business issues, any IDM operating as a foundry eventually may have to cope with the problem of 1) enabling competitors, and/or 2) competing with customers (witness, for example, the issues coming to light in the Apple/Samsung relationship). Given that Intel is attempting to grow its own

business into the smartphone/tablet space (the part of the market driving the bulk of leading-edge foundry volume today) it is safe to say that most mobile players considering Intel as a manufacturing partner would run into both problems. Thus, significant success for Intel's efforts in a high-volume foundry business would likely have to come at the expense of its current model; becoming the "foundry of choice" for the industry by definition would drive huge conflict issues (unless its own business collapses to the point of non-existence).

Additionally, the economics of such a move are likely to be negative for Intel, at least from an ROIC/capital intensity point of view. Recall that, as an IDM, Intel earns a gross margin on both the "manufacturing" and "design" portions of its business. In contrast, TSMC and other foundries earn a manufacturing margin only; they exist in a much shallower profit pool than Intel is used to (see Exhibit 135).

Exhibit 135 The Profit Pool of General Foundry Is Generally Much Shallower Than That of an IDM



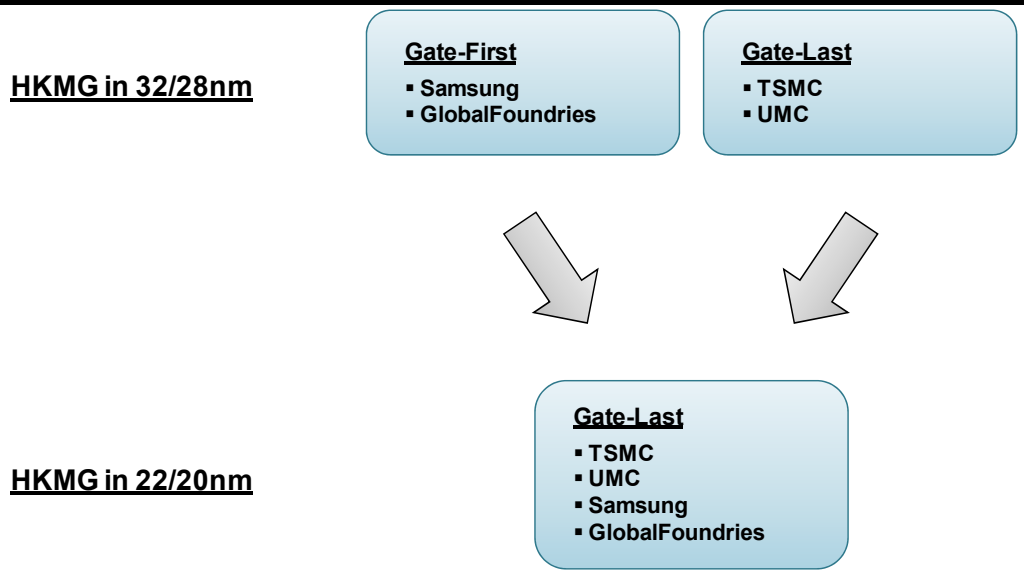
Source: Gartner, Strategy Analytics and Bernstein estimates and analysis.

Therefore (barring a complete collapse of Intel's core business) we see Intel's primary foundry efforts as remaining strategic in nature, mostly targeting high-value customers and, at the margin, removing the sources of bleeding-edge ramps from the pure-play foundry industry.

But, Could Apple Be a Wildcard?

However, while we believe a broad move into general-purpose, high-volume foundry is highly unlikely, Apple could in fact be a wildcard. Apple has somewhat unique characteristics — it is undoubtedly a competitor (at least at the platform/system level in the market that Intel is trying to penetrate), but it also has aspects of a strategic partner (and indeed, the companies have a long history of working together). And, of course Apple is in the process of moving away from its current supplier (Samsung) given that the competition issues are becoming too much to sustain (see Exhibit 136).

Exhibit 136 **We Think Apple Will Likely Change Its Foundry Supplier at 20nm as All Foundries Will Converge to "Gate-Last" in This Generation**



Source: Bernstein research.

Apple is making huge strides on its own custom chip designs (going as far as to implement a hand layout of the latest A6 processer cores); thus we believe a move by Apple to x86 will not be happening anytime soon (see Exhibit 137). However, it is true that it could benefit from Intel's process technology. Given Intel's increasing technology gap to the pure-play foundry industry (which all of Apple's non-Samsung competitors are tied to) we believe Intel would present a very attractive potential offering for Apple, given a roadmap that may be superior on both power/performance and cost versus what Apple can get otherwise (see Exhibit 138 and Exhibit 139).

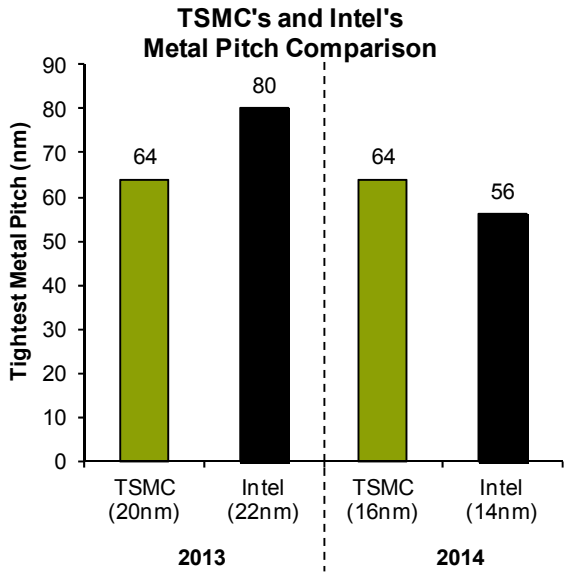
Exhibit 137 **Apple's Increasing Investment in Design Is Evidenced in Its Latest Processors, A6 and A6X, in Which Apple Designed Its Own Cores Instead of Using Cores Designed by ARM**

Product	iPhone / iPhone 3G	iPhone 3GS	iPhone 4 / iPad	iPhone 4S / iPad 2 / New iPad	iPhone 5
Chip			A4	A5 / A5X	A6 / A6X
# of Cores	1	1	1	2	2
Core	ARM 11	Cortex-A8	Cortex-A8	Cortex-A9	ARMv7, compatible with Cortex-A15*
Core Designed By	ARM	ARM	ARM	ARM	Apple
Manufacturing Geometry	90nm	65nm	45nm	45/32nm	32nm

* A6 and A6X are the first Apple SoC chips using its own ARMv7-based processor design, compatible with ARM Cortex-A15.

Source: AnandTech and Bernstein Research.

Exhibit 138 TSMC Should Have Slightly Tighter Transistor Density and Possibly Smaller Die Area and Lower Cost Than Intel in 22/20nm; However, the Advantage Can Be Reversed in 16/14nm



Source: Corporate data and Bernstein estimates and analysis.

Exhibit 139 We Estimate the Cost Savings Coming from Tighter Metal Wire Pitch to Be ~$3.2 per Chip

Cost Savings from Tighter Pitch	
Apple Chipset ASP (US$)	25
Value from Foundry per Chip (%)	35%
Value from Foundry per Chip ($)	**8.8**
Tightest Metal Pitch	
TSMC 20nm	64nm
Intel 22 nm	80nm
Area Saving from Tighter Pitch per Chip (%)	36%
Cost Savings from Tighter Pitch per Chip (US$)	**3.2**

Source: Bernstein estimates and analysis.

Additionally, we believe the strategic issues from Intel's standpoint, while still reasonably substantial, are likely less for Apple as a customer (versus say, Qualcomm). Apple does not sell its own chips (meaning competition occurs at the level of Intel's own customers, rather than at the chipset level); Apple can almost certainly provide volume commitments, it has a relatively simple product mix, lots of R&D resources to manage the port, and a decent enough profit pool in its devices such that Intel could conceivably extract at least some incremental value.

A Deep Dive Into High-Volume Foundry Economics

Our analysis of the economics of such a large-scale foundry deal from Intel's perspective suggests that, at least from an earnings basis, it could be attractive.

Given the price-sensitive consumer-focused nature of mobility, it is unlikely that these markets can support "value-pricing" to the extent that pure strategic foundry can. Thus, part of the Intel bear case on such an offering focuses on the inherent gross margin compression that could result. In fact, we believe that high volume foundry would be gross-margin dilutive for Intel. Using Apple as a proxy, we (very roughly!) estimate gross margins for such a business in the 40%-ish range (below Intel's current ~60% margins) (see Exhibit 140 through Exhibit 142).

However, we do not believe that such a foundry business would necessarily be dilutive to Intel's operating margins, as we believe the incremental opex burden associated with it should be relatively lighter. As a result, we believe the EPS upside from a foundry business for a customer the size and with the characteristics of Apple could be reasonably attractive (say, $0.30+/share) (see Exhibit 143 and Exhibit 144).

Exhibit 140 We Estimate (Very Roughly) That a Quad-Core 14nm AX Processor Might Be on the Order of 70mm2…

Processor	# Cores	Node (nm)	Die Size (mm2)	size/core (mm2)
A4	1	45	53.0	53.0
A5	2	45	122.2	61.1
Total Die Size Increase				130.6%
Die size increase from # cores				100.0%
Die size increase from increase in performance				**15.3%**
A5	2	45	122.2	61.1
A5 (new iPad 2)	2	32	73.3	36.7
Die Size Reduction due to smaller node				**-40%**

Estimate AX 14nm die size

Processor	# Cores	Node (nm)	Die Size (mm2)	size/core (mm2)
A5 (new iPad 2)	2	32	73.3	36.7
Die Size Reduction to 22nm (one node)			-40%	
AX (22nm, dual core)	2	22	44.0	22.0
Die size increase from move to quad-core			100%	
AX (22nm, quad-core)	4	22	88.0	22.0
Die size Increase from performance improvement			15.3%	
AX (22nm, quad-core, increased performance)			101.4	25.4
Die Size Reduction to 14nm (one node)	4	14	-40.0%	
Die size Increase from performance improvement			15.3%	
AX (14nm, quad-core, increased performance)	**4**	**14**	**70.2**	**17.5**

Source: Bernstein estimates and analysis.

Exhibit 141 **...and Require ~30K 300mm Wafers per Month (e.g., a Large Leading-Edge Fab)**

Wafer Diameter (mm2)	300
Wafer Area (mm2)	70,686
Edge Exclusion	5%
Usable Area	67,152
Estimated AAPL die size (mm2)	70
Gross Dies/Wafer	957
Yield Assumption	90%
Good Dies/Wafer	861
iOS Device Demand, 2015 (M units)	325.2
Wafers needed per year	377,554
Wafers needed per month	**31,463**

Source: Bernstein estimates and analysis.

Exhibit 142 **On These Base-Case Assumptions for Units, ASPs and Costs, We Estimate Intel Might Earn a Foundry Margin of ~40% from Apple Volume**

Wafer Diameter (mm2)	300
Wafer Area (mm2)	70,686
Edge Exclusion	5%
Usable Area	67,152
Current Average Intel Die Size (mm2)	154
Average ASP/Die (Q112)	$119
Average Dies/Wafer	435
Average ASP/Wafer ($K)	$52
MPU Gross Margin	75%
Average Cost/Wafer ($K) (2012)	**$13**
Wafer Cost Added/year	3.0%
Estimated Wafer Cost (2015)	**$14**
AAPL Dies/Wafer	957
ASP/Die	$25
AAPL Revenue/Wafer ($K)	**$24**
Intel Foundry Gross Margin	**40.8%**

Source: Bernstein estimates and analysis.

Exhibit 143 **We Believe Foundry Net Margins for Intel Could Be in the Ballpark of 20% or More, Not Hugely Lower Than the Company's Core Business (Although ROIC Will Be Lower)**

Annual AAPL Units (M)	325	325	325	
AAPL ASP	$25	$25	$25	
Intel Market Share at AAPL	50%	80%	100%	
INTC Foundry Revenue ($B)	$4.1	$6.5	$8.1	
INTC Foundry Gross Margin	40.8%	40.8%	40.8%	
INTC Foundry Gross Profit ($B)	$1.7	$2.7	$3.3	
R&D ($B)	$0.5	$0.8	$1.0	
%	12.0%	12.0%	12.0%	Assume 1.5x TSMC R&D
SG&A ($B)	$0.041	$0.065	$0.081	
%	1.0%	1.0%	1.0%	Assume a point or so (minimal incremental)
INTC Foundry Operating Profit ($B)	$1.1	$1.8	$2.3	
%	27.8%	27.8%	27.8%	
Tax Rate	28.5%	28.5%	28.5%	
INTC Foundry Net Income ($B)	$0.8	$1.3	$1.6	
INTC Foundry Net Margin	19.8%	19.8%	19.8%	
Diluted Shares	4900	4900	4900	Current SCB 2014 estimate
EPS Impact	**$0.16**	**$0.26**	**$0.33**	

Source: Bernstein estimates and analysis.

Exhibit 144 **Intel EPS Accretion from an Apple Foundry Relationship Could Be Material, Particularly If Intel Can Be Successful in Driving Higher ASPs (e.g., Getting Paid for Additional Value Add)**

INTC EPS Sensitivity to AAPL Foundry Volume (Assumes 100% Share)

		AAPL Unit Demand (M)					
		275	300	325	350	375	400
AAPL ASP	$15	-$0.07	-$0.08	-$0.08	-$0.09	-$0.10	-$0.10
	$20	$0.10	$0.11	$0.12	$0.13	$0.14	$0.15
	$25	$0.28	$0.30	$0.33	$0.35	$0.38	$0.41
	$30	$0.45	$0.49	$0.54	$0.58	$0.62	$0.66
	$35	$0.63	$0.68	$0.74	$0.80	$0.86	$0.91

Note: SCB 2014 INTC EPS estimate is $2.97.

Source: Bernstein estimates and analysis.

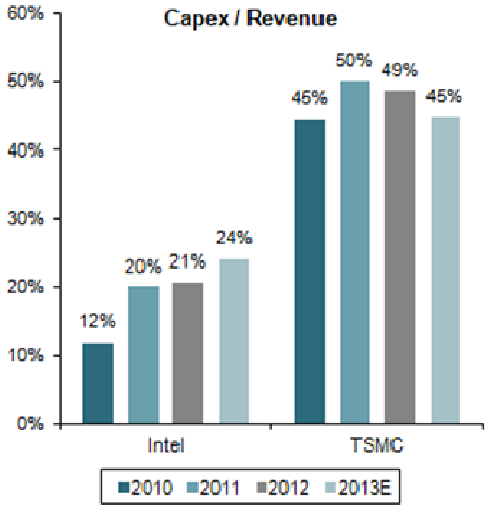
However, from a capital intensity basis, high-volume foundry is likely to be troubling for Intel. Apple is big enough that Intel would have to likely build greenfield capacity (Apple is capable of filling a fab by itself). In such a scenario, we believe a foundry deal of this size would have an ROIC perhaps a third of what Intel is used to, with our (rough) math above implying a third or less profit per wafer, and thus ~3x the capex spend to earn a dollar of profit, versus Intel's current core business (see Exhibit 145). Economics of this sort should not be surprising, and can be easily seen in TSMC's financials today given the company spends more than 50% of its revenue on capex (see Exhibit 146). But, they should be of concern for investors already worried about rising capital intensity and impact on cash flow for Intel.

Exhibit 145 **We Believe Intel's Profit Generation on a High-Volume Foundry Wafer Would Be Significantly Lower Than Its Current Core Business**

	Revenue / Wafer ($K)	Gross Profit / Wafer ($K)
Intel Volume	$52	$38
Foundry Volume	$24	$10

Source: Bernstein estimates and analysis.

Exhibit 146 **Intel's Capex Intensity Is Much Lower Than TSMC's**

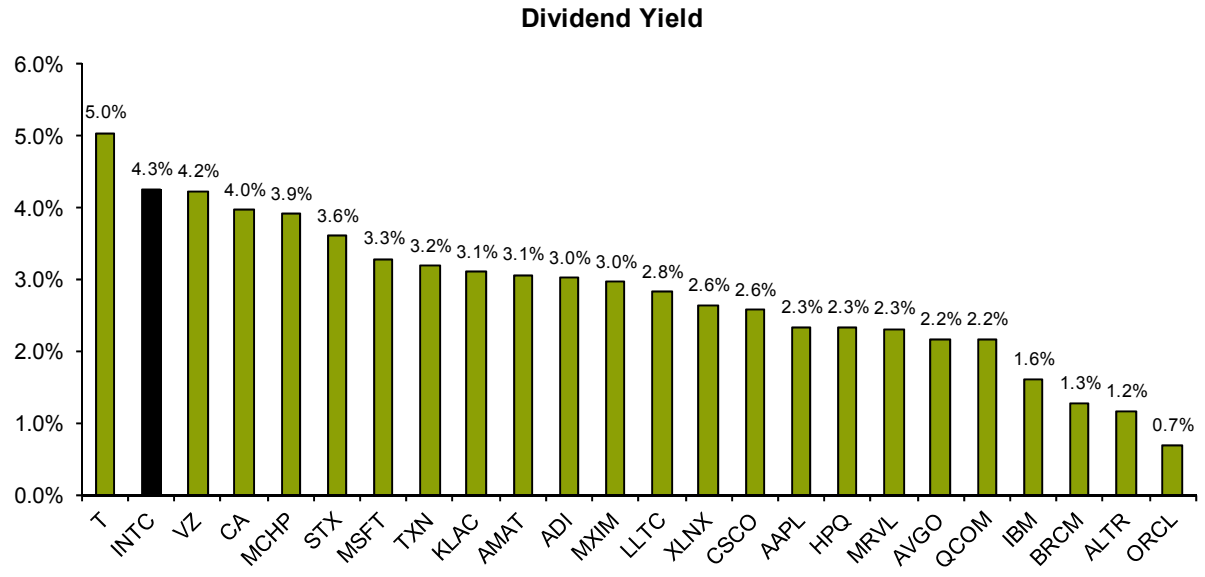


Source: Gartner, Strategy Analytics and Bernstein estimates and analysis.

Greatly Increasing Investment in the Wake of a Slowing Market May Pressure Cash Return, Long a Point of Stability for Intel's Stock

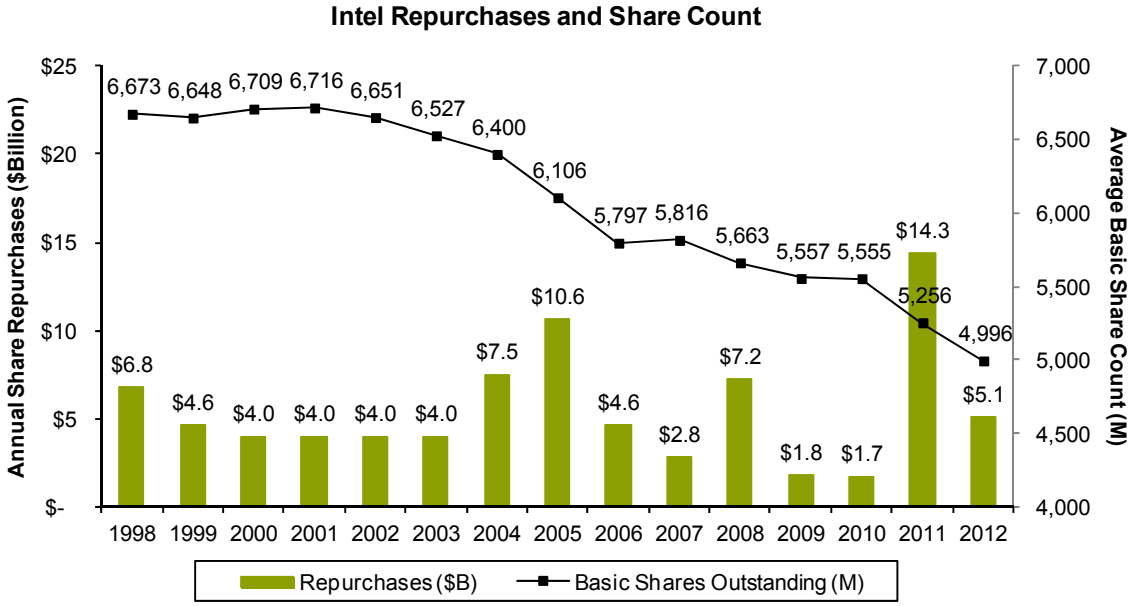
Many investors take comfort in Intel's cash return, with a >4% dividend yield and a history of buybacks (indeed, this is the greatest source of pushback to our underperform thesis; no one has yet really tried to argue with us on the math). And indeed, the company has one of the higher yields available in technology today, and has been diligent in recent years in reducing share count through repurchases (see Exhibit 147 and Exhibit 148).

Exhibit 147 **INTC Has One of the Highest Dividend Yields in the Space**



Source: Capital IQ and Bernstein analysis.

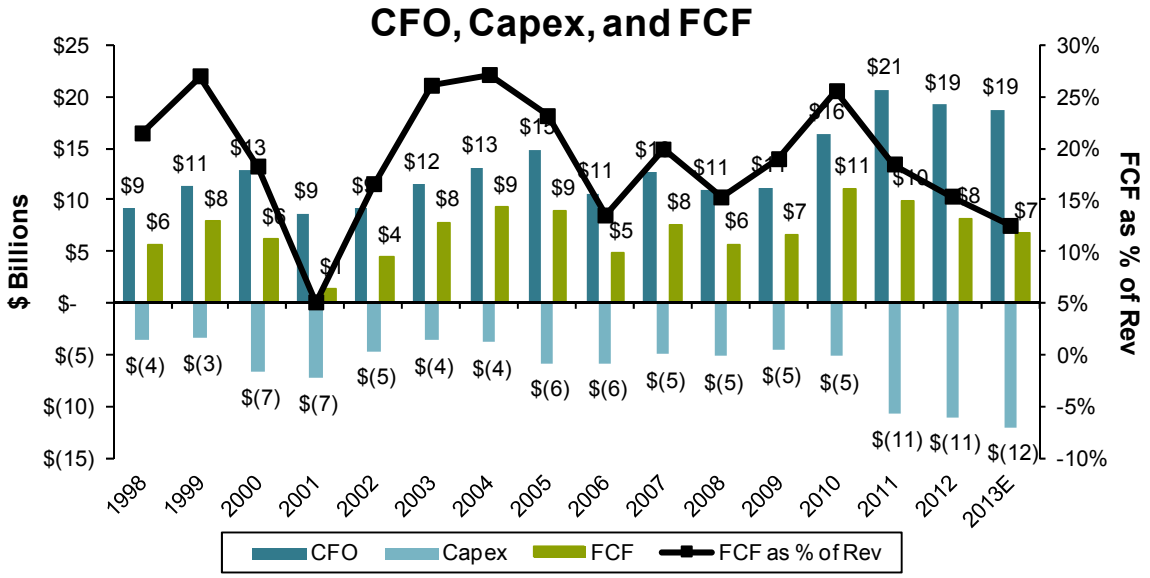
Exhibit 148 **Intel Has Repurchased More Than $80 Billion in Stock Since 1998 and Brought Share Count Down by About 25%**



Source: Corporate reports and Bernstein analysis.

However, efforts to further extend Intel's process gap versus the competition have greatly accelerated capex requirements; coupled with stagnation in core markets free cash flow has come under pressure in the last few years (see Exhibit 149).

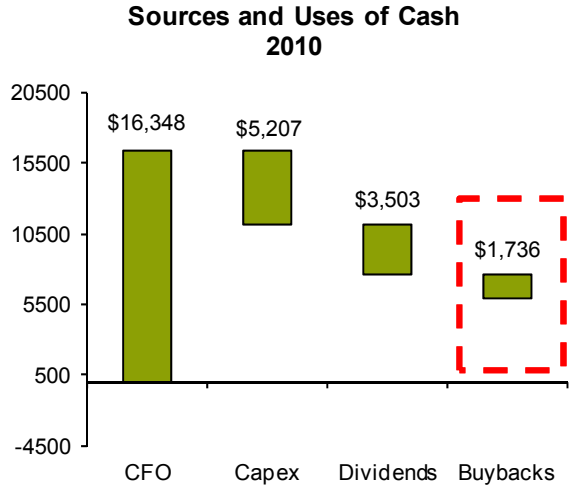
Exhibit 149 Increasing Capex and a Stagnating Demand Environment Is Pressuring Intel's Free Cash Flow



Source: Corporate reports and Bernstein analysis.

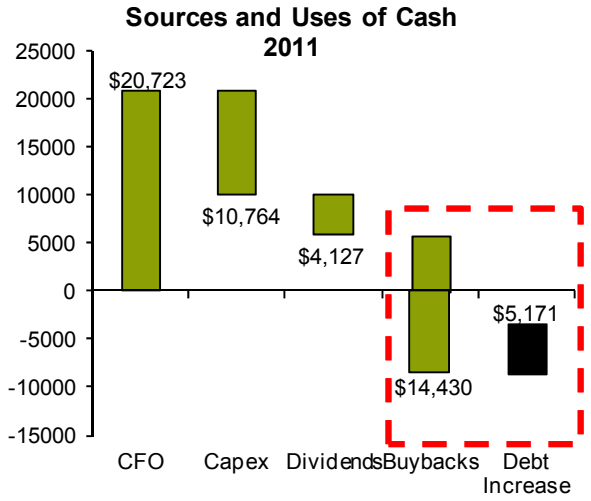
Additionally, Intel has resorted to borrowing to fund buybacks for the last two years (see Exhibit 150 through Exhibit 152). However, while we believe Intel's cash flow from operations remains sufficient to fund capex and dividends, it is reaching the point where buybacks can no longer be sufficiently covered by the company's cash generation. Further balance sheet leverage (whether by draining cash on hand or more borrowing) will now be a necessity to fund buybacks of any substantial magnitude (see Exhibit 153).

Exhibit 150 In 2010, Cash Flow from Operations More Than Covered Capex, Dividends and Share Buybacks



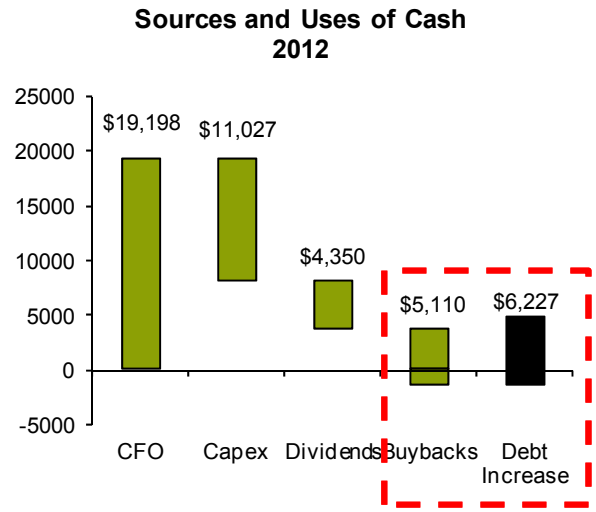
Source: Corporate reports and Bernstein analysis.

Exhibit 151 In 2011, Intel Funded Excess Buybacks Through Borrowing…



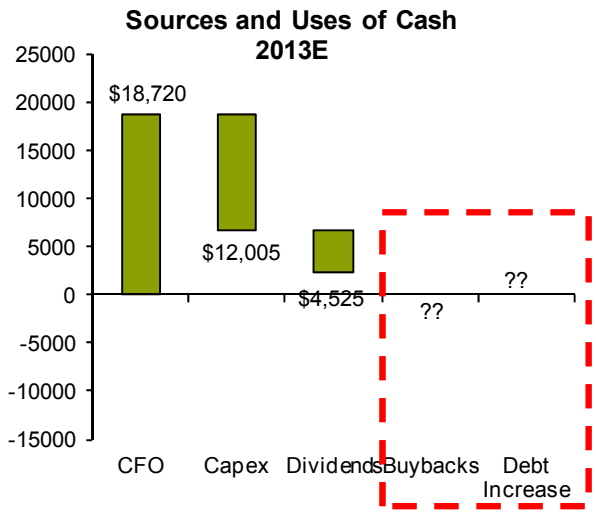
Source: Corporate reports and Bernstein analysis.

Exhibit 152 ...a Trend That Continued in 2012



Source: Corporate reports and Bernstein analysis.

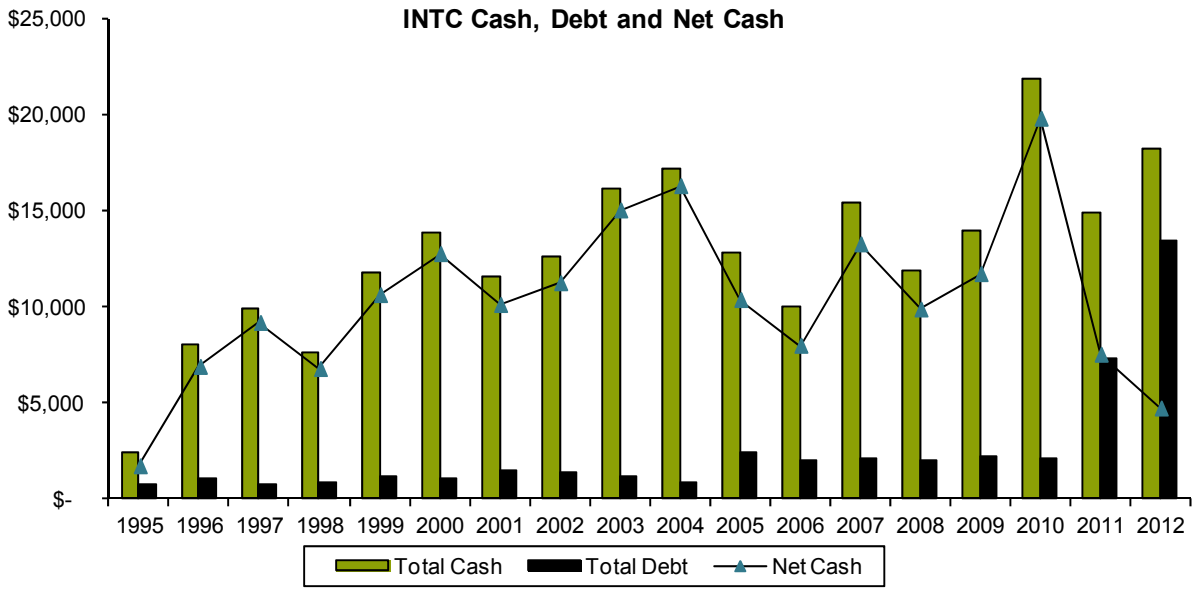
Exhibit 153 Further Leverage (Either Draining Cash on Hand, or Borrowing) Will Be Needed to Fund Buybacks in 2013 and Beyond at Current Demand and Capex Levels



Source: Corporate reports and Bernstein estimates and analysis.

While Intel's pristine credit rating has enabled it to borrow funds at extremely attractive rates, leverage works best when a company is growing (as Intel is not). And, borrowing to fuel buybacks has reduced net cash balances to <$5 billion (including trading assets and marketable long-term securities), the lowest level since 1995, and a stark contrast from only a few years ago when net cash exceeded $20 billion (see Exhibit 154).

Exhibit 154 Intel's Cash Position Has Declined, With Net Cash Levels at 10-Year Lows



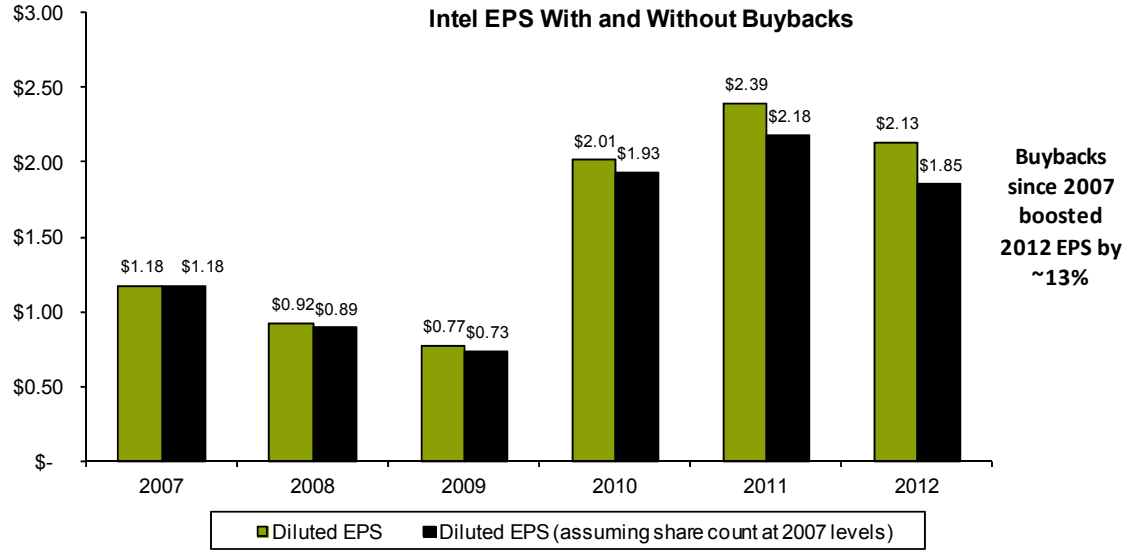
Note: INTC gross and net cash includes cash and cash equivalents, STI, and trading assets.

Source: Corporate reports and Bernstein analysis.

One of the ultimate bear theses on Intel's stock involves a significant cut to cash return (such as a reduction in the dividend). While we do not forecast anything as severe as a cut to the dividend at this point, it is not *quite* as laughable an idea as it might have been a few years ago. And certainly, we believe a plausible case can (at a minimum) be made for the pace of cash return increases to slow versus history given (absent a large pickup in Intel's top line) buybacks must by necessity be funded by increasing leverage, and dividend "headroom" appears more limited today (with low cash dividend coverage, high yield, and payouts currently well above company targets).

Intel's free cash flow currently appears (to us) sufficient to fund capital needs and the current dividend (though the gap has been closing in recent years). We expect further share buybacks will therefore need to be accompanied by increasing leverage, whether via draining cash on hand, or more borrowing. While Intel certainly has more capability to take on debt, levering a tremendously capital-heavy business in a cyclical environment is not sustainable forever, particularly in the absence of growth. We note that share buybacks have fueled a non-trivial amount of EPS growth over the last few years (see Exhibit 155), and it is likely the pace of buybacks will slow going forward.

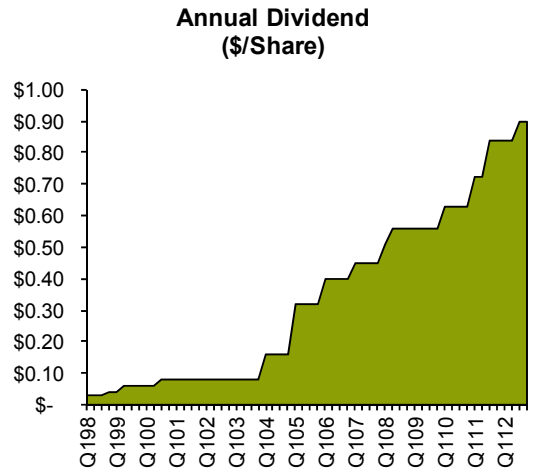
Exhibit 155 Buybacks Since 2007 Have Boosted Intel's EPS by 13%



Source: Corporate reports and Bernstein analysis.

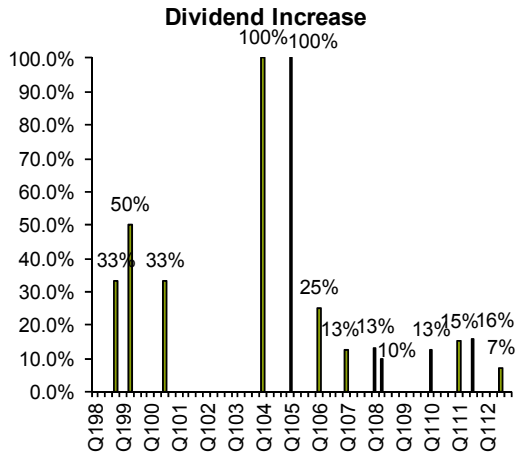
Intel has been fairly consistent at raising its dividend over the years (see Exhibit 156), but recently the magnitude of increases has slowed; the latest increase (to $0.90 per share per year, in 3Q:12) was a 7% raise, the smallest dividend increase in Intel's history (see Exhibit 157).

Exhibit 156 While Intel Has Consistently Increased Their Dividend…



Source: Corporate reports and Bernstein analysis.

Exhibit 157 …the Latest Increase Was the Smallest in Company History



Source: Corporate reports and Bernstein analysis.

Given relatively low dividend coverage versus peers, a current high yield, and a payout ratio (at >50% of FCF) that is above current targets (40%), we believe a continued slower pace of dividend increases is possible versus what investors have enjoyed in the past, under our current forecasts for the company's growth. We are concerned that a slowing of cash return growth is the best that investors can hope for; of course if the core business deteriorates even this could prove optimistic.

The End Game Could Look Rosy, But the Journey Could Be Painful

Longer-Term Accelerating M(o)ore Investments May Be a Winning Strategy, But the Journey Is Likely to Be Painful

Keep in mind that, while we believe the intensified capex and shifts to Intel's business model that are forthcoming as the industry moves more to a power-centric focus will be painful for Intel's stock, we *do not* believe the company is doing anything wrong. Quite the contrary, the other option (dialing back on capex and technology spending, and —for now — accelerating further cash return) is likely a recipe for slow death as the company loses the one staggering advantage it possesses, namely manufacturing prowess. Rather, we believe the company is preparing to take necessary pain today for the prospect of a brighter future tomorrow (indeed, this is the way a company should be run).

One can postulate an end game (say, five years or more out) in which Intel still owns whatever is left of the PC market (whether growing, stagnant, or shrinking). On top of that, it could (eventually) be a formidable player in new mobile markets as the industry refocuses on power efficiency, with technology leadership allowing a performance/power envelope that could conceivably be very superior to offerings from competitors at that time (particularly if the process migration at the foundries and, hence, for the ARM camp does not go as smoothly as hoped). And, Intel could potentially leverage its Infineon assets, finally delivering integrated 3G and LTE that could, perhaps, help it secure a leading position in a smartphone market of a billion+ units.

But, massive capex and investment will be necessary to craft a company capable of dominating these markets, but which (in a bit of a chicken-or-the- egg manner) also requires that dominance (e.g., significant unit share) to fill the capacity the investments will put into place. 450mm costs have only just begun to ramp ($2 billion for the pilot line this year is only the beginning) and a 450mm production fab, when it comes, will dwarf anything we've seen so far (with even larger revenue needed to fill it). Improvements to Atom may bring Windows 8 tablets to a successful point in the market but could backfire — tablets already

appear to be significantly cannibalistic, and we fail to see how making tablets better will limit their cannibalistic tendencies.

We believe one could look back in five years or more, and complement the path Intel chose; future Intel (and future Intel stock) could be a phenomenal story at that point. But, we believe the journey is likely to be much less forgiving for the stock until we arrive.

From Friend to Enemy? How Mourning Moore's Law Will Change the Foundry Landscape

Highlights

Since its birth two to three decades ago, the foundry industry, together with the fabless industry that subsequently emerged, has clearly demonstrated the merits of its business model. By freeing customers from the heavy burden of manufacturing assets, foundries allow IC designers to creatively put the benefits of Moore's Law to every possible application. Despite the fact that the foundry industry also felt the pressure of cost escalation in advancing Moores's Law, the rising cost burden actually helped the industry if we take a very long-term view. Many IDMs found themselves unable to achieve sufficient scale in order to be cost competitive in new technologies, and hence turned to the foundries for help. Over time, foundries captured more shares from IDMs, and as some of the foundry companies grew bigger, the benefit of scale became more prominent. Somewhat counter-intuitively, we conclude that the cost pressure actually has been the foundry's friend.

The industry, in particular its leader TSMC, is further propelled to an even higher altitude as semiconductor growth has shifted from PCs to mobile devices in recent years. The combination of foundries and fabless companies successfully captured the mobile growth and trumped the IDMs. By 2011, a quarter of the semiconductor industry value had shifted to the fabless companies.

But can this situation be sustained? We indeed see challenges. Once a friend of the foundry industry, the cost increase has however risen to a point that we can arguably begin to mourn the slow death of the economy of Moore's Law. Even TSMC is feeling the pressure, let alone the small foundries.

Meanwhile, facing the rapid shift to mobile devices, Intel has no choice but to mount an attack on the mobile market. Its prior attempts unfortunately were unable to gain it a meaningful share in the market. Undeterred by these setbacks, Intel continues to make slow but steady progress in technologies and put up a bigger fight by spending record-high capex and accelerating its mobile SoC development at an unprecedented pace. If Intel continues down this road, it is expected to command a lead in process technology versus TSMC and Samsung in the next two to three years.

Considering the technology leadership, we think Intel is a credible contender for Apple's foundry business. It likely would take some time for Intel to win the business but Apple's appetite for differentiated technologies and comfortable profit margin make this possibility very conceivable. Should Intel be successful either as a mobile chipset supplier or a foundry player, it would be negative to either TSMC's customers or to TSMC itself.

As for Samsung, since the high cost of advanced technologies casts doubt on the growth prospects of the memory business, the company is moving into logic IC with rising intensity. Extrapolating from the current trajectory, we find Samsung likely would become more self-sufficient in logic ICs for the next few years, leaving smaller demand for TSMC's customers.

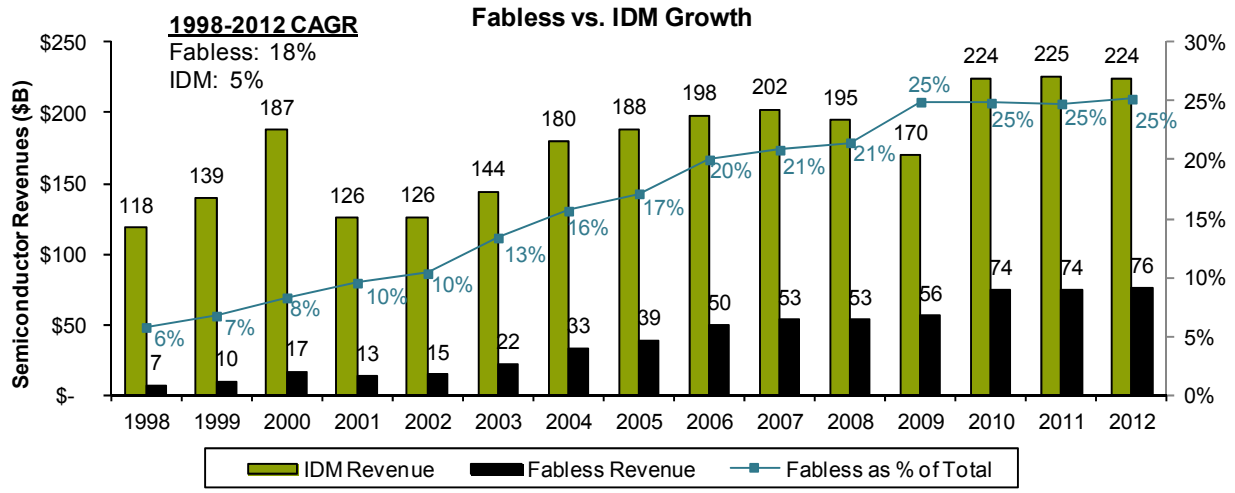
In the case of TSMC, we continue to forecast margin deterioration because competition pressure from Intel and Samsung hinder its ability to transfer the cost of leading technology development to customers. We remain conservative on TSMC, especially as it is granted a high valuation right now. We rate TSMC market-perform with a target price of NT$107.

Over the Past Two to Three Decades, Foundry + Fabless Growth Clearly Trumped IDMs

From the early beginnings of the semiconductor industry in the 1970s, the large semiconductor companies owned both design and manufacturing capabilities internally and are hence called the Integrated Device Manufacturers (IDMs). In the 1980s, the "foundry + fabless" business model emerged, which separates the design and manufacturing business. Companies dedicated to manufacturing, or foundries as they are called, own and manage fabrication plants and can work with any design company (fabless). This model frees the design companies from the burden of high capital expenditure without building fabrication plants, thus lowers small fabless companies' entry barrier and enables them to focus on product development. Contrasting the two models, the IDMs achieve efficiency through vertical integration, and the foundries and fabless benefit from economies of scale and flexibility.[3]

While both models have their own merits, the combination of foundry and fabless has clearly trumped IDMs. From 1998 to 2012, the fabless companies have outgrown the IDMs by 4x; fabless collectively grew 18% per year on average, whereas IDMs only expanded 5% every year (see Exhibit 158). Foundries and their fabless customers are now indisputably a very important force in this industry, with fabless taking 25% of the market share in 2012 (see Exhibit 159).

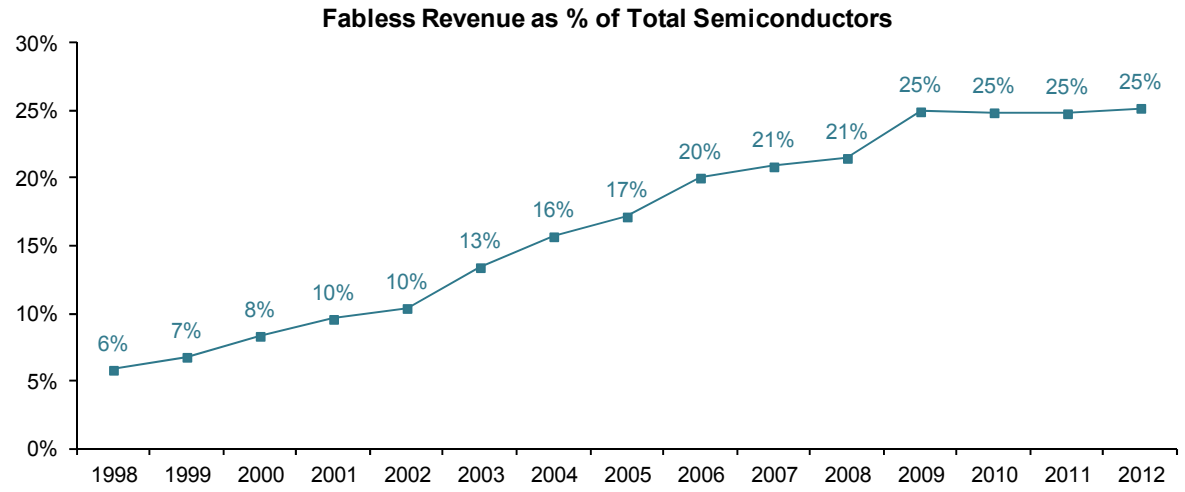
Exhibit 158 **The Fabless Industry Has Grown at an 18% CAGR Since 1998, Compared With IDM Growth of 5%**



Source: Global Semiconductor Alliance, IC Insights, WSTS and Bernstein U.S. Semiconductors team.

[3] See our prior call at **Foundry: Is the Foundry Model Broken? We Don't Think So**.

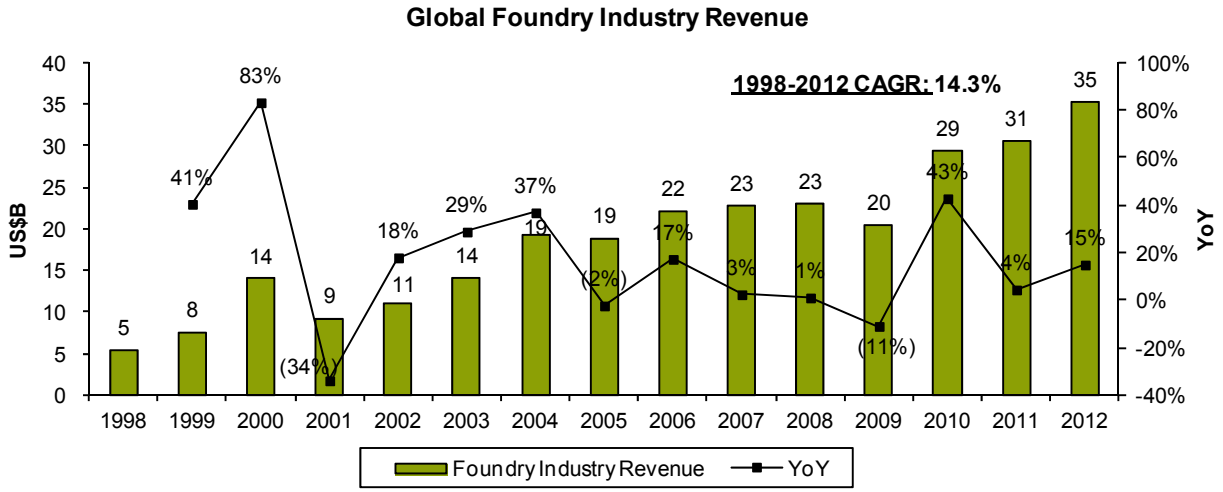
Exhibit 159 **Fabless Companies Have Increased in Market Share from 6% to 25%**



Source: Global Semiconductor Alliance, IC Insights, WSTS and Bernstein U.S. Semiconductors team.

Fundamentally, by sharing assets across a diverse customer base, foundry has lowered demand volatility and hence enjoys better asset utilization as well as cost savings compared to IDMs. The large demand aggregated in this business model also enlarges foundry's scale and drives its cost competitiveness further. Most importantly, freeing up chip designers from the burden of heavy manufacturing facilities, foundry greatly lowers the barrier of innovations. Designers creatively have put technologies to every possible use, fully reaping the benefits of Moore's Law in cost, performance and power efficiency. Sharing customers' success, the foundry industry also benefits from Moore's Law and has quickly grown over 6x during the past 15 years (see Exhibit 160).

Exhibit 160 **Foundry Also Benefit from Moore's Law and Quickly Grew Over 6x During the Past 15 Years**



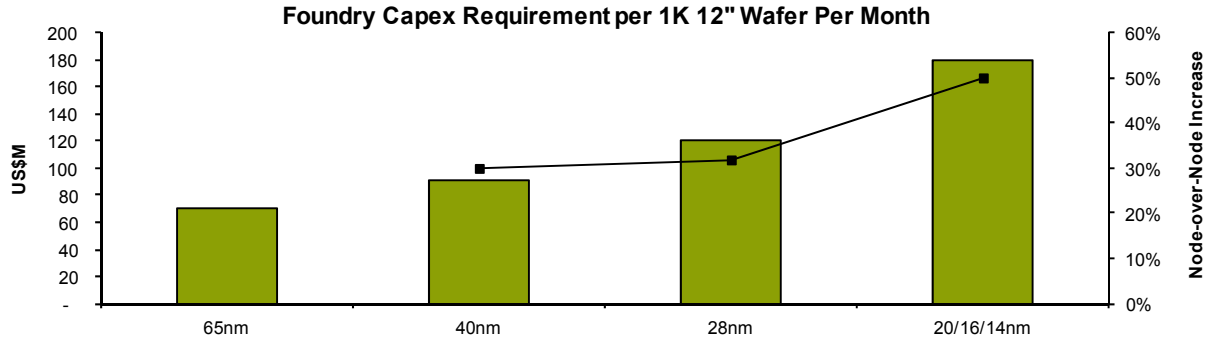
Source: Gartner and Bernstein estimates and analysis.

As We Mourn the Slow Death of Moore's Law and Discuss the Consequences, the Cost Escalation in Technologies, Ironically, Has Been a Key Contributor to Foundry's Growth in the Past

Cost hikes demanded by new technologies are not new to this industry (see Exhibit 161). In fact, it has pressured most IDMs (e.g., TI, Renesas, NXP, Freescale, etc.) to stop investment, which is needed to keep up with Moore's Law. This "fab-lite" trend at IDMs, together with the boom of fabless companies, has brought more than sufficient demand to offset the escalating cost burden. Therefore, somewhat counter-intuitively, the cost increase has been helping the foundry industry grow. Not until recently has the cost escalation reached the point where even leading foundry and fabless begin to feel the pain.

As other IDMs depend on foundry to varying degrees for manufacturing service, Intel and Samsung have become the only two "pure" IDMs left currently. The standardization of memory and CPU chips helps them accumulate sufficient scale to thrive with the IDM model under cost pressure. Their technology leadership and solid execution further drives them to the dominant position in their respective markets and earn a great deal of money.

Exhibit 161 We Estimate Capex Requirement per Capacity Will Increase 50% from 28nm to 20nm and Grow Even Faster from 20nm to 14nm



Source: Bernstein estimates and analysis.

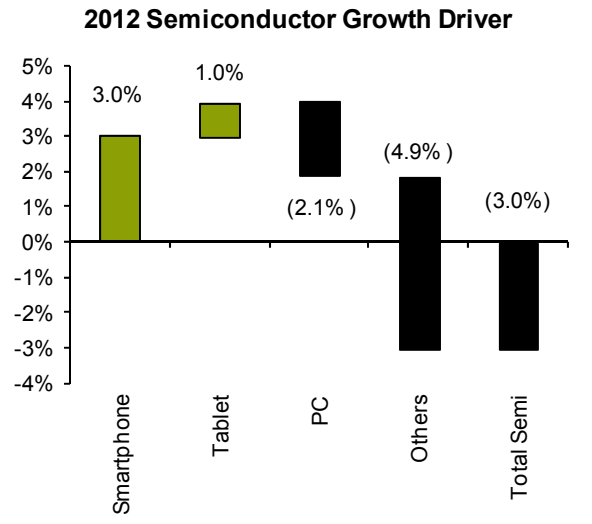
The Shift from PCs to Mobile Devices Further Elevates the Role of Foundries and Fabless in the Semiconductor Supply Chain

Another important trend in the semiconductor industry is the transition from PC to mobile applications. Started a few years ago, mobile devices have been replacing PCs as the main semiconductor growth driver. While semiconductor for mobile devices (smartphones and tablets) drove the industry growth by 3%, semiconductor for PCs shrank and resulted in a 3% decline for the whole industry (see Exhibit 162). Capturing this wave of growth, leading foundries, particularly TSMC, and mobile fabless players, such as Qualcomm and MediaTek, delivered growth that dwarfed their IDM rivals.

For example, in the past three years, we saw TSMC's revenue from communications double from NT$36 million in 1Q:10 to NT$71 million in 4Q:12. Contribution from communications, rising steadily from 39% to 54%, has clearly become the driving force of TSMC's revenue growth (see Exhibit 163). Collectively, the combined revenue of TSMC, Qualcomm and MediaTek grew 22% in 2012, while the IDMs, Intel, Texas Instruments and Freescale dropped by 3% (see Exhibit 164). Furthermore, it seems that investors also believe that foundry + fabless would continue to excel versus IDMs in the future, as shown in their market valuation: all three foundry/fabless companies grew in market capital while two of the three IDMs dropped (see Exhibit 165).

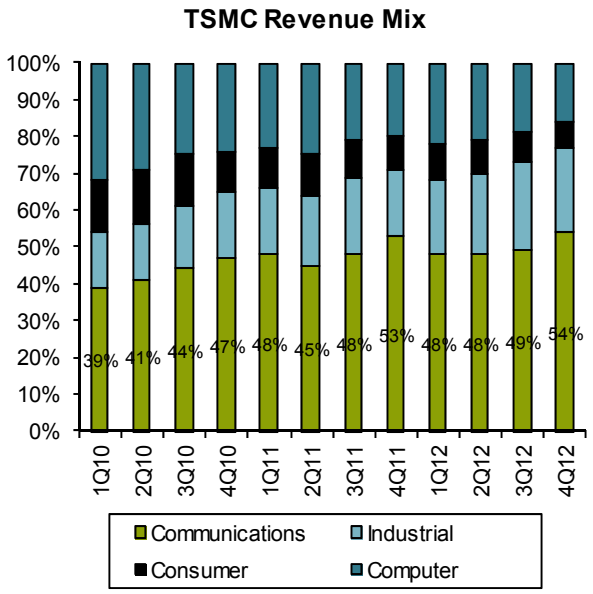
In summary, the shift of the focus from PCs to mobile applications has triggered a sea change in the industry. Foundries and fabless now command a position they never had before.

Exhibit 162 Mobile Devices Have Become the Semiconductor Growth Driver



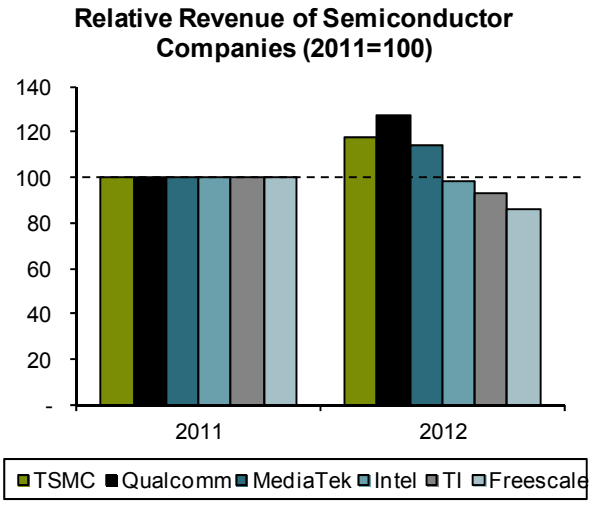
Source: Gartner and Bernstein analysis.

Exhibit 163 TSMC's Revenue Contribution from Communications Rose Steadily in the Past Two Years



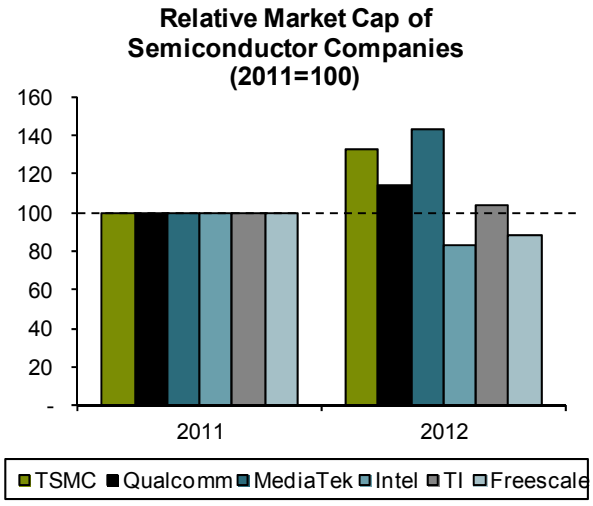
Source: Gartner and Bernstein analysis.

Exhibit 164 Fabless + Foundry Companies Grew in Revenue Compared With Their IDM Peers…



Source: Company data and Bernstein analysis.

Exhibit 165 …and in Market Cap Too



Source: Capital IQ and Bernstein analysis.

As Samsung Pushes into Logic and Intel Moves into Mobile Space, the Clash of the Three Titans (Intel, TSMC and Samsung) Is Inevitable

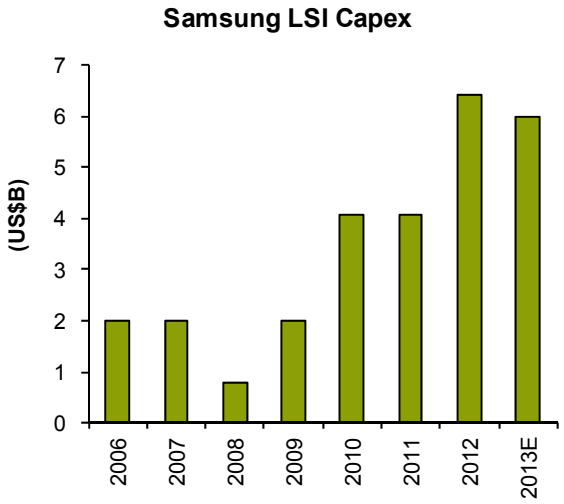
The success of foundries and fabless in the mobile space, on the other hand, also invites stronger competitors. Going forward, as slowing Moore's Law casts doubt on the growth trajectory of memory, Samsung's strategic push into logic IC has become apparent. The unprecedented shift from PC to mobile applications also forces Intel to move into power-centric technologies. The clash of the three titans is inevitable.

Node migration is slowing in memory too, which is causing lower bit growth and thus higher profitability (see **New NAND Paradigm** and **New DRAM Order**), further emboldening Samsung to invest more aggressively in logic. The rising investment in System LSI supports this view (see Exhibit 166).

Intel, despite the indisputable technology leadership and dominant market share in the performance-driven CPU segment, also faces great challenges now as the PC market declines. We believe that it has no choice but to leverage its core competitive advantages — technology leadership and manufacturing prowess — to make a strong push into mobile applications.

As the result, the collision of the three largest semiconductor companies in the world is unavoidable. This and the diminishing economic benefit from Moore's Law form the basis of our conservative thesis on TSMC in the long term.

Exhibit 166 **Samsung's Rising Investment in System LSI Supports the View that the Company Is Expanding into Logic IC Strategically**



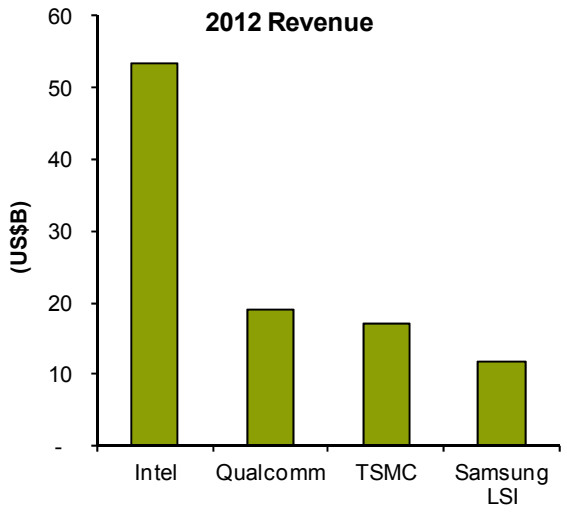
Note: Samsung's Logic capex pre-2010 is estimates from Bernstein Global Memories and Consumer Electronics Team.

Source: Bernstein Global Memories and Consumer Electronics Team.

Intel Accelerated the Development for Mobile SoC Products and Has Demonstrated Power Efficiency Comparable With Competing ARM-Based Chips

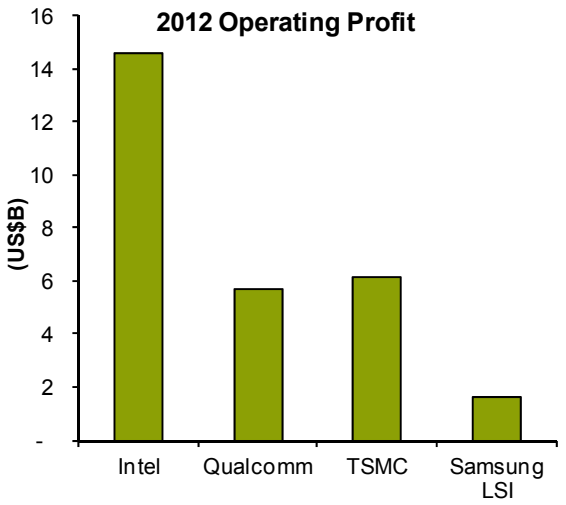
Facing this rapid sea change, the leader of IDMs, Intel, has no choice but to mount an attack on the mobile market. Intel is still the world largest semiconductor company, from both a revenue and an operating profits perspective (see Exhibit 167 and Exhibit 168). It is also the indisputable technology leader (see Exhibit 169). Leveraging these strengths, Intel has been striving to enter the mobile market. Intel is quickly lowering the power footprint of its SoC production by accelerating the pace of Moore's Law, accelerating the development for SoC products, and at the same time supercharging with its unprecedented capex in the industry. After a few failed attempts, Intel's latest mobile chips finally demonstrate comparable power efficiency with competing ARM-based chips made by TSMC.

Exhibit 167 Intel Is Still the Largest Semiconductor Company by Revenue…



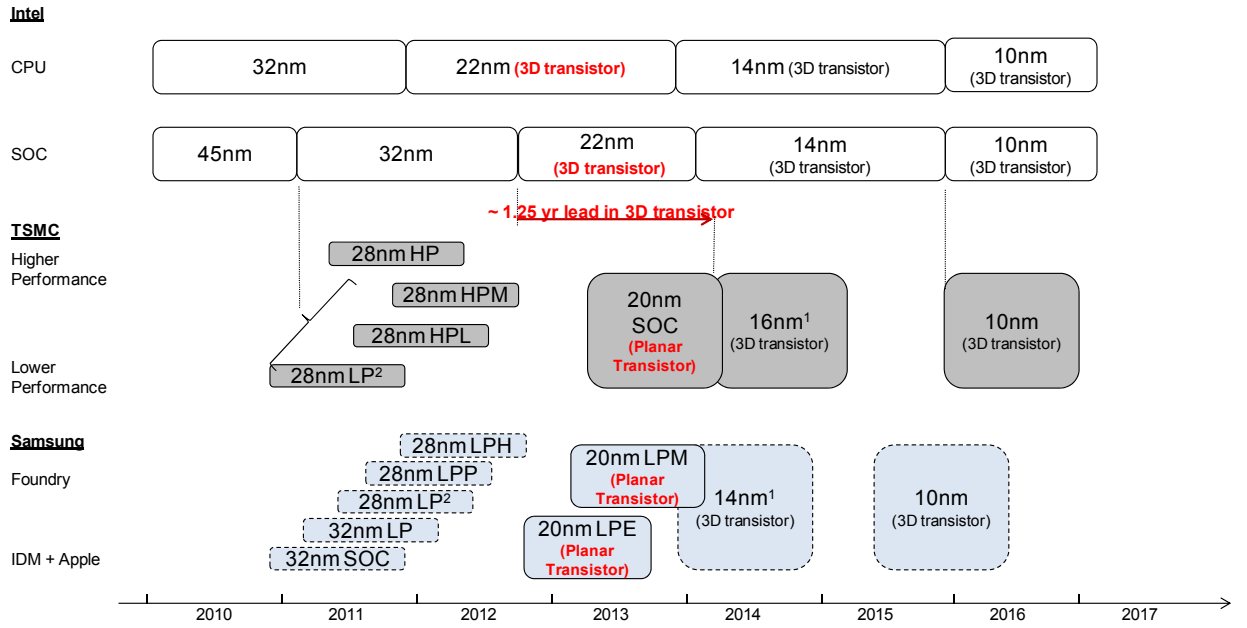
Source: Corporate data and Bernstein analysis.

Exhibit 168 …and by Profit



Source: Corporate data and Bernstein analysis.

Exhibit 169 Intel's Process Technology Is More Advanced Than TSMC's and Samsung's



Note: Dotted line refers to SCB estimate. Solid line is company reported. 1. TSMC's 16nm, GlobalFoundries' 14XM and Samsung's 14nm are all "3D transistor version of 20nm." They are similar technologies and deliver comparable performance. 2. Poly/SiON flavor

Source: Corporate data and Bernstein estimates and analysis.

Since 2011, Intel has launched several SoC processors in an attempt to enter the mobile market (see Exhibit 170). These have been largely unsuccessful in the commercial sense. In 2012, Intel's market share in smartphones was merely 0.2% and it is virtually non-existent in tablets in contrast to its domination in the PC space (see Exhibit 171).

Undeterred, Intel is maintaining a slow but steady progress in mobile technologies. It has put up a bigger fight by accelerating in mobile SoC development and planning an even bolder capex to extend its scale advantage. According to its plan, Intel will have three nodes (or two transitions, 32nm→22nm

and 22nm→14nm) in three years — much faster than the regular cadence of one transition every two years (see Exhibit 172 and Exhibit 173).

We believe that these efforts are gradually paying off. This is evidenced as Intel has narrowed the gap in power efficiency, which is viewed as the most critical technological drawback for Intel. The latest benchmark, from independent third parties, shows that the gap has indeed closed (see Exhibit 174 and Exhibit 175).[4]

Furthermore, Lenovo's latest flagship smartphone, K900, is running on Intel's 32nm Clover Trail+ (or Z2580) SoC. The handset delivers performance better than top-tier ARM-based phones, including Samsung's Galaxy S4 (see Exhibit 176 through Exhibit 178).

Following that, Intel's next tablet chipset, Bay Trail, is scheduled for holiday 2013 tablets, and its smartphone SoC, Merrifield, will be shipped to customers by the end of 2013[5] (see Exhibit 179). All this points to Intel's steady pace in the mobile market and the fact that the company is exerting pressure on TSMC's customers as well as TSMC itself.

Exhibit 170 Intel's Prior Generations of Mobile SoC

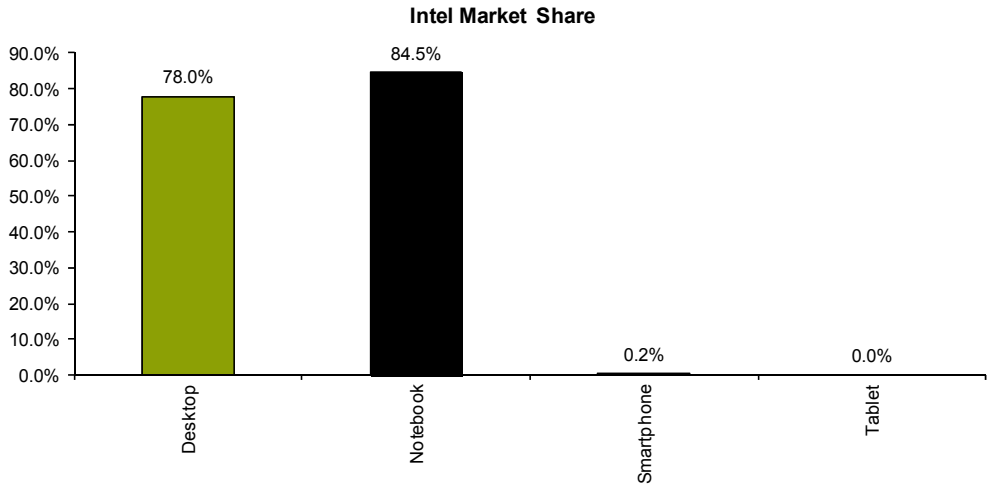
Category	SoC	Geometry	# of Cores
Smartphones	Moorestown	45 nm	1
	Medfield (Z2480, Z2460, Z2420)	32 nm	1
	Clover Trail+ (Z2580, Z2560, Z2520)	32 nm	2
	Merrifield	22 nm	?
Tablets	Oak Trail (Z670)	45 nm	1
	Clover Trail (Z2760)	32 nm	2
	Bay Trail	22 nm	4

Source: Corporate data, Bernstein U.S. Semiconductors team and Bernstein Asian Semiconductors team.

[4] Refer to our prior call for more details: **Global Semiconductors - An Update on The Silicon Wars: Where Do We Stand in the ARM vs. x86 Performance Fight?**

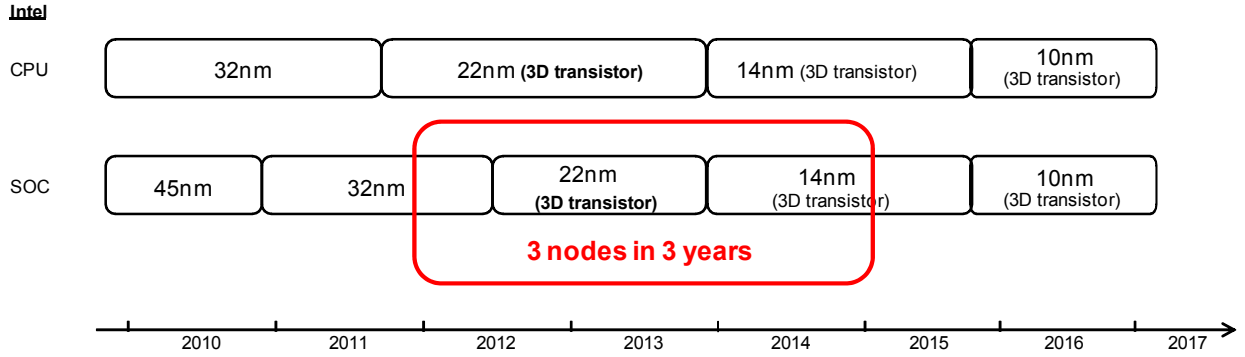
[5] See details at http://newsroom.intel.com/community/intel_newsroom/blog/2013/04/09/intel-developer-forum-transforming-computing-experiences-from-the-device-to-the-cloud.

Exhibit 171 **Intel's Current Market Share in Mobile Devices Is Tiny Compared With Its Dominating Position in PCs**



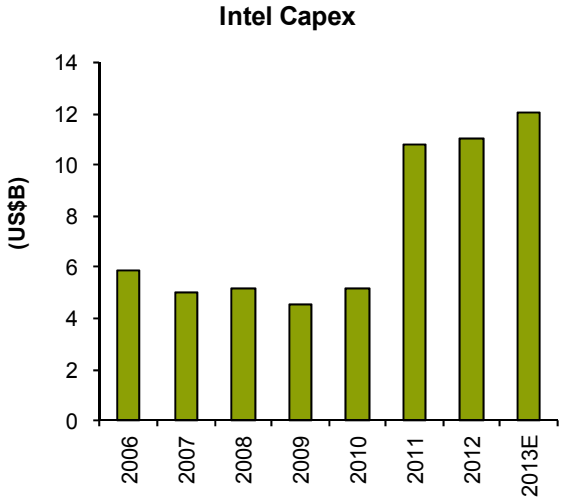
Source: Bernstein U.S. Semiconductors team.

Exhibit 172 **Intel Plans to Accelerate Its Mobile SoC Development**



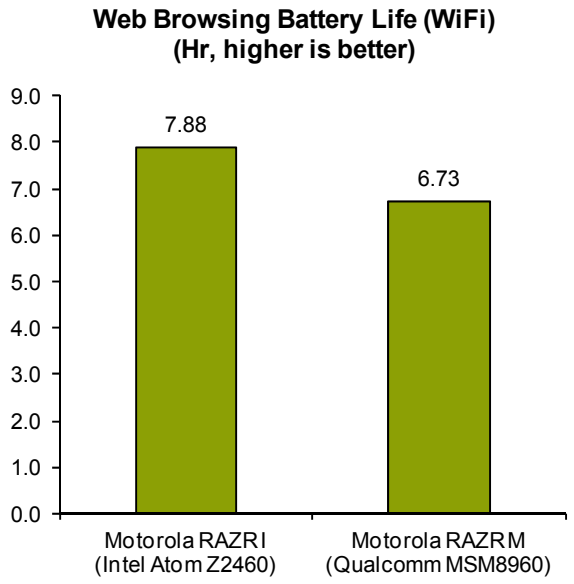
Source: Corporate data and Bernstein analysis.

Exhibit 173 **Intel Is Investing Unparalleled Capex Now**



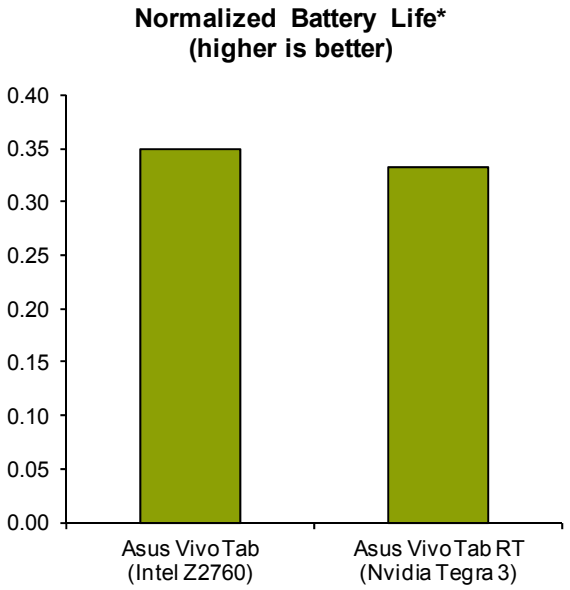
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 174 The Intel Chip for Mobile Phones Nicely Outperforms Qualcomm's in Battery Life…



Source: Anandtech and Bernstein research.

Exhibit 175 …and Its Chip for Tablet Performs on Par With Nvidia's Tegra 3



* Hours of web browsing using WiFi divided by battery capacity in watt-hour for VivoTab RT and Surface and hours of playing 720p video playback divided by battery capacity in watt-hour for VivoTab.

Source: Anandtech, corporate data and Bernstein research.

Exhibit 176 Lenovo Announced Its Latest Flagship Smartphone, K900, Featuring Intel's Clover Trail+ (or Z2580) Processor

Source: Lenovo.

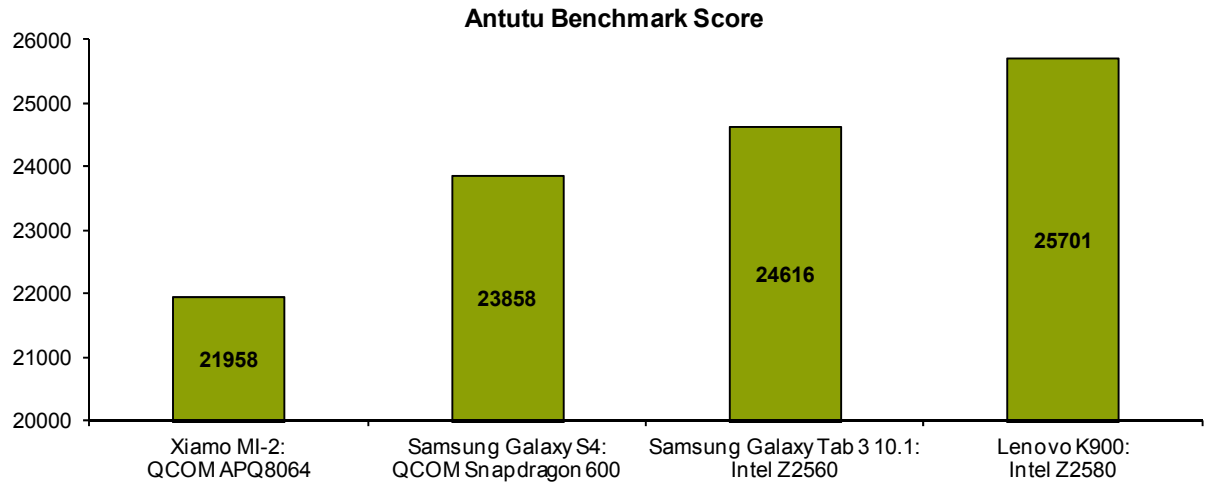
Exhibit 177 **Intel's Clover Trail+ (Z2580) Will Compete with Qualcomm's Snapdragon S4 Pro (APQ8064); Reportedly Lenovo's K900, Equipped with Z2580, Will Be Ready for Shipment in April 2013**

	Qualcomm	Intel
	APQ8064 (Snapdragon 600 Series)	Z2580 (Clover Trail+)
Mfg Geometry	28nm	32nm
Number of Cores	4	2 with HT[1]
Core	Krait	Atom
CPU Frequency	1.5GHz	2GHz
Integrated Comm Standards	None	None
GPU	Adreno 320	SGX544MP2
Video Playback	1080p	1080p
Representative Smartphones	LG Optimus G, HTC Butterfly, HTC J Butterfly, Sony Xperia Z, Sony Xperia ZL, Asus Padfone, Google Nexus 4, Xiaomi MI-2	Lenovo K900
Availability	Handset shipped in the market now	Reportedly handset shipped in the market in Apr, 2013

1 HT: Hyper-Threading; Intel's technology to allow a core to perform two jobs in parallel. A single-core with HT therefore performs comparably to two cores.

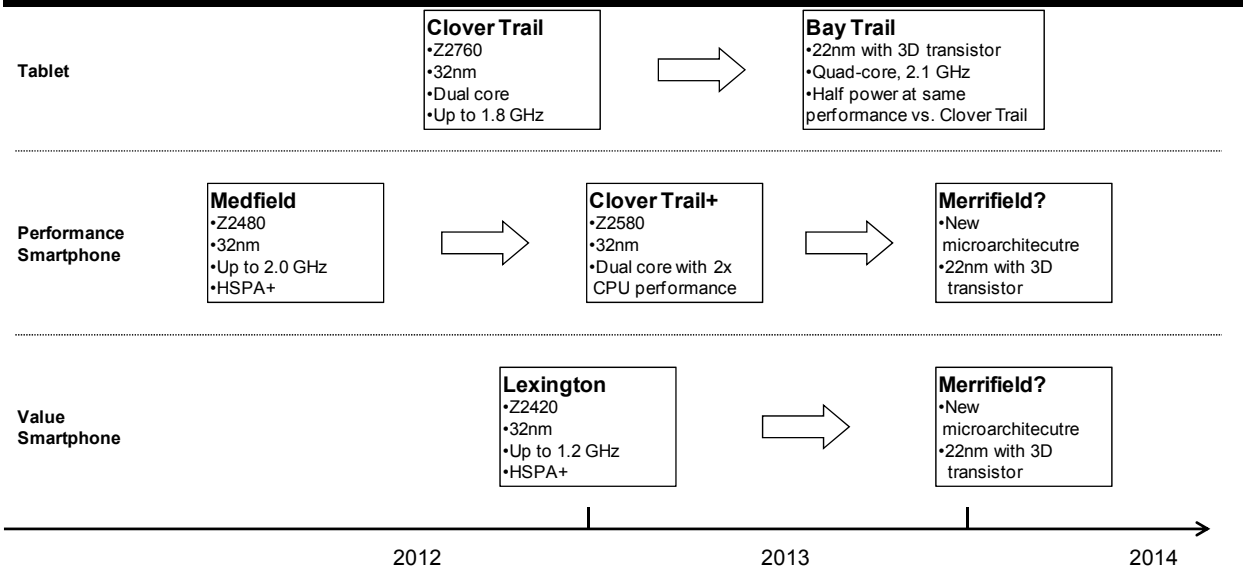
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 178 **Leaked Benchmark Shows That Intel's High-End Mobile Chips, Z2460 and Z2580, Deliver Better Performance Than QCOM's Snapdragon S4 Pro and 600**



Source: www.pcpop.com, www.fonearena.com, www.androidauthority.com/samsung-gt-p5200-benchmark-203496/, www.androidauthority.com/rumor-galaxy-tab-3-10-1-intel-atom-z2560-chip-212222/ and Bernstein analysis.

Exhibit 179 **Intel's SoC Roadmap Covers Both Smartphones and Tablets with Superior Performance**



Source: Corporate data and Bernstein estimates and analysis.

Intel's Mobile SoC Process Will Likely Command a Meaningful Lead Versus TSMC's and Samsung's in the Next Two to Three Years

Should Intel continue executing its roadmap, its mobile SoC process will command a meaningful lead versus TSMC's and Samsung's in the next two to three years. Later this year, Intel's mobile SoC will enter mass production with 22nm and 3D transistors. However, during the latest earnings conference, TSMC guided that 20nm (with only planar transistor) wouldn't begin revenue contribution until 2Q:14. This is surprising as this makes the transition from 28nm to 20nm take 2.75 years, the slowest transition in the past 10 years (see Exhibit 180). At the same time, TSMC guided its 16nm will come approximately one year after 20nm, which means TSMC's 3D transistor might not start revenue contribution until 2Q:15.

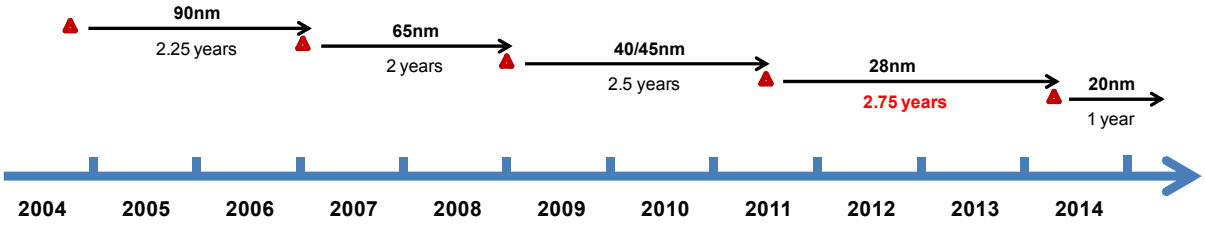
On the other hand, Intel is bringing 3D transistor, and the substantial improvement in performance (~20%) and power efficiency (~35%) (see Exhibit 181),[6] in 22nm mobile SoC this year. Intel's lead in 22/20nm is pressuring some foundries and fabless to "skip" 20nm and move to 16/14nm quickly as foundries (and Samsung) try to adopt 3D transistor quickly to level the playing field with Intel. Regardless, this still likely would leave a window of ~one year in which Intel would be the sole supplier of 3D transistor chips in the mobile market.

Further, somewhat deceptively, the foundries' 16/14nm process actually does not have finer geometry than 20nm. Their 16/14nm, in fact, is the "3D transistor" version of 20nm by converting planar transistor to 3D. It has no transistor density increase and thus no cost saving that all historical node transitions brought[7] (see Exhibit 182). Intel, on the contrary, likely will have a full shrink in its 14nm in late 2014. Intel hence could reverse its historical disadvantage in transistor density (see Exhibit 183) and potentially enjoy cost benefit versus foundries in this generation. This could potentially last another solid two years before both camps release 10nm in late 2016 (see Exhibit 184).

[6] More details on the next process nodes can be found in **Foundry: Beyond 28nm - What to Look for in 20nm and 16/14nm?**

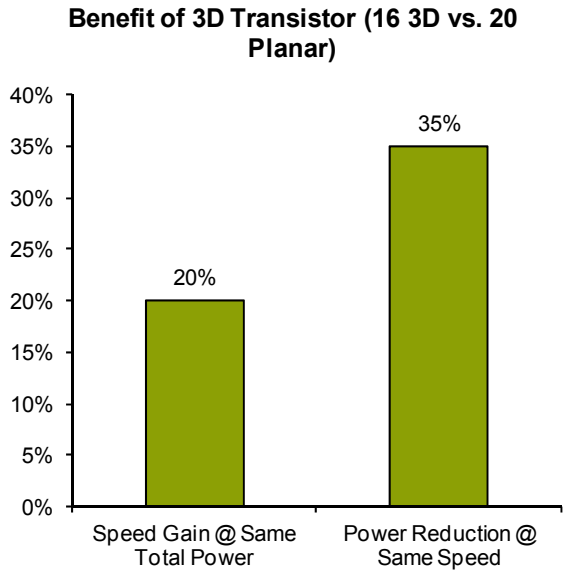
[7] More details could be found in **Foundry: 20nm = 16nm ~= 14nm? Demystifying the Designation of Technology Node**.

Exhibit 180 The Transition from 28nm to 20nm Would Be 2.75 Years, Longer than the Typical Cadence of ~Two Years



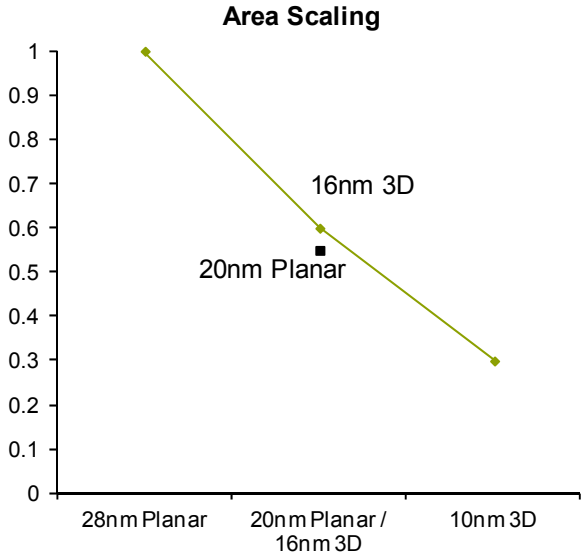
Source: Corporate data and Bernstein analysis.

Exhibit 181 3D Transistor Enables Substantial Advantage Over Planar Transistor in Performance and Power Consumption



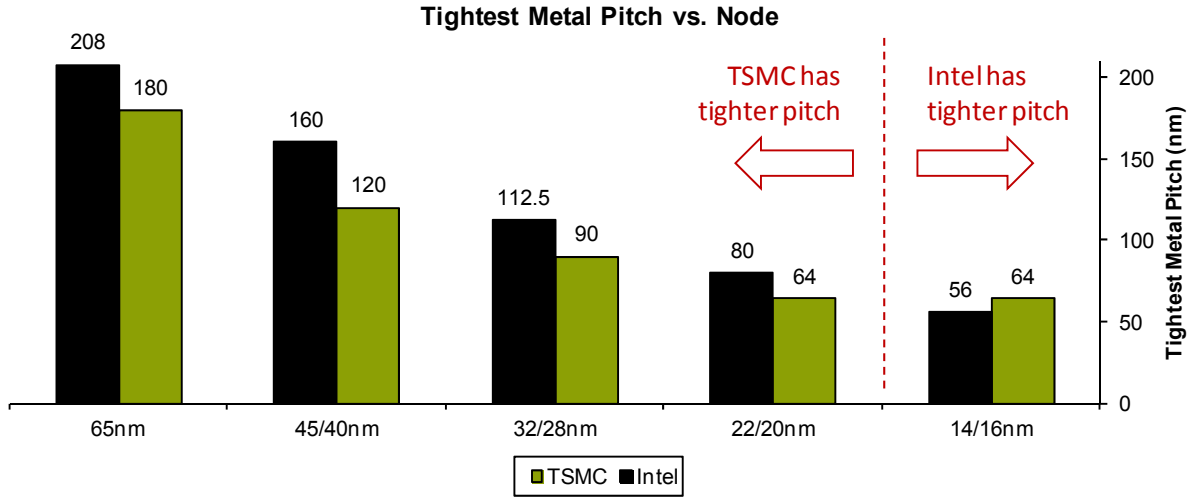
Source: TSMC and Bernstein estimates and analysis.

Exhibit 182 As 16nm Is Essentially the "3D Transistor Version of 20nm," It Does Not Enable Any Area Scaling from 20nm



Source: TSMC and Bernstein analysis.

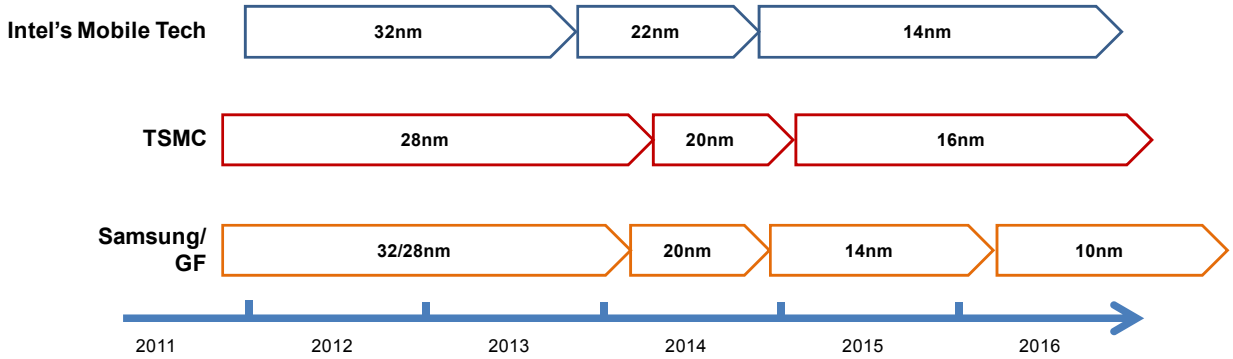
Exhibit 183 TSMC Historically Has Tighter Metal Pitch and Therefore Possibly Lower Cost Than Intel; However This Can Be Reversed in 14/16nm



Note: Intel's presentation given in July 2012 (http://www.semi.org/ko/sites/semi.org/files/docs/Mark%20Bohr_Intel.pdf) suggests the shrink of 0.7x per generation to continue beyond 22nm.

Source: Corporate data and Bernstein estimates and analysis.

Exhibit 184 Summary of Changes in Performance and Cost Difference for 22/20nm and 16/14nm



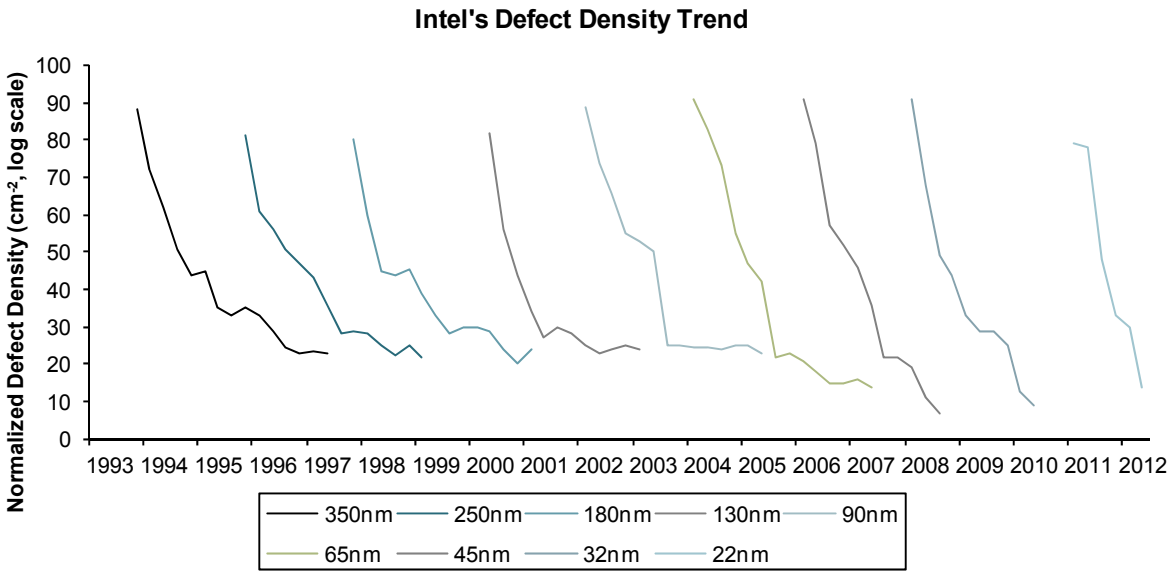
	22/20nm node	16/14nm node
Performance	Intel better by 10-20%	Intel better by 20-30%
Power Consumption	Intel better by 20-30%	Intel better by 20-30%
Die area [2]	TSMC smaller by 36%	Intel smaller by 23%

Note: 1. The left edge of the box is beginning of mass production; 2. Die area is estimated based on metal pitch.

Source: Corporate data and Bernstein research.

Finally, Intel's 14nm likely can enjoy a smoother yield improvement as it is the second generation for Intel to produce 3D transistor. Intel can also leverage the experience from the vast production volume of CPU chips. As can be seen in Exhibit 185, Intel was able to improve its 22nm process rapidly, as measured by the steeper defect density (a measurement of defects per wafer area and inversely related to yield) reduction. Due to the lack of prior production experience, foundries and its customers, on the contrary, will face great uncertainty in yield as 16nm is the first time they have ever produced a 3D transistor.

Exhibit 185 **Intel's Prior Experience in 3D Transistor in 32nm Helped to Reduce the Defect Density in 22nm**



Source: Intel and Bernstein analysis.

Intel Is a Credible Contender for Apple's Foundry Business But Not Likely in the Next Generation

Considering the technology leadership, we think Intel is a credible contender for Apple's foundry business. To gauge the possibility, we searched for the recent job posts at Intel and found 60 foundry-related jobs. This clearly indicates an active expansion of its foundry organization (called Intel Customer Foundry, or ICF) (see Exhibit 186).

However, the design efforts and risk considerations should make TSMC and Samsung more sensible choices in the next generation (20nm) for Apple. Being vertically integrated with no external customers, Intel has very unique manufacturing processes and design methodologies. We estimate that it would take around two years for a potential customer, such as Apple, to adopt Intel's technologies. Therefore in our view, TSMC and Samsung are the most possible foundries for Apple in 20nm.

It is worth noting that we don't think TSMC would be the sole supplier to Apple as the risk of moving 100% the supply chain to TSMC as well as likely new OSAT and substrate suppliers is high.

Intel conceivably can replace Samsung and share Apple's business with TSMC in the following generation (14nm). Though Apple would like to cut its ties with Samsung as soon as possible, we don't think counting on TSMC and Intel completely is a reasonable next step owing to the high risk of two new suppliers. The most possible transition is Samsung (28nm) -> TSMC + Samsung and maybe TSMC + Samsung + Intel (20/22nm), and finally TSMC + Intel (16/14nm) (see Exhibit 187).[8]

[8] The possible scenarios were analyzed in **Global Semis: The Apple Processor Conundrum (cont'd)... Intel Joins the Fray?**

Exhibit 186 **The Search for Foundry Engineers Indicates Intel's Intent to Expand in Foundry Business**

Apply Online | Add to My Job Cart

Job Description

Sr. Technology and Design Integration Engineer - 711103

Description

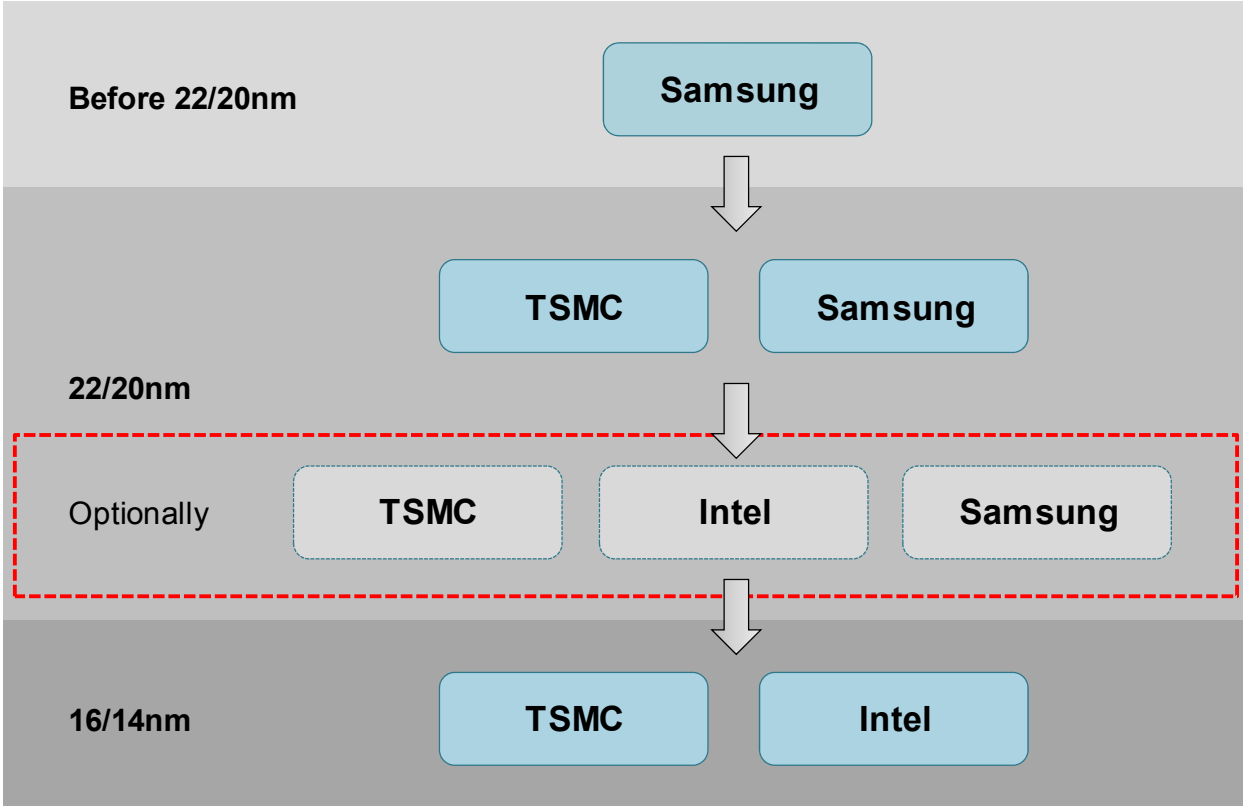
Intel's Custom Foundry (ICF) division within the Technology and Manufacturing Group (TMG) is looking for an Engineer that can provide a bridge between technology and designs and provide optimized solutions to enable these designs on Intel process. The designs can be internal collateral kit teams and/or external customers. In this position, your responsibilities will include but not be limited to:
- Interfacing with technology development team, foundry design kit team, and design teams to address design collateral issues and provide optimum solutions to these issues.
- Providing technology trainings to customers and internal ICF teams.
- Providing onsite technology customer support to ramp design execution.
- Working with ICF product management teams in engagement phases to support any needs related to process technology.
- Performing design simulation, variation/EM/RV/aging analysis, layout, Design Rule Checking (DRC), Layout Versus Schematic (LVS) checking, and parasitic extraction
- Creating and managing usage specification documents/whitepapers for all process.
- Establishing a robust process design collateral validation and test suite with kit team collateral. This includes process file/variation/aging tables, verification flows, mask layer usage, and special device templates.

Qualifications

You should possess a minimum of a Master's degree in Electrical Engineering or Computer Engineering and at least 8 years of experience in VLSI industry; or a PhD degree in Electrical Engineering or Computer Engineering and at least 4 years of experience.

Source: Intel.

Exhibit 187 The Possible Transition Path of Apple's Foundry Business



Source: Bernstein research.

We're Less Concerned About Samsung's Direct Competition With TSMC from the Perspective of Its Business Model Conflict With Customers; However, the Samsung Threat Lies in Its Growing Self Sufficiency in Logic ICs, Leaving Less Demand for TSMC's Customers and TSMC

Over the past a few years, Samsung has been making remarkable progress in logic ICs. Its Exynos application processors have impressive performance and have been deployed in many internal and external handsets/tablets. Its LTE modem, although not as good as Qualcomm's, is also in commercial use. The acquisition of CSR last year extends its ability into connectivity. As Samsung improves its internal logic IC capability by leaps and bounds, its customers are also become increasingly wary of the interest conflict. We thus are doubtful that Samsung will evolve into a general foundry and be a direct competitor to TSMC.

We believe the threat from Samsung is actually in its vertical integration. We anticipate its set business, ranging from smartphones, tablets and PCs, will provide enough demand for Samsung to establish scale and be cost competitive, even accounting for Apple's likely departure. Marrying it with the improving design and manufacturing capability, Samsung very possibly will be much more self sufficient in logic ICs and leave significantly less demand available for TSMC's customers and TSMC in the future.

A Slower Moore's Law Can Conceivably Give Fabless Companies More Sourcing Options, But the Threat of Intel's Mobile Efforts Could, in the Long Term, Negatively Impact Them

Though we do not believe shrink is dead, it will almost assuredly slow over time. To the extent that this slowdown allows more choice in the mid-term by fabless customers seeking options, this could be advantageous (as it would allow them to likely achieve better pricing through multi-source options, not available today). We note, for example, Qualcomm actively seeking multiple sources for 28nm and 20nm today (with volume at TSMC, Samsung, and GlobalFoundries).

In the long term, however, Intel likely presents a unique threat as it will undoubtedly put increasing pressure on the foundry ecosystem (as it "saps" TSMC's high-value leading-edge customers away), and try to grow its own business into the mobile SoC space that is the lifeblood of many large fabless customers today. Should the foundry ecosystem prove unable to keep up with Intel, many (particularly mobile) fabless companies could encounter difficulties, as moving to Intel will likely not be an option. Among our coverage, we believe Qualcomm's radio leadership can provide some protection (it is as far ahead in radio technology as Intel is on process technology) and (just like Intel) it has tremendous R&D scale in its area of expertise; nevertheless the health and sustainability of its manufacturing options bears watching over the long term. Broadcom may be less impacted by process gaps (historically it was never one to push huge volume at the leading edge, and is a consummate user of the multi-sourcing strategy already), but it is taking steps (for instance, in the networking space) to move some key portions of the portfolio forward.

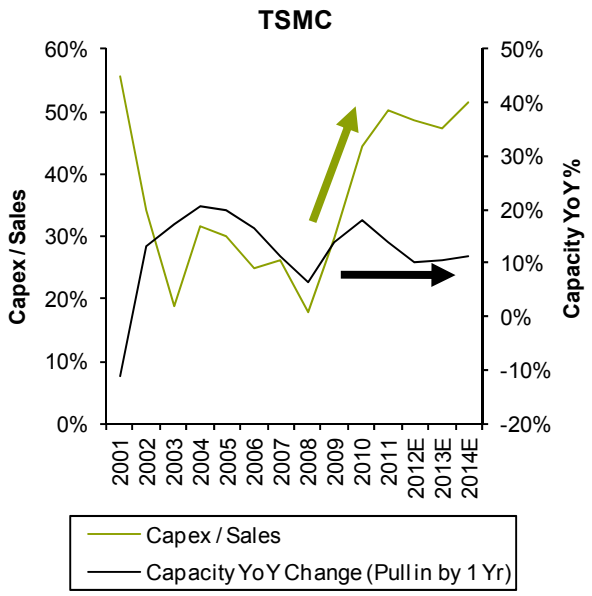
We Continue to Forecast Margin Deterioration for TSMC Because of Competition Pressure

As for TSMC, albeit our positive view on near-term 28nm demand and Apple's business in 2014 and 2015, we believe margin deterioration is forthcoming. With the technology lead in the next two to three years, Intel likely will make further headway into the mobile market and exert pressure on foundries and their customers. Samsung will also further leverage its vertical integration and become more self-sufficient in logic ICs. Both developments are negative to TSMC's customers and hinder TSMC's ability to transfer cost increase to them.

Owing to the rising capital cost requirements, TSMC is expected to spend more in capex just to maintain capacity addition at a pace that is comparable with its history (see Exhibit 188). The competition will limits pricing power and the ramp-up speed of 20nm and below, making depreciation grow much faster than sales (see Exhibit 189). Although the company repeatedly guided otherwise, we don't think TSMC can pass the entire cost burden to its customers and keep its profitability unchanged. We project TSMC's earnings growth to fall behind top-line (see Exhibit 190) as its GM/OPM deteriorate (see Exhibit 191). Its ROE will drop in the next few years as well (see Exhibit 192).

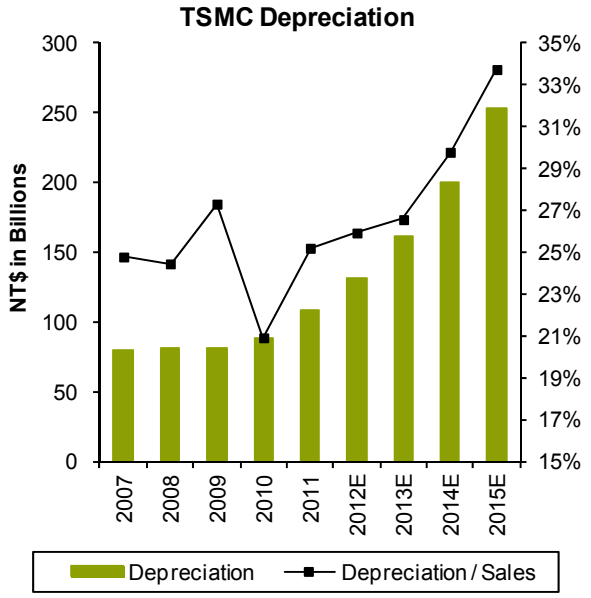
We therefore remain conservative on TSMC, especially considering its high valuation. It is currently trading at 3.7x book value, much higher than the 3.3x historical average P/B (see Exhibit 193). We rate TSMC market-perform.

Exhibit 188 Owing to the Higher Capital Cost of New Technologies, TSMC Has to Maintain High Capex Just to Keep Capacity Addition at a Pace Similar to Its History



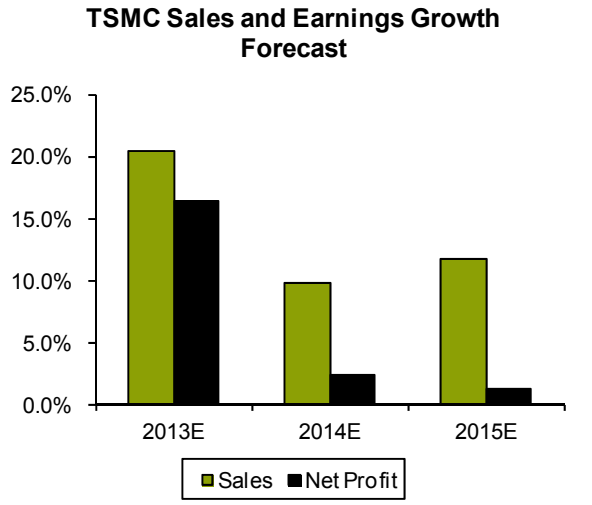
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 189 We Project TSMC's Sales Growth Is Insufficient to Offset Rising Depreciation Burden



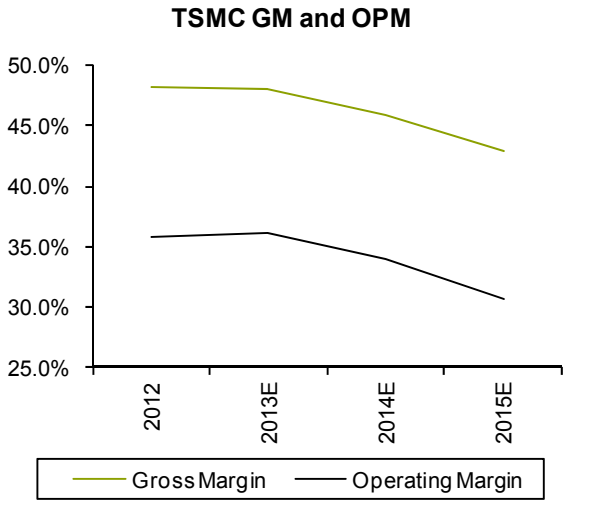
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 190 TSMC's Earnings Growth Is Expected to Fall Behind Its Revenue Growth…



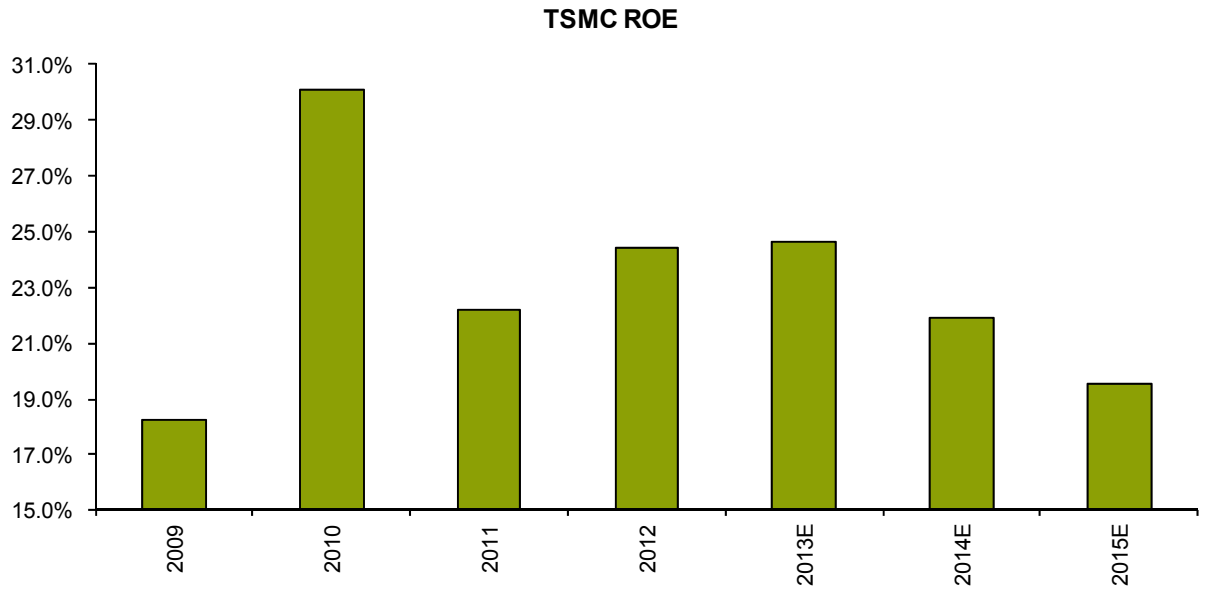
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 191 …Due to Margin Deterioration in 2014



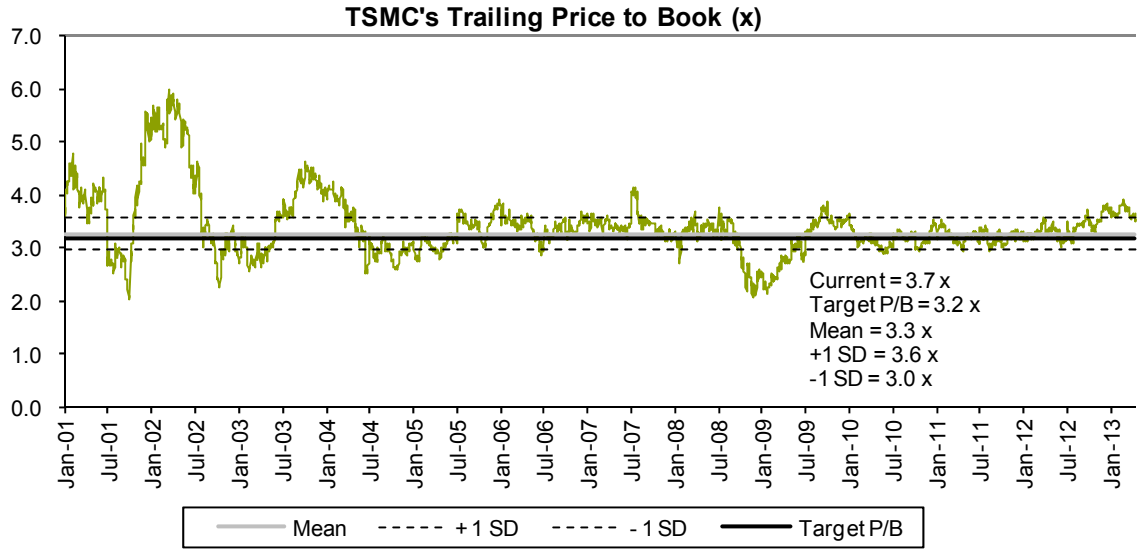
Source: Corporate data and Bernstein estimates and analysis.

Exhibit 192 TSMC's ROE Is Expected Drop in 2014 and 2015



Source: Corporate data and Bernstein estimates and analysis.

Exhibit 193 TSMC Is Currently Trading at a High P/B Level



Source: Bloomberg L.P., corporate data and Bernstein estimates and analysis.

The New Memory Paradigm — Why Scaling Limitations Are Good for Memory Suppliers

In earlier chapters, we have discussed the slowing of Moore's Law and the impact on the logic semiconductor industry. In this chapter, we address what the potential end of scaling means for the Memory industry.

Node migration is becoming increasingly difficult in both NAND and DRAM. We see strong signs of shrink slowing down in all types of memory technology, but most notably in NAND. This slowdown is bringing forth a new paradigm. Slower migration means lower supply growth and thus a positive for supply/demand balance and hence pricing. Furthermore, technological complexity is increasing the risk and makes investing in new capacity less attractive.

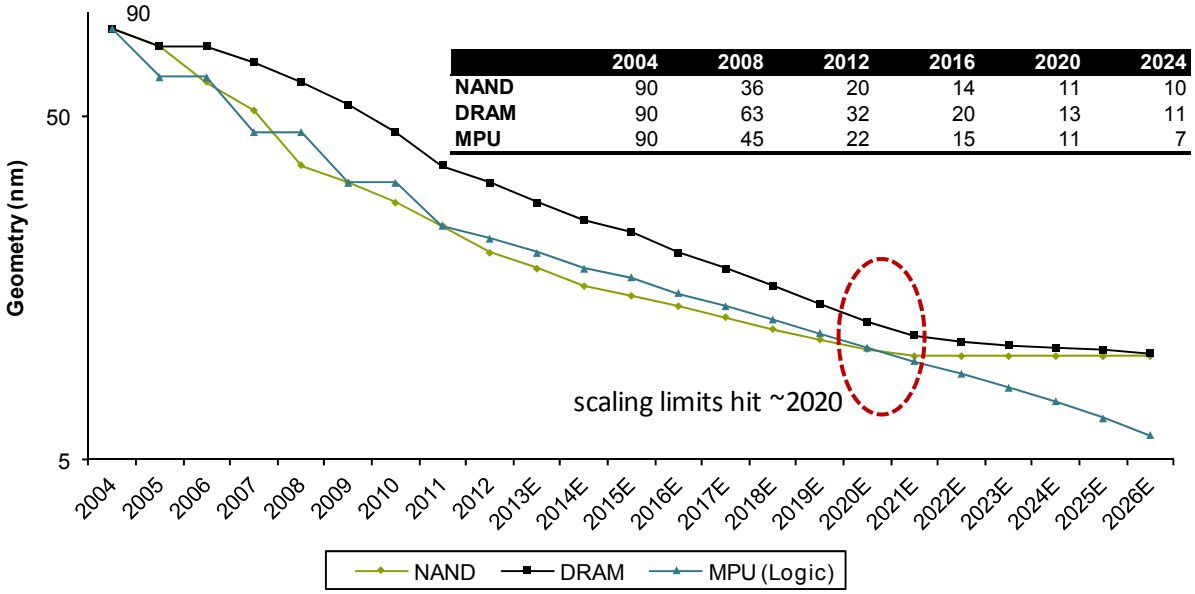
We evaluate the limitations of DRAM and NAND and potential replacements in the next decade. 2D NAND will likely co-exist with 3D NAND for several years but has the potential to be at least partially replaced by ReRAM or 3DReRAM in the next decade. For DRAM, we do not see any viable candidate for replacement, but it may be slightly cannibalized around the edges by PCRAM, STT-MRAM and even NAND. Regardless of which technology wins here, we have no doubt the leaders will be the incumbents. In particular, Samsung with its tremendous resources seems particularly well positioned, with teams working on all types of new memory. SanDisk, with its focus and investment in 3DReRAM, is well positioned to benefit as is (by default) its partner, Toshiba.

As NAND Scaling Slows, So Too Does Bit Growth

NAND Will Soon Face Scalability Challenge at the 10-12nm Level

For NAND, on the technology side and as NAND scaling continues, the number of critical electrons is expected to fall to only 10 at sub-1xnm design level, implying a shortage of electrons to store multiple states in a cell (see Exhibit 194 through Exhibit 196).

Exhibit 194 NAND Scaling Has Accelerated Beyond DRAM, and MPUs to Be the Leader in Process Technology; However, We See NAND Hitting a Wall at 10nm by 2021; DRAM Will Also Hit a Wall Around 11nm by 2022



	2004	2008	2012	2016	2020	2024
NAND	90	36	20	14	11	10
DRAM	90	63	32	20	13	11
MPU	90	45	22	15	11	7

Source: ITRS and Bernstein analysis.

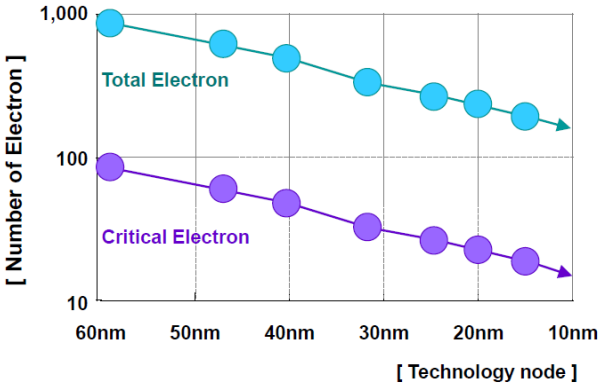
With multi-level cell (MLC) and tri-level cell (TLC) requiring four and eight voltage levels, respectively, managing this small number of 10 electrons is becoming closer to impossible. As scaling continues and complexity increases, we note that capex is also increasing and overall cost declines are slowing, which is why we see a new memory technology is necessary.

Exhibit 195 Issues With 10nm Floating Gate NAND Below 12nm

X - direction	CG poly-Si void Interference Bit-Line loading
Y - direction	WL bending Interference WL-to-WL leakage

Source: SK Hynix and Bernstein analysis.

Exhibit 196 The Number of Critical Electrons Will Fall to Only 10 at Sub-1xnm Design Rule



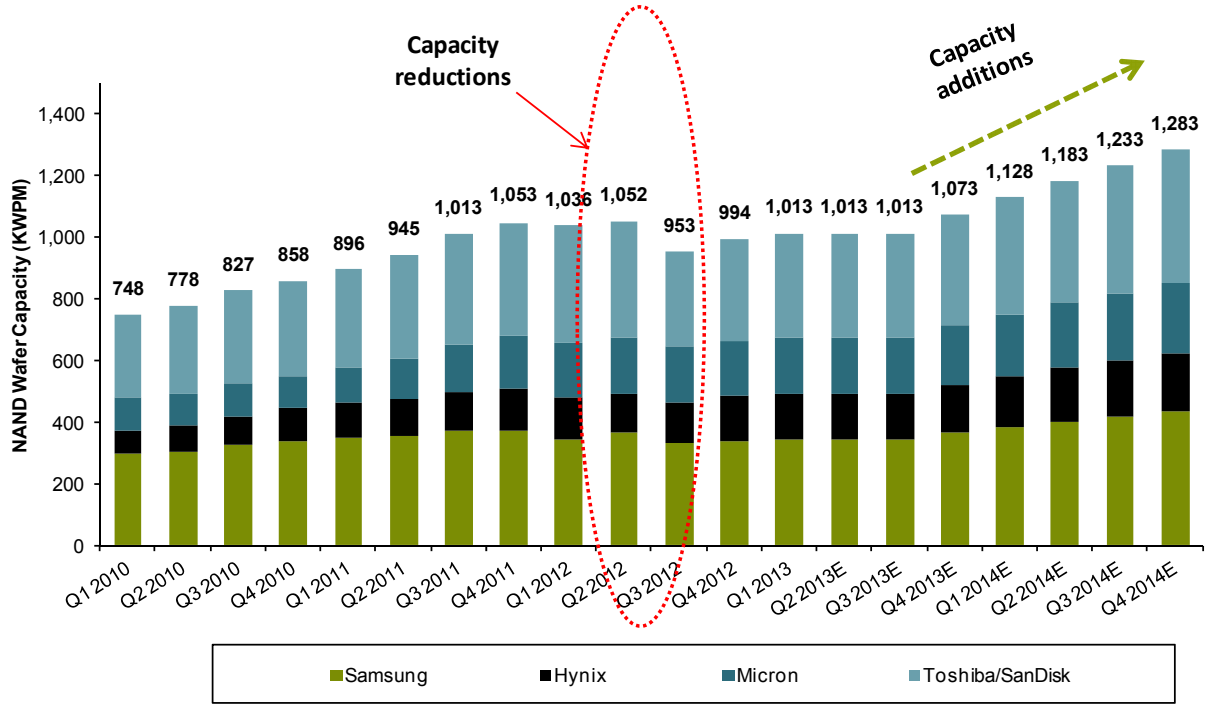
Source: SK Hynix.

As a Result, Shrink Is Decreasing and 475 KWPM Additional Wafer Capacity Will Be Required by 2017

We see no wafer growth before 4Q:13, at the earliest (41% GB production growth in 2013) and, with GB/wafer growth falling as technology advancement begins to slow down, we see a large gap developing between supply and demand that must be filled with additional wafer capacity by 2H:13. We estimate that 475 KWPM additional wafer capacity will be required by 2017 to meet demand projections (see

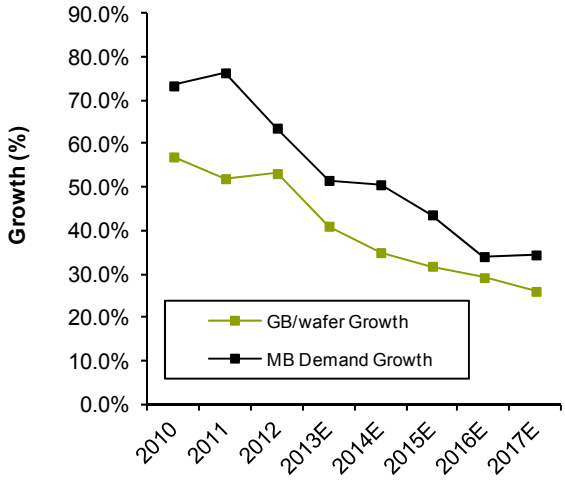
Exhibit 199). If NAND makers continue to refuse to add capacity due to technological risk and complexity, we will see margins soar.

Exhibit 197 NAND Supply Wafer Capacity: We Expect the Industry to Start Adding Wafers Back in 4Q:13



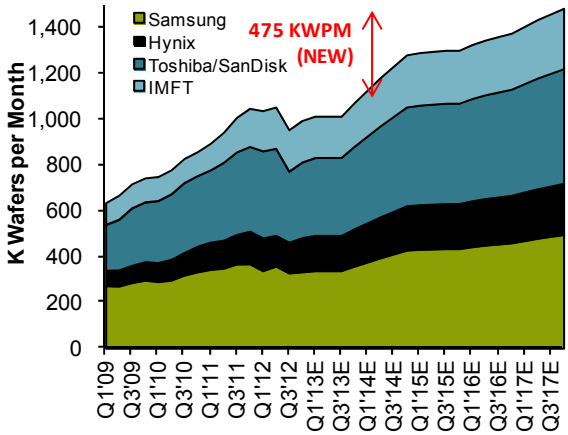
Source: DRAMeXchange and Bernstein estimates and analysis.

Exhibit 198 Without New Wafers, the GB/Wafer Growth Is Not Enough Due to Technology Constraints…



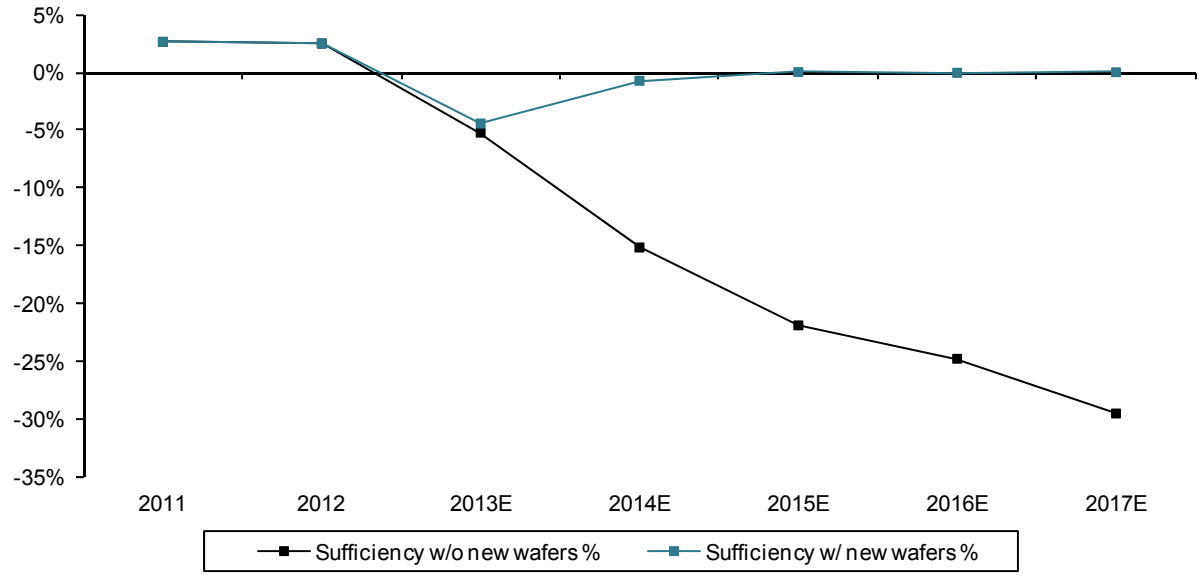
Source: DRAMeXchange, Gartner and Bernstein estimates and analysis.

Exhibit 199 …Hence the Need for an Additional 475 KWPM Wafer Capacity by 2017



Source: DRAMeXchange, Gartner and Bernstein estimates and analysis.

Exhibit 200 **The Long-Term NAND Will Be in Severe Undersupply Without Considerable Addition of New Capacity**

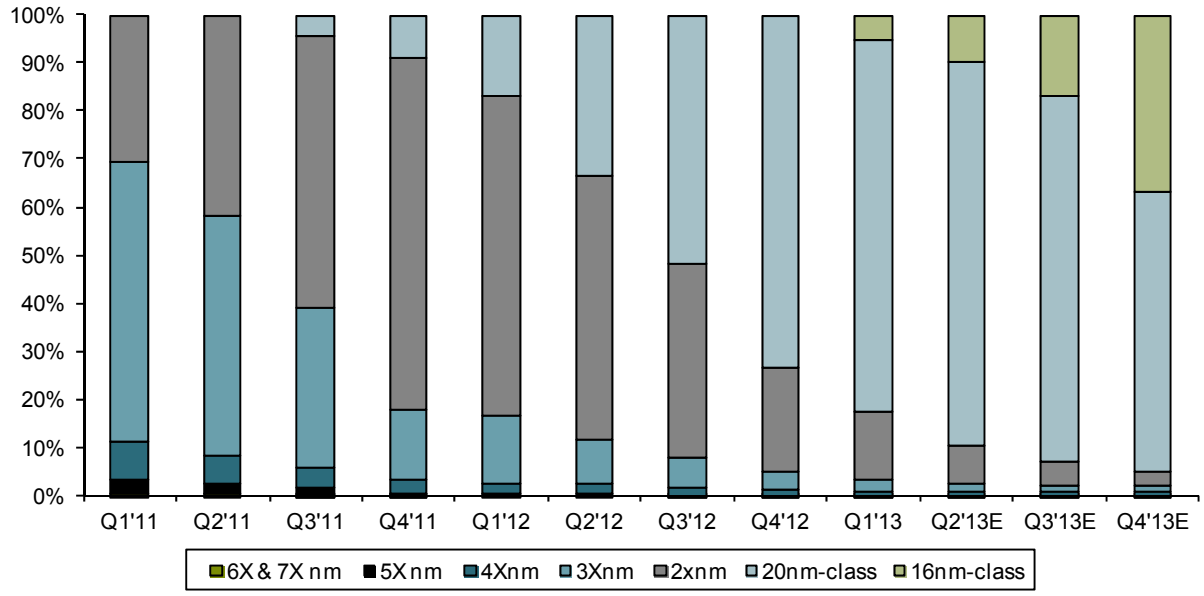


Source: DRAMeXchange, Gartner and Bernstein estimates and analysis.

However, Increased Complexity Combined With Higher Costs Make NAND Makers Unlikely to Add New Capacity Anytime Soon

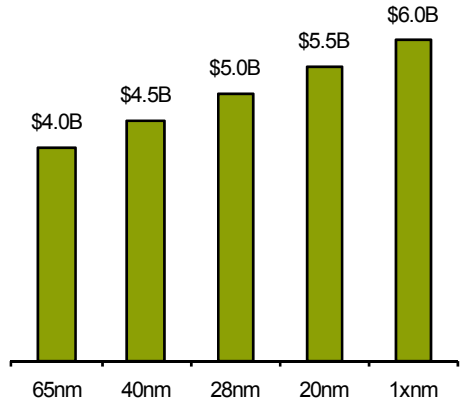
We estimate 78% of NAND is currently produced on 20nm-class (see Exhibit 201). As scaling continues and complexity increases, capex is also increasing (see Exhibit 202 and Exhibit 203). Furthermore, this increased complexity means cost declines are slowing (see Exhibit 204).

Exhibit 201 **NAND Process Technology Is Now Entering the Sub-20nm Arena**



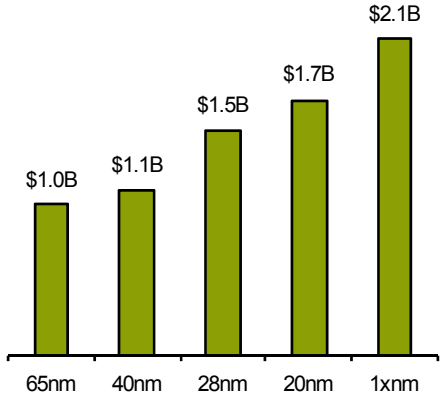
Source: DRAMeXchange and Bernstein estimates and analysis.

Exhibit 202 Capex per 100kWPM New Capacity Continues to Increase…



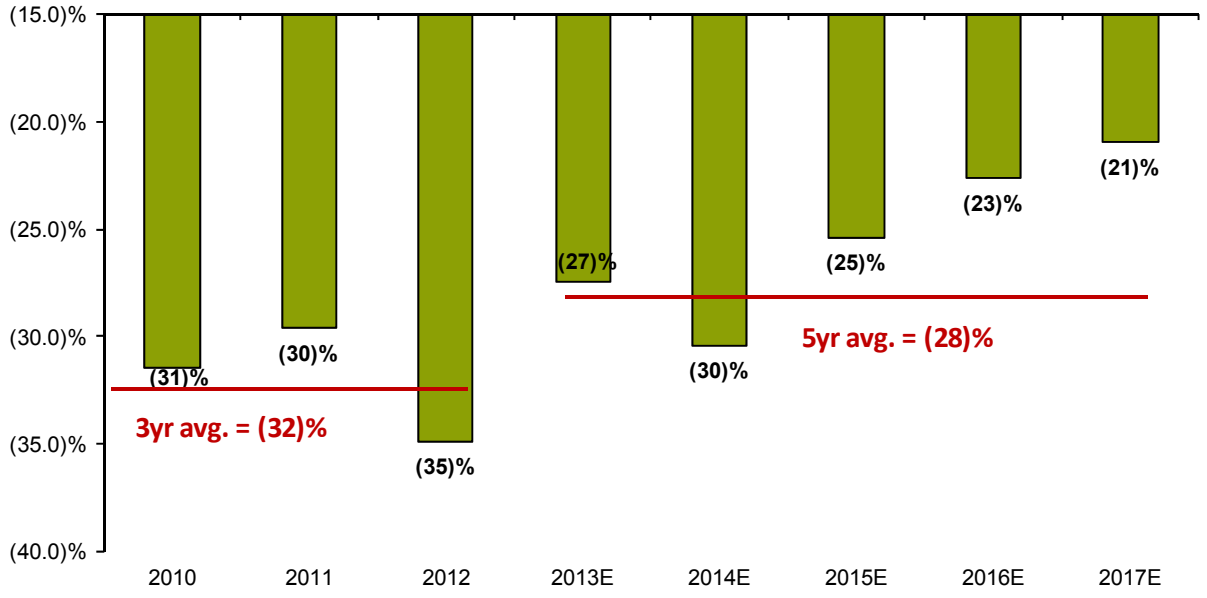
Source: Bernstein estimates and analysis.

Exhibit 203 …as Does the Capex to Just Upgrade Fab Equipment



Source: Bernstein estimates and analysis.

Exhibit 204 We Forecast Aggregate YOY Cost/GB Decrease for NAND Players to Come Down



Source: Corporate reports and Bernstein estimates and analysis.

At Today's Prices, NAND Makers Do Not Make Adequate Returns

We estimate that full-year 2012 NAND industry gross margins averaged 23%, compared to NAND customers, which generate ~60-80% gross margins (Fusion-io, EMC, Apple NAND).

At these 23% gross margins, NAND makers are making a mere 3% ROIC (see Exhibit 205), which is an unacceptable return considering the cost of capital, risk and technological uncertainty involved in these investments. Therefore, NAND makers should not invest in supply capacity at today's levels.

We assume $6 billion PP&E for one fabrication plant and 1.7 million wafers per year. Assuming $2,000/wafer gets us to $3.4 billion sales per fab, we use one quarter of $3.4 billion sales/fab as a proxy for current assets required, and combined with $6.0 billion PP&E, this yields $6.8 billion in total assets. A key

assumption behind our ROIC calculation is that financial debt plus equity exactly equals total assets in this theoretical example.

Assuming 15% opex/sales and 20% corporate tax rate, we get to 7% net income/sales under the 100% equity financing scenario. Under the 50% equity/50% debt scenario, we get to -3% net income/sales.

Exhibit 205 NAND Economics Assuming 23% 2012 Gross Margins

NAND Theoretical with 23% Gross Margins			
PPE ($B)	6.0		
Wafers per month ('000)	140		
Wafers per year (M)	1.7		
$/Wafer	2,000		
Sales/fab ($B)	3.4		
Sales/PPE ($)	0.6		
Current Assets ($B)	0.8	Assumes one quarter of sales/fab	
PPE ($B)	6.0		
Total Assets ($B)	6.8		
Sales/Assets	49%		
Debt Equity Split	**All Equity**	**50/50**	
Debt ($B)	0.0	3.4	
Equity ($B)	6.8	3.4	
Total ($B)	6.8	6.8	
GM	23%	23%	
OpM	8%	8%	Assumes 15% OpEx/Sales
EBIAT	7%	7%	Assumes 20% corporate tax
NI%	7%	-3%	Assumes 3% post tax cost of debt
ROIC	3%	3%	Assumes Total Assets = Financial Debt + Equity
ROE	3%	-3%	

Source: Bernstein estimates.

Even at the 28% gross margins we estimate NAND makers made in 1Q:13, we believe the ROIC is only 5% (see Exhibit 206).

Exhibit 206 NAND Economics Assuming 28% 1Q:13 Gross Margins

NAND Theoretical with 28% Gross Margins			
PPE ($B)	6.0		
Wafers per month ('000)	140		
Wafers per year (M)	1.7		
$/Wafer	2,000		
Sales/fab ($B)	3.4		
Sales/PPE ($)	0.6		
Current Assets ($B)	0.8	Assumes one quarter of sales/fab	
PPE ($B)	6.0		
Total Assets ($B)	6.8		
Sales/Assets	49%		
Debt Equity Split	**All Equity**	**50/50**	
Debt ($B)	0.0	3.4	
Equity ($B)	6.8	3.4	
Total ($B)	6.8	6.8	
GM	28%	28%	
OpM	13%	13%	Assumes 15% OpEx/Sales
EBIAT	10%	10%	Assumes 20% corporate tax
NI%	10%	0%	Assumes 3% post tax cost of debt
ROIC	5%	5%	Assumes Total Assets = Financial Debt + Equity
ROE	5%	0%	

Source: Bernstein estimates.

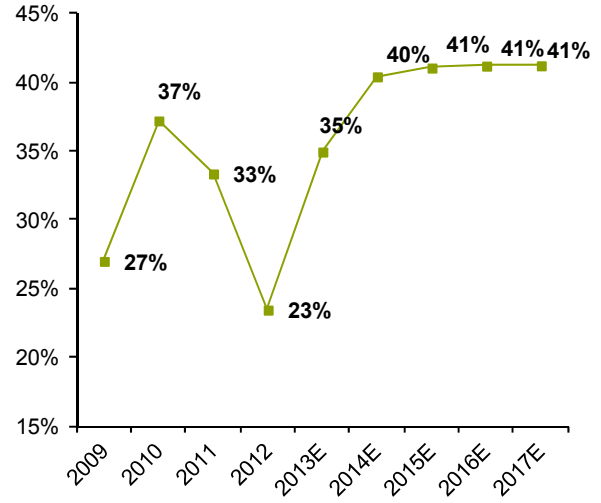
Our base case NAND economics model assumes that NAND industry gross margins will go back up to 35% in 2013 assuming $0.66/GB ASP. However, we estimate that 45% gross margins are actually required for NAND makers to reach 12% ROIC (see Exhibit 207 through Exhibit 209).

Exhibit 207 NAND Economics Assuming 45% Gross Margins (Our Base Case Is 35% in 2013E)

NAND Theoretical with 45% Gross Margins			
PPE ($B)	6.0		
Wafers per month ('000)	140		
Wafers per year (M)	1.7		
$/Wafer	2,000		
Sales/fab ($B)	3.4		
Sales/PPE ($)	0.6		
Current Assets ($B)	0.8	Assumes one quarter of sales/fab	
PPE ($B)	6.0		
Total Assets ($B)	6.8		
Sales/Assets	49%		
Debt Equity Split	**All Equity**	**50/50**	
Debt ($B)	0.0	3.4	
Equity ($B)	6.8	3.4	
Total ($B)	6.8	6.8	
GM	45%	45%	
OpM	30%	30%	Assumes 15% OpEx/Sales
EBIAT	24%	24%	Assumes 20% corporate tax
NI%	24%	14%	Assumes 3% post tax cost of debt
ROIC	12%	12%	Assumes Total Assets = Financial Debt + Equity
ROE	12%	13%	

Source: Bernstein estimates.

Exhibit 208 We Currently Model NAND Industry Gross Margins at ~41% Going Forward…



Source: DRAMeXchange, corporate reports and Bernstein estimates and analysis.

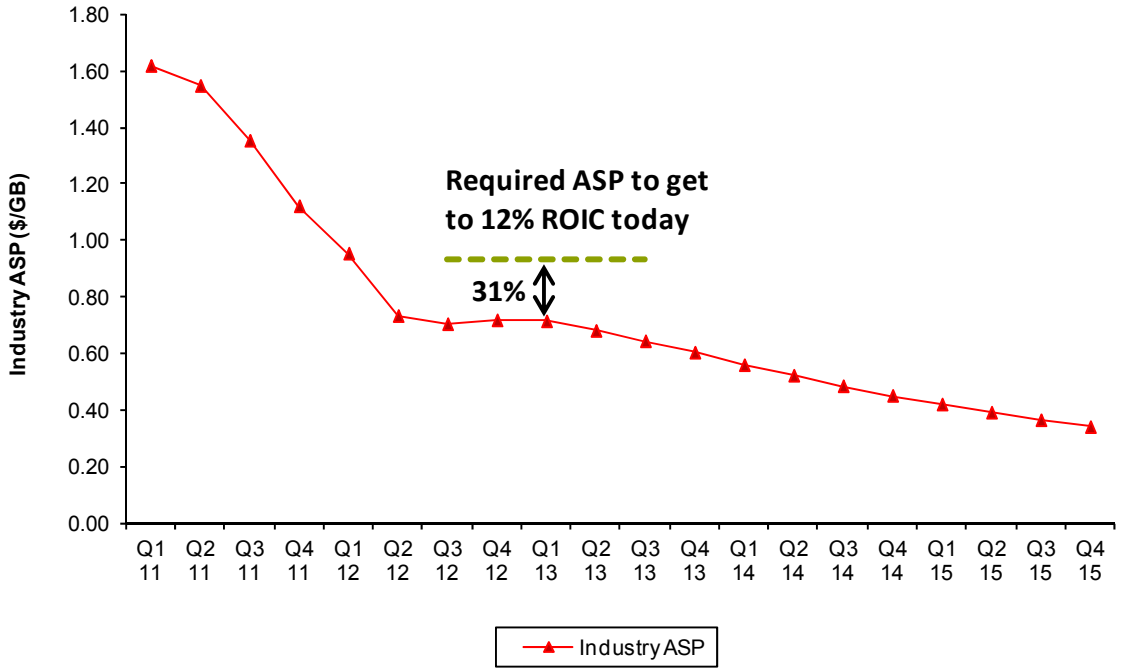
Exhibit 209 …While We Believe NAND Gross Margins Would Have to Be 45%+ to Make the ROIC Work for NAND Makers

Gross Margins	ROIC	
10%	(2.0)%	
15%	0.0%	
20%	2.0%	Today
25%	3.9%	
30%	5.9%	
35%	7.9%	
40%	9.8%	Required ROIC
45%	11.8%	
50%	13.8%	

Source: DRAMeXchange, corporate reports and Bernstein estimates and analysis.

Getting to 45% gross margins and 12% ROIC today would require NAND ASP 31% higher than 1Q:13 NAND Industry ASP levels (see Exhibit 210).

Exhibit 210 **The NAND ASP Required to Get to 12% ROIC Today Is 31% Higher Than 1Q:13 NAND Industry ASP Levels**



Note: For quarters, Micron's closest fiscal quarter is used (i.e., 2Q:FY11 is used as a proxy for 1Q:CY11).

Source: DRAMeXchange, corporate reports and Bernstein estimates and analysis.

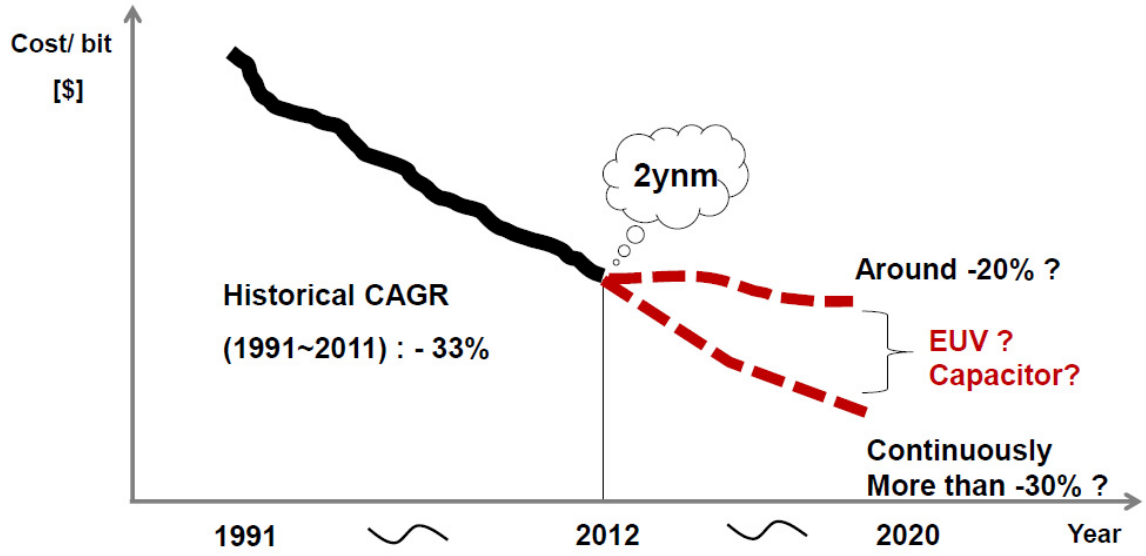
DRAM Scaling and Hence Bit Growth Also Slowing

DRAM Is Also Facing Difficulties, Though Less Imminent Than NAND

For DRAM, we have seen its cost per GB reduced exponentially over the past several decades as node shrink continues. However, the exponential reduction may not continue as the current technology faces limitation (see Exhibit 211).

Even though it still has several more legs to advance than NAND, it is becoming increasingly questionable if current DRAM technology will be able to maintain the storage capacitance in decreasing cell area past 1xnm products. This provokes a huge challenge, associated with the density increase happening at the same time.

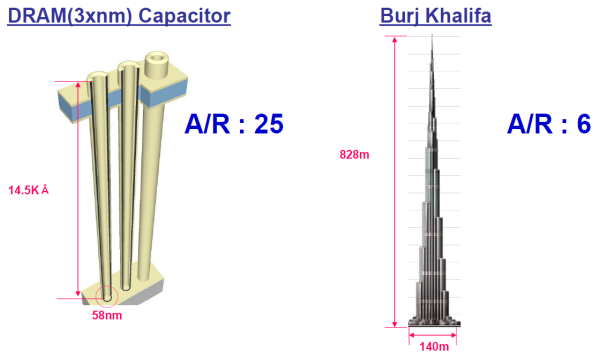
Exhibit 211 Cost per GB Has Been Decreasing Exponentially Over the Past Couple of Decades; However, as the Current Technology Faces Limitation, We Are Increasingly Doubtful If the Rate of Technological Advance Will Continue to Follow Moore's Law Going Forward



Source: SK Hynix.

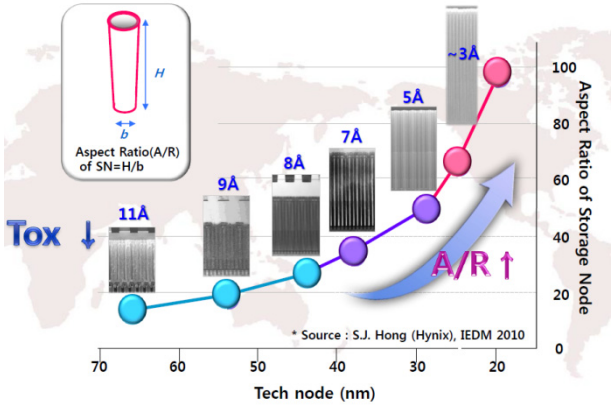
One of the critical challenges DRAM faces is high aspect ratio. At 3xnm, the aspect ratio (trench depth/diameter) of DRAM's cell capacitor already reached 25x, which is much higher than the world's tallest building Burj Khalifa's aspect ratio of 6x (see Exhibit 212). As node shrinks, the aspect ratio rises exponentially, and this creates a major challenge to manufacturers, especially in the deposition and etching processes (see Exhibit 213). We see DRAM scaling slowing down and eventually reaching limitation at 15nm.

Exhibit 212 At 3xnm DRAM, Aspect Ratio of Capacitors Reached 25 vs. World's Tallest Building's 6



Source: SK Hynix.

Exhibit 213 And the Aspect Ratio of Capacitors Becomes Too Large as Node Shrinks

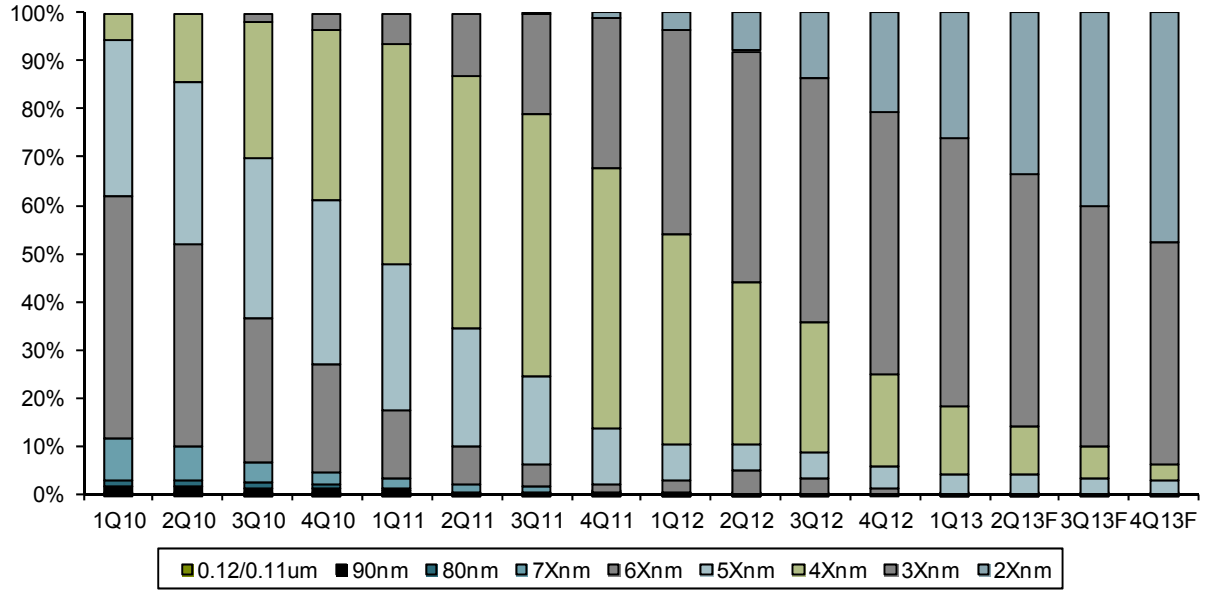


Source: SK Hynix.

Supply Growth Is Naturally Slowing as the Pace of Shrink Slows and as the Industry Continues to Convert PC DRAM to Mobile DRAM, With 15-25% Die Penalty

We see DRAM shrink slowing, which is causing supply growth to slow dramatically (see Exhibit 214). DRAM GB per wafer growth is slowing, which is one of the key reasons why supply/demand balance has improved and will remain structurally better going forward. We expect GB per wafer growth to fall from 44% in 2012 to 22% by 2017 as node migration slows.

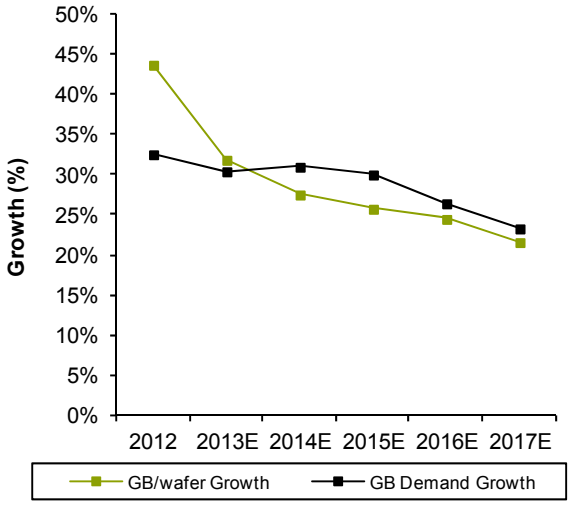
Exhibit 214 DRAM Industry Node Migration Is Slowing



Source: DRAMeXchange and Bernstein estimates and analysis.

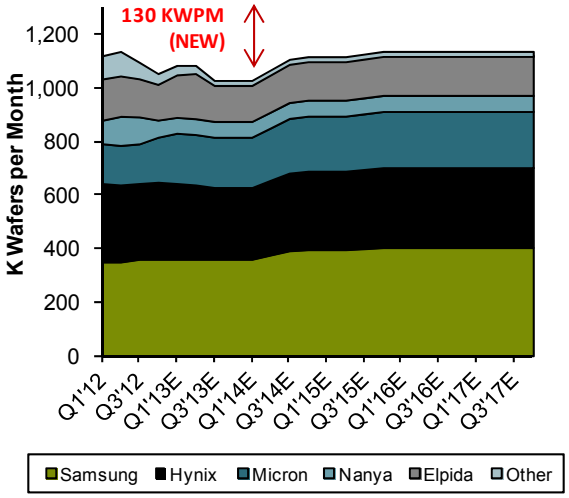
As GB per wafer growth falls, even with weak PC demand the DRAM industry faces shortages. The new order in DRAM, with just three players controlling 97% of the market, makes new capacity additions increasingly unlikely. While we do need an additional 130,000 wafers by the end of 2017 to reach balance in our industry model, we believe it is more likely that no wafers will be added, and thus shortages continue for longer.

Exhibit 215 GB/Wafer Growth Is Slowing and Falling Behind Demand Growth Due to Technology Constraints…



Source: DRAMeXchange, Gartner and Bernstein estimates and analysis.

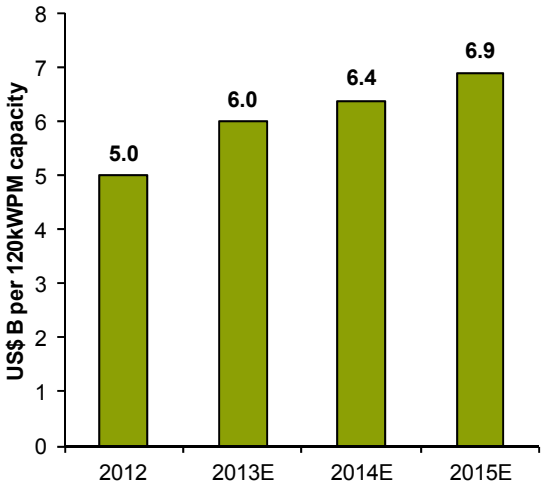
Exhibit 216 …Hence the Need for an Additional 130kWPM Wafer Capacity by 2017



Source: DRAMeXchange, Gartner and Bernstein estimates and analysis.

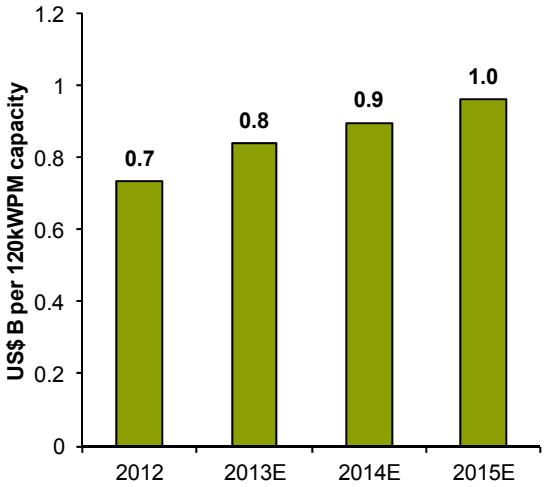
This complexity also further discourages new entrants as cost of entry is higher than ever. The DRAM industry node migration has come a long way, and we are now approaching an end of further scaling. The cost associated with additional technology advancement is becoming larger and this further discourages new entrants to the industry. Costs to build a fab and be relevant continue to increase. The cost for new fabs is increasing, making it extremely costly and risky for new entrants. The prospect of new entrants in DRAM is preposterous today (see Exhibit 217 and Exhibit 218).

Exhibit 217 Capex per 120kWPM New DRAM Capacity Continues to Increase…



Source: Bernstein estimates and analysis.

Exhibit 218 …as Does the Capex to Just Upgrade DRAM Fab Equipment



Source: Bernstein estimates and analysis.

Longer Term, DRAM May Be Slightly Cannibalized

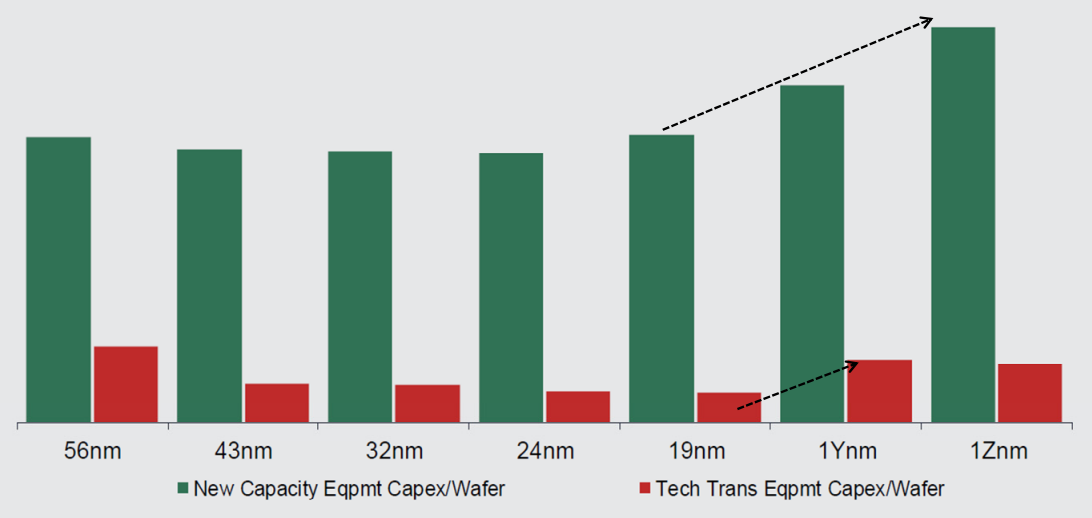
For DRAM, we do not see any viable candidate for replacement, but it may be slightly cannibalized around the edges by PCRAM, STT-MRAM and even NAND.

3D Used as a Way to Extend Scaling

3D NAND Is Being Used as a Way to Continue Cost Declines and Bit Growth

At sub-1Xnm, NAND scaling becomes extremely complicated and costly. SanDisk at its recent Investors Day explained that the capex required to upgrade to the 1Ynm node will be twice the previous nodes as it increases tools required for quadruple patterning. Furthermore, the number of critical electrons is expected to fall to only 10, presenting huge complexity for the controller (see Exhibit 219).

Exhibit 219 Planar NAND Scaling Is Becoming More Costly — SanDisk Shows That the 1Ynm Technology Transition Will Cost 2x the Previous Nodes



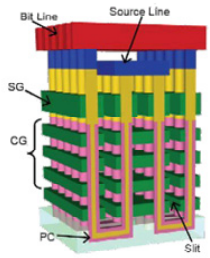
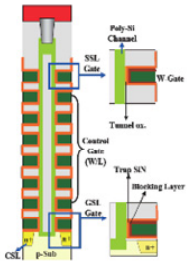
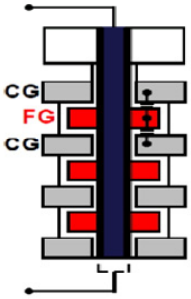
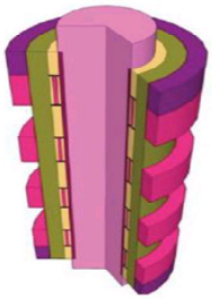
Source: SanDisk 2013 investor day.

The concept for 3D NAND is simple: rather than laying the cells flat on the surface, higher densities can be achieved by stacking them on top of each other. The main issue is that conventional etching systems deal with aspect ratios (ARs) of 3:1-4:1, while 3D etching requires an aspect ratio of 20:1 or more.

All NAND companies are investing heavily in different types of 3D NAND or vertical NAND (see Exhibit 220). SanDisk and Toshiba have been pushing 3D NAND processes with its pipe-shaped Bit Cost Scalable (p-BiCS) technology. This is planned for mass production starting in 2016, after 1Znm.

Samsung (TCAT), SK Hynix (3D FG) and Micron also have their own 3D architectures, while Applied Materials and Macronix are developing their own systems to make the vertical stacking possible. Both Samsung and SK Hynix plan to have samples within 2013.

Exhibit 220 Competitors Utilize Various Different 3D NAND Architectures

	p-BiCS (Toshiba)	TCAT (Samsung)	3D FG (Hynix)	Micron
Structure	 Tanaka. H, VLSIT 2007	 J. Jang, VLSIT 2009	 S. Whang, IEDM 2010	 G. Hawk, FMS 2011
Key Features	- P+ SONOS Cell	- TANOS Cell	- Floating Gate	?
Key Issue	- Large Cell Size - Reliability	- Large Cell Size - SL Resistance	- Process of bit separation - Disturbance	?

Source: SK Hynix.

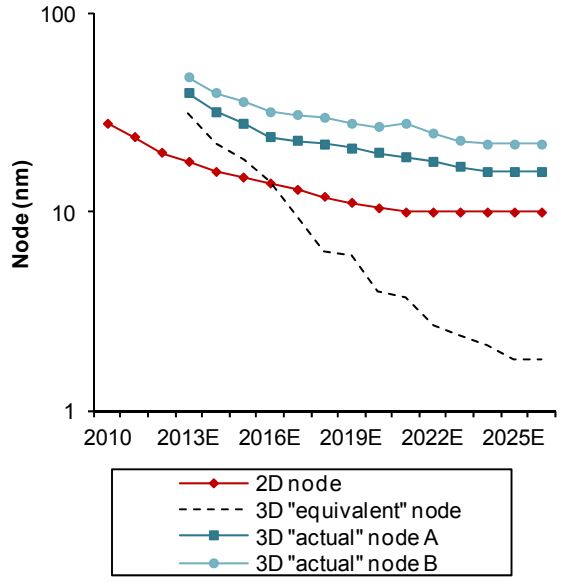
3D NAND Will Allow Cost per GB to Decline Past 2015

We believe planar NAND cannot scale below 10nm, and hence 3D NAND will be critical to continuing cost declines beyond 10nm. Although 3D NAND will likely be introduced at much older or larger nodes, we see that due to increased layers of NAND cells, the "equivalent node" can keep scaling for much longer in 3D. Even so, we still see limits to 3D NAND around 2020, when 3D hits the 2D equivalent node of 1.8nm (see Exhibit 221 and Exhibit 222).

This increased density through vertical stacking enables NAND bits/cm2 and thus GB/wafer to keep rising. We see 3D NAND bit density overtaking 2D NAND in 2017 (see Exhibit 223). However, due to the extra layers and processing required for 3D, we estimate that the wafer output or thousand wafers per month (KWPM) will be less than in a 2D NAND fab (see Exhibit 224). Taking into account both of these drivers (higher GB per wafer but lower wafer output), we still see 3D NAND output in GB per fab overtaking 2D NAND in 2018 (see Exhibit 225).

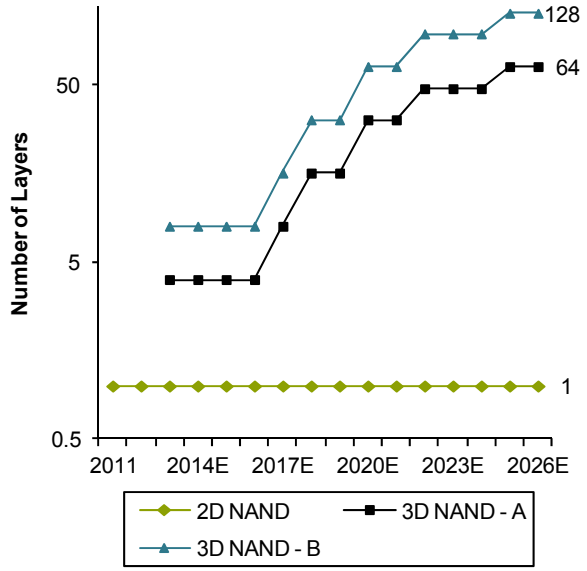
Finally, on a cost-per-GB basis, our extensive analysis shows that 3D NAND will become cheaper than 2D NAND by 2017 and reach $0.06 per GB by 2024 (see Exhibit 226).

Exhibit 221 While 2D NAND Reaches Its Technological Limitation at ~10nm, 3D Equivalent Node Will Shrink Further and Reach ~1.8nm by 2025



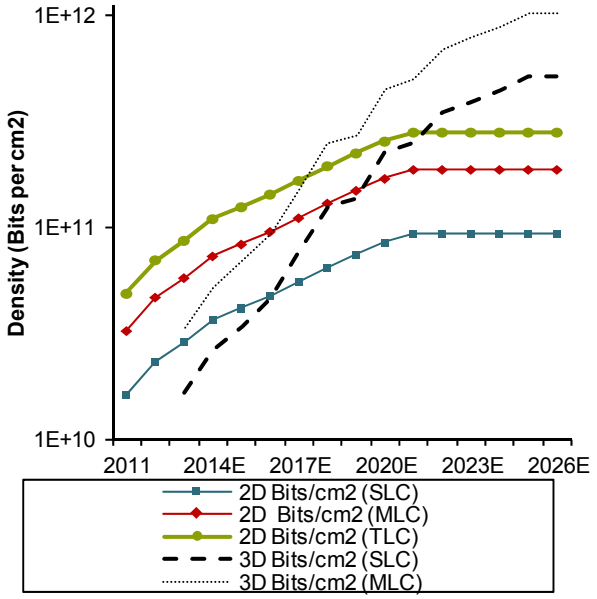
Source: ITRS and Bernstein estimates and analysis.

Exhibit 222 Together With Node Shrinks, Number of Layers Will Also Increase…



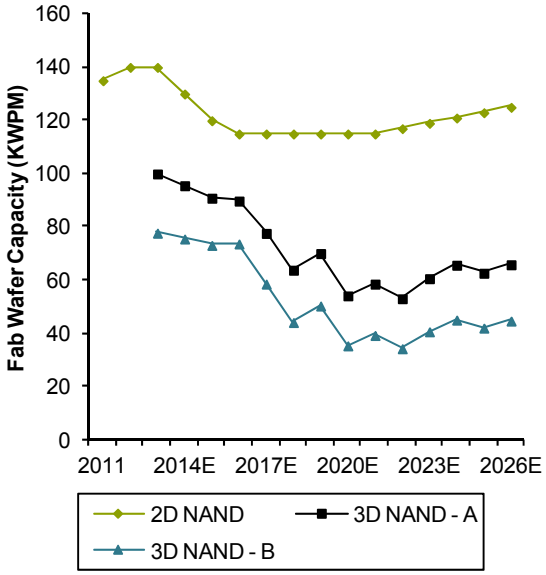
Source: ITRS and Bernstein estimates and analysis.

Exhibit 223 …Allowing Bit Density to Further Rise for 3D NAND, Overtaking 2D NAND in 2017



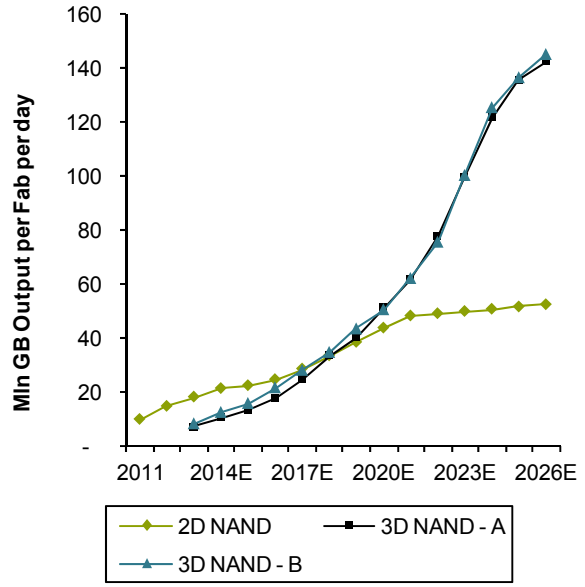
Source: ITRS and Bernstein estimates and analysis.

Exhibit 224 Increased Processing Steps, However, Will Lead to Lower Wafer Output



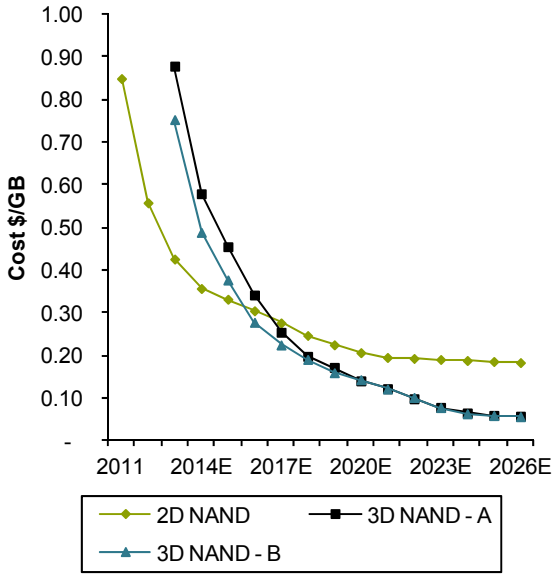
Source: ITRS and Bernstein estimates and analysis.

Exhibit 225 Even So, GB per Fab Will Continue to Increase for 3D NAND, and We Expect Will Surpass 2D NAND by 2018



Source: ITRS and Bernstein estimates and analysis.

Exhibit 226 3D NAND Cost per GB Will Surpass 2D NAND in 2017, Allowing for $0.06 per GB by 2024

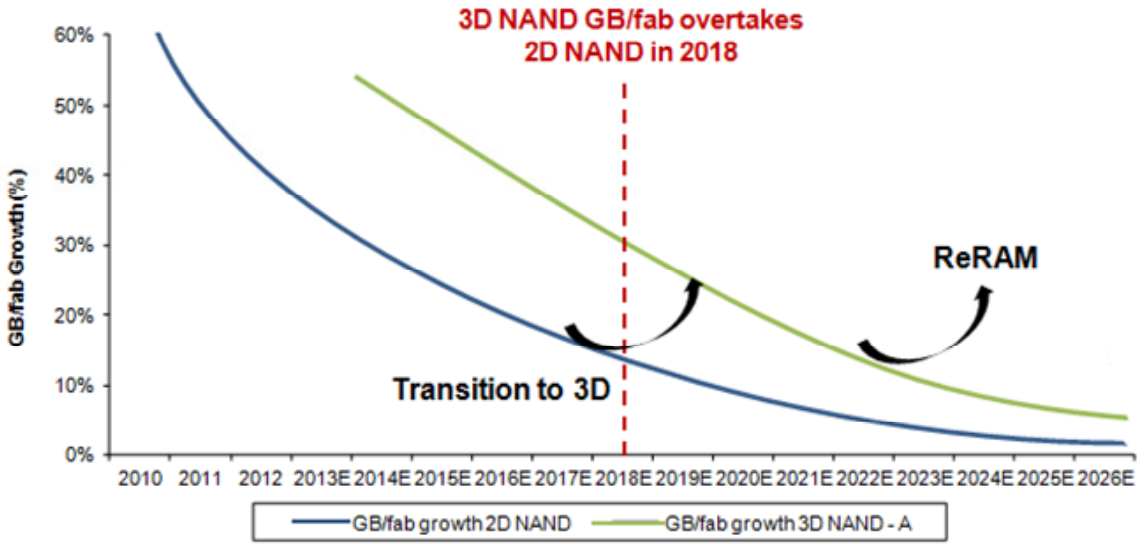


Source: ITRS and Bernstein estimates and analysis.

NAND Supply Growth Fall Will Continue, Even With 3D NAND

Our analysis shows that although 3D NAND will allow the GB/fab growth to continue for another decade, it will never get back to the historical 60% GB/wafer (or GB/fab) growth (see Exhibit 227). Furthermore, 3D NAND will run out of steam around 2022 and will require a new technology to continue the supply growth.

Exhibit 227 3D NAND Enables NAND Supply Growth to Continue, But Significantly Lower Than Historically and New Technology Will Be Required in Early 2020s



Source: ITRS and Bernstein estimates and analysis.

3D NAND Adds Significant Technological Complexity — Not Mainstream Until 2015-16

3D NAND adds increased complexity in the manufacturing process and increased burden on the NAND controllers too. In manufacturing, the process will move from a lithography-centric production environment to a potentially less expensive but just as complex etch/deposition flow. In particular, due to the huge number of layers (up to ~100), high aspect ratio etch will become the potential gating factor. Equipment companies such as Applied Materials and Lam Research are working closely with NAND makers to solve these issues. In NAND controllers, 3D NAND introduces a new layer of complexity. Failure mechanisms need to be studied and understood, and controllers need to be optimized for this. We expect these issues to take some time to solve.

While 3D structure can be the temporary solution for the imminent problems, it also has its own challenges in solving all of NAND's current problems. 3D NAND's production yield is very low due to its complex structure. Under current technology, the multi-stack patterning is extremely difficult to stabilize and its particular design makes it very demanding to monitor any defects inside 3D structure.

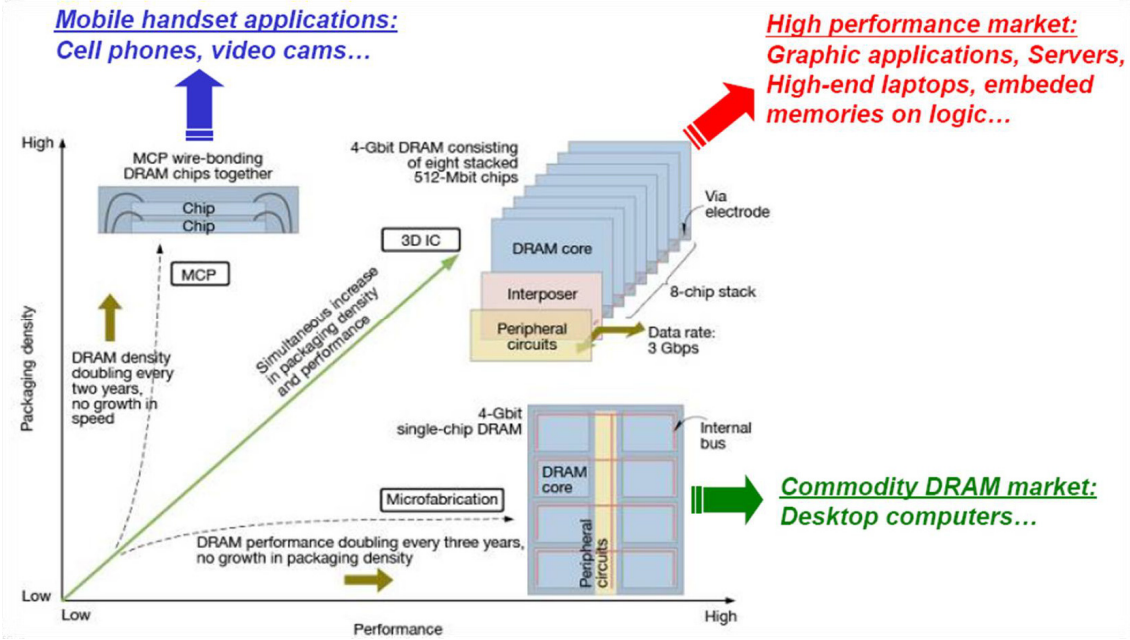
We believe 3D NAND is just a temporary solution to scaling issues, but will not become mainstream until 2015-16. Risks to this include companies' execution on 2D NAND scaling and ability to ramp expertise in 3D NAND. Even so, 3D NAND cannot be the ultimate solution for scalability challenge; rather a complete new memory is required to solve all these problems.

3D DRAM Uses TSV to Increase Performance and Density, But Does Not Help Bit Growth or Costs

DRAM is also facing scaling limitations. This is pushing companies to look at different ways to improve cost and performance. However, the current solution for DRAM is a little less exciting as it doesn't really help the cost side of the equation.

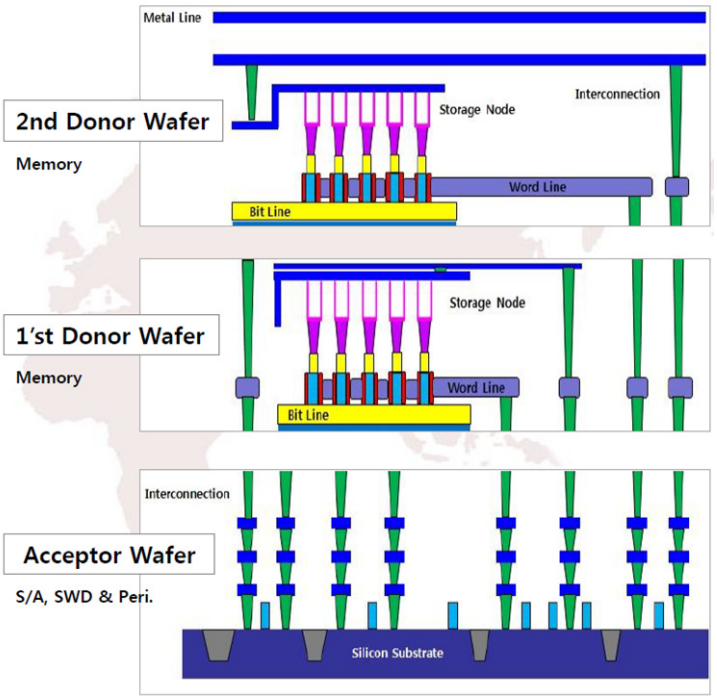
3D stacked die using through-silicon vias (TSV) are used to vastly improve performance through super-fast interconnects. This also improves power consumption and allows for more dense DRAM solutions. However, it does not help on the cost side.

Exhibit 228 3D DRAM Using TSV Boosts Packaging Density and Performance



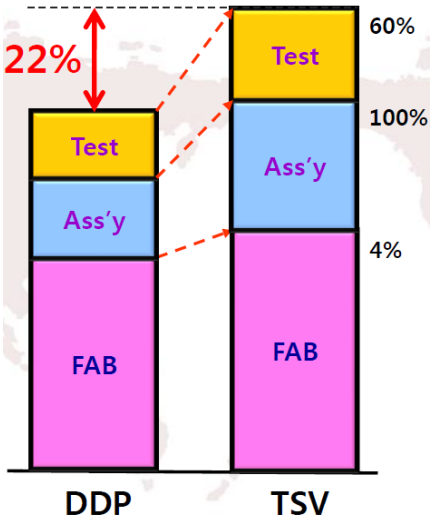
Source: SK Hynix.

Exhibit 229 3D DRAM — Wafer Stacking



Source: SK Hynix.

Exhibit 230 However, TSV Costs 22% More Than Dual Die Package



Source: SK Hynix.

New Memory Technologies Are Needed to Extend Scaling in the Next Decade

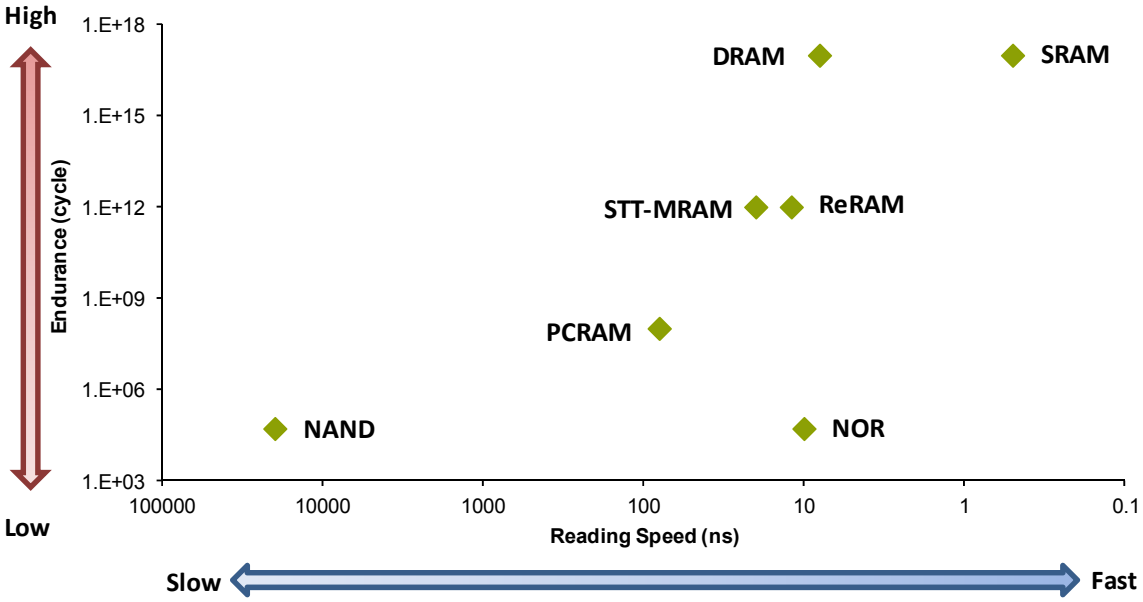
We See Several Interesting New Memory Technologies on the Horizon

The limitations of conventional memory devices have provoked needs for new memory technologies (see Exhibit 231), and currently, there are many types of new memories that are being developed by both research institutions and commercial semiconductor tycoons. While they differ vastly in terms of development stage and commercialization viability, we find several interesting new memory technologies on the horizon. Exhibit 232 through Exhibit 234 summarize the new technologies and major characteristics of each, together with the existing memory types. We discuss some of the major emerging technologies in more detail later.

Exhibit 231 Limitations of Conventional Memory Devices Lead to a Development of New Memory

Source: SK Hynix.

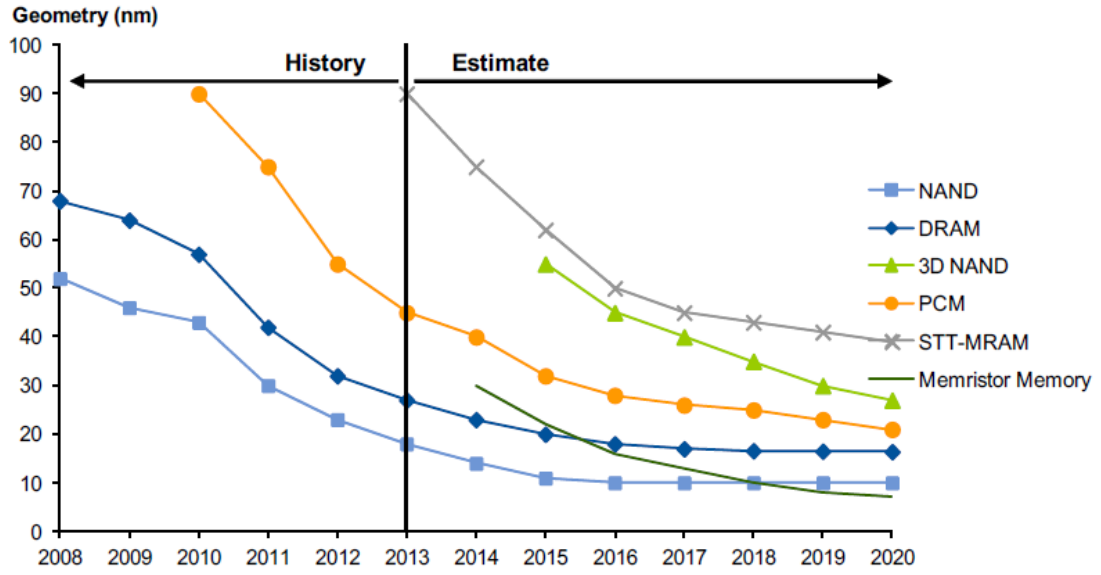
Exhibit 232 Endurance and Performance Comparison for Memory Technologies



Source: Gartner.

Exhibit 233 depicts historical geometry advancement and forecast by memory types. Outside of DRAM and NAND, only PCRAM has been commercially available so far, but its current geometry (~45nm) has lagged far behind the conventional memories due to difficulties in scalability. For other emerging technologies, ReRAM is expected to go commercial by late 2014 with ~30nm node. Its flexible scalability allows the shrink in node sizes much faster for ReRAM than any other emerging memories, and it is expected to eventually surpass NAND's geometry by 2018. On the other hand, STT-MRAM has issues sustaining STT switching characteristics at lower nodes, and we expect its node migration will be the slowest.

Exhibit 233 **Migration Timeline for the Mainstream and Emerging Memory Technologies**



Source: Gartner.

Exhibit 234 summarizes key characteristics of some future memory technologies that we discussed earlier. Boasting the best scalability, lowest production cost, lowest power consumption and plausible manufacturability, we believe ReRAM has the largest potential to become the next mainstream memory, most likely replacing NAND flashes.

Exhibit 234 **Summary of Characteristics by Memory Types: We See ReRAM Has the Biggest Potential to Grow as the Next Mainstream Memory**

	Mainstream Technologies		Emerging New Memories		
	DRAM	NAND	ReRAM	PCRAM	STT-MRAM
Scalability	15nm	12nm	<10nm	25nm	40nm
Cost/Gb	$6.00	$0.50	Potentially lower than NAND	Similar to DRAM	Highest
Reading Speed	Fastest	Slowest	Very Fast	Slow	Fast
Endurance (cycles)	1.0E+17	1.0E+04	1.0E+12	1.0E+08	1.0E+12
Non-Volatile	No	Yes	Yes	Yes	Yes
Power Consumption	Highest	Low	Lowest	Higher than NAND	Lower than NAND
Manufacturability	Mass Production	Mass Production	Compatible	Changes Needed	Incompatible
Conclusion	No Perfect Replacement	Expect 3D NAND Then Replaced By ReRAM	Replace NAND by ~2018	Niche	Niche

Source: Gartner and Bernstein analysis.

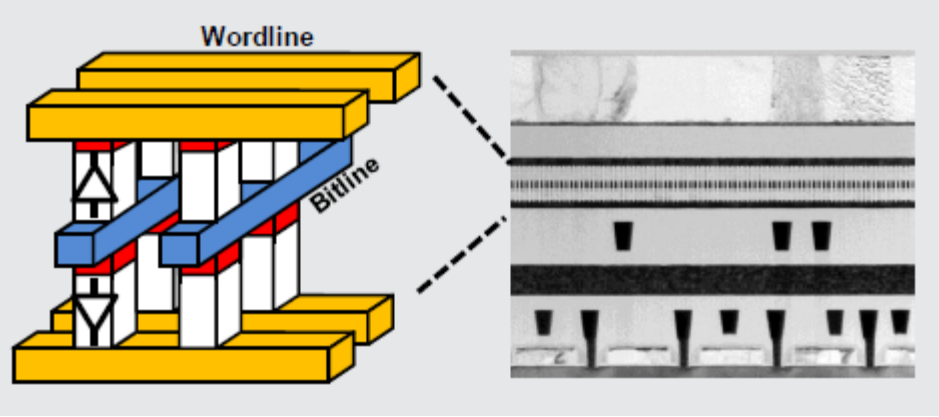
In the following sections, we introduce some of the major emerging technologies, including ReRAM, PCRAM, STT-MRAM and NRAM.

Resistive Random-Access Memory (ReRAM or RRAM) — Potential NAND Replacement

Resistive random-access memory (ReRAM or RRAM) utilizes a dielectric material, which is sandwiched between two electrodes. When a sufficiently high voltage is applied across the cell, a filament forms in the dielectric and lowers the resistance of the cell (see Exhibit 235). The wire can be broken by reversing the voltage, therefore increasing resistance. It stores data using cell resistance — a filament lowers the resistance (binary 1) and a cell without a conductive filament is high resistance (binary 0).

ReRAM can read and write much faster than PCRAM and STT-MRAM, and requires lower voltages. It has the potential to replace NAND going forward, and there is research going on to improve its endurance further to make the new technology suitable for wide adoption in applications. This is not available in the market yet, but Hewlett-Packard, in collaboration with Hynix, is aiming for commercial manufacturing of its memristor-based ReRAM starting from the end of 2013. Following Hewlett-Packard, there is SanDisk, but we expect the earliest possible commercial production to commence in 2015 as SanDisk's technology will most likely incorporate EUV in the manufacturing process.

Exhibit 235 **Structure of 3D ReRAM — ReRAM Utilizes a Dielectric Material, Which Is Sandwiched Between Two Electrodes**



Source: SanDisk.

PCRAM — Potential DRAM or NOR Replacement

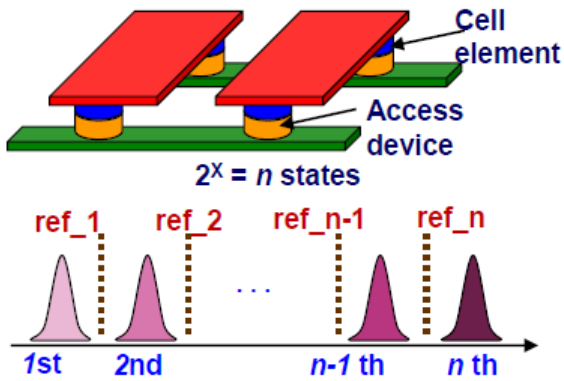
Phase-change memory (PCM or PCRAM) is a non-volatile type random-access memory that utilizes chalcogenide glass as a mechanism of action. Heat produced by the passage of electric current switches the glass between two states — crystalline (low resistance) and amorphous (high resistance) — and stores data (see Exhibit 236).

PCRAM is emphasized as a potential substitute of NAND and to some extent DRAM, thanks to its high durability, fast read and random-access ability. PCRAM does degrade with use, but it can theoretically endure 100 million write cycles — extremely higher durability than flash. Also, it does not require erasing an entire block of cells to have new data to be stored in each cell.

However, as the switching process is thermal, PCRAM is very sensitive to temperature and the process requires a relatively large amount of power.

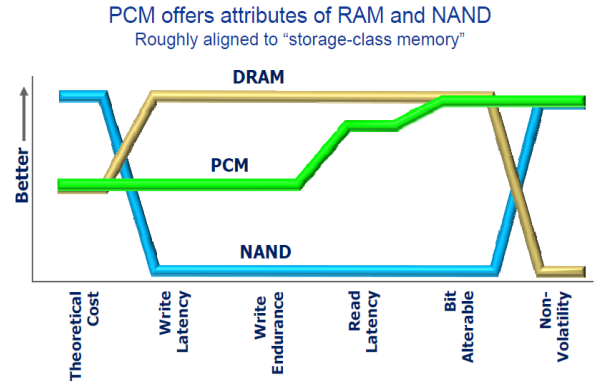
It is already commercially available at Micron, but at a very small quantity and sizable premium in terms of price. Despite several advantages, we believe PCRAM is likely to penetrate only into niche markets as its slower performance than ReRAM and worse scalability than NAND prevent it from becoming a perfect replacement for either NAND or DRAM (see Exhibit 237).

Exhibit 236 PCRAM Structure



Source: SK Hynix.

Exhibit 237 PCRAM Is Proved to Be at Least Equal or Better Than NAND in Every Aspect But Cost — the Biggest Drawback Why It Can't Completely Replace NAND



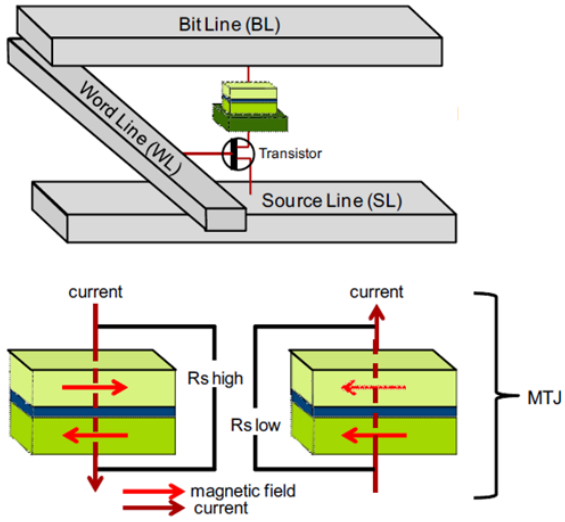
Source: Micron .

Spin-Transfer Torque Memory (STT-MRAM) — Potential DRAM or SRAM Replacement

STT-MRAM, an advanced version of magneto-resistive RAM (MRAM), shows a huge improvement over the previous MRAM. Its use of spin-polarized current instead of magnetic field significantly lowers power consumption when switching magnetization of storage layer and thus leading to a high endurance (see Exhibit 238).

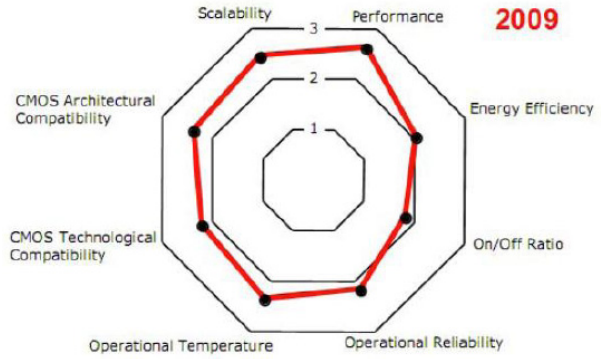
Due to its high performance and endurance and similar electrical interface, STT-MRAM is often identified as the most feasible replacement option for SRAM in future devices (see Exhibit 239). It is expected to solve SRAM's limitations that we have encountered during its scaling-down attempts, such as leakage, reliability problem and device mismatch. However, the speed of current STT-RAM is yet to be comparable to SRAM and research is on to improve the matter.

Exhibit 238 STT-RAM Uses Spin-Polarized Current Instead of Magnetic Field



Source: Gartner.

Exhibit 239 STT-RAM Has Advantages in Performance and Scalability



Source: Samsung (Grandis).

Nano-RAM (NRAM) — An Alternative to Replace NAND After 2018

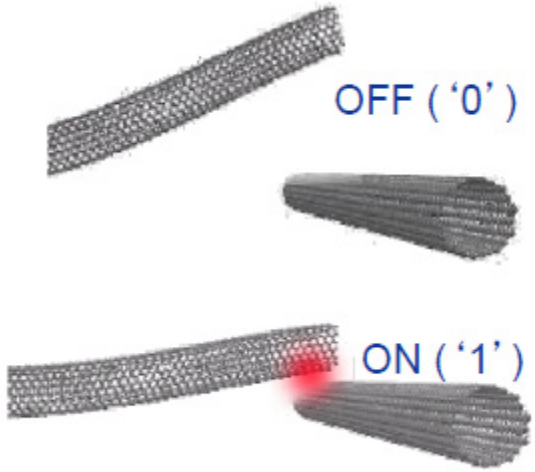
NRAM is another type of potential mainstream memory that has characteristics of both DRAM (random-access) and NAND (non-volatile). The basic structure of NRAM consists of a non-woven fabric matrix of carbon nanotubes (CNT), where tubes attract and resist each other depending on the resistive state. A few advantages that it has over the conventional memory types are namely low power consumption, high endurance and better scalability (see Exhibit 240 and Exhibit 241).

Unlike DRAM, it does not require power to refresh and retain data and therefore it is non-volatile. Also, it uses simple touch/un-touch switching mechanism between CNTs, which makes it more energy efficient than NAND, which demands a high voltage to erase data. The microscopic characteristics of tubes allow NRAM to go beyond the existing memories in terms of scalability.

These characteristic of NRAM hint at the possibility of its universal usage in the future electronic devices, replacing both DRAM and NAND, potentially SRAM as well, which will give assemblies a huge advantage in terms of space.

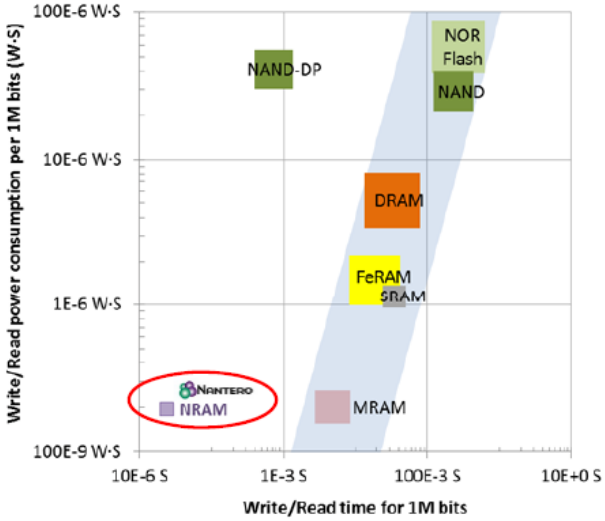
Nantero is the leading advocate of this new technology but commercial production of NRAM has not taken place yet due to cost constraints.

Exhibit 240 NRAM Utilizes Fabric Matrix of Carbon Nanotubes, Where Resistance Varies Depending on Whether It's in Physical Contact or Not



Source: Nantero and Bernstein analysis.

Exhibit 241 NRAM Is Allegedly Better in Both Speed and Energy Consumption Than Other Memory Types

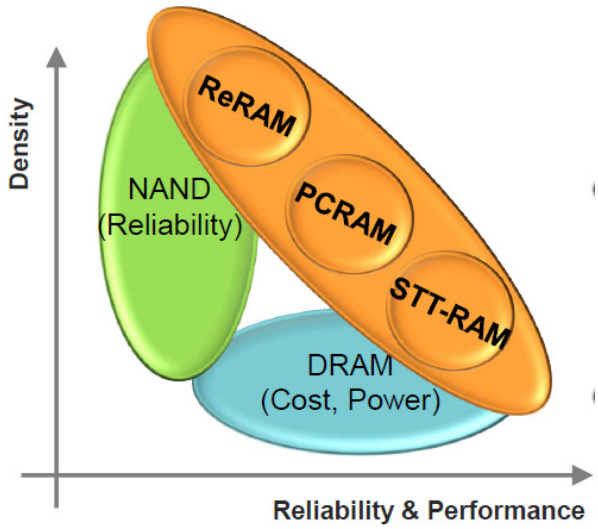


Source: Nantero and Bernstein analysis.

We Believe ReRAM Will Start to Cannibalize NAND and HDD After 2018

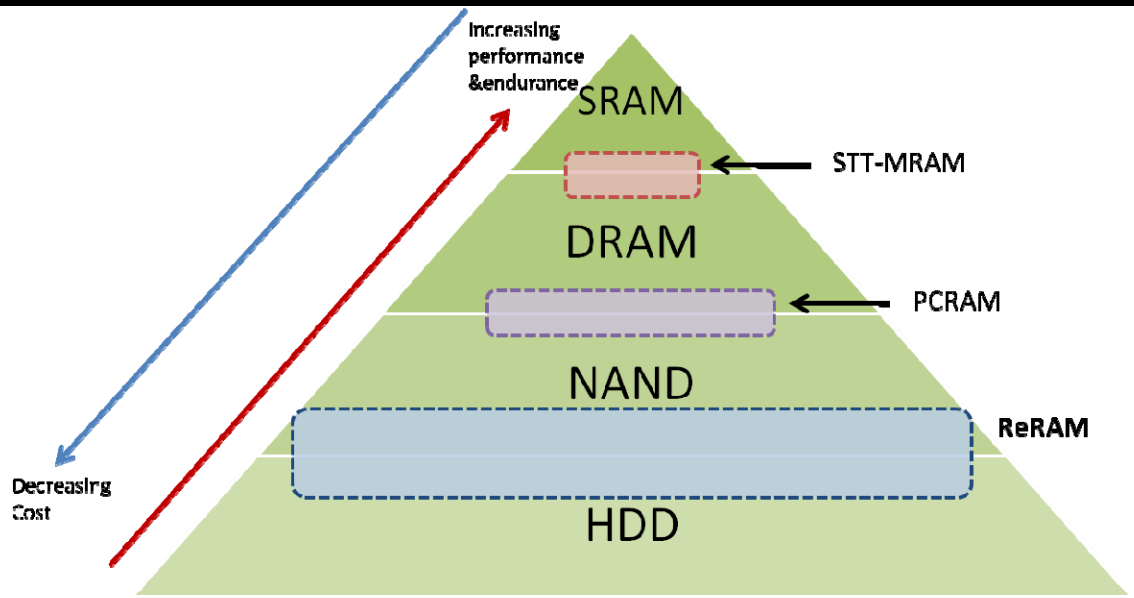
Considering each memory's characteristics and cost issues, the most probable replacement will happen, with STT-RAM replacing SRAM and some DRAM with its strong performance, PCRAM penetrating into devices where DRAM and NAND both are extensively used, and ReRAM for its low cost yet high density replacing storage roles of NAND and HDD (see Exhibit 242 and Exhibit 243). Out of the three emerging technologies, we believe ReRAM has the highest potential to become the next mainstream memory, thanks to its low cost yet high performance.

Exhibit 242 Positioning of Emerging Memory Technologies



Source: SK Hynix.

Exhibit 243 Future Memory Positioning: We Believe ReRAM Will Become the Next Mainstream Memory, Overtaking the Sweet Spot Between NAND and HDD



Source: SK Hynix and Bernstein estimates and analysis.

Backend — Never a Beneficiary, Potentially a Victim?

In this chapter, we analyze how the IC backend industry, in particular packaging, will be strategically different in the future as the economy of Moore's Law suffers a slow death.

Unlike the wafer manufacturing industry, the semiconductor packaging industry does not have the equivalent of Moore's Law. The packaging industry indeed continues to innovate and create value, but the pace of technology advancement is slower than that of Moore's Law. The wafer manufacturers therefore demonstrate much stronger growth than the IC assembler in revenue and profitability, and are better rewarded by investors.

The two industries also have very different competitive dynamics. Foundry is a business in which the winner takes all, as technology leadership is crucial to high profit, which further propels R&D to sustain technology leadership. In the OSAT[9] industry, on the other hand, the absence of Moore's Law and the lower capital requirements make technology and scale much less critical, and high return-on-investment is mostly driven by operation efficiency.

Recently, as the challenges of Moore's Law mount, foundries have begun to explore other means to sustain the growth momentum, most notably by bringing wafer-/silicon-based technologies into packaging. As a result, the long-held symbiotic relationship between foundries and OSATs is put under unprecedented stress.

In the near term, bumping, a wafer-based process, is gaining popularity due to the adoption of flip chip. Bumping can be performed at foundries or OSAT companies. However, it counter-intuitively does not create tension between foundry and OSAT because of low investment returns. The rest of the flip chip package process is quite profitable but foundries have no interest in this. We believe that flip chip adoption in mobile applications is the most important technology trend in the OSAT industry in the next one to two years. SPIL, in particular, has high exposure to this trend and therefore is the top pick of our coverage.

In the long run, 2.5D/3D IC shifts value from OSAT and substrate sector to foundries. It is arguably the most promising technology in the "mid-end." As many wafer manufacturers invest heavily to develop this technology, we've seen growing friction between foundries and the OSAT companies. We however believe that high cost will keep it from mass adoption in the near future, and that the current concern of the value shift is unwarranted. Among Intel, TSMC and Samsung, we think the vertical integration at Intel and Samsung will help them bring 2.5D/3D technology earlier to the market, while TSMC risks falling behind.

In conclusion, the absence of Moore's Law is no guarantee that the backend industry can survive the slowing of Moore's Law unscathed. The ramifications, however, can be very different depending on investment horizon. Near term, we're comfortable with the growth outlook of ASE and SPIL in light of their exposure to mobile applications and flip chip. We expect the subtle balance between foundries and OSATs in bumping will remain. Medium term, 2.5D/3D IC will remain too expensive to become a meaningful headwind on OSATs. We project it will not be a significant growth area for foundries either. Long term, the emergence of "mid-end" likely will tilt the competitive landscape to favor foundries. However, we remain doubtful this will be able to fully offset the mounting burden in the core business as the slow death of Moore's Law takes its toll.

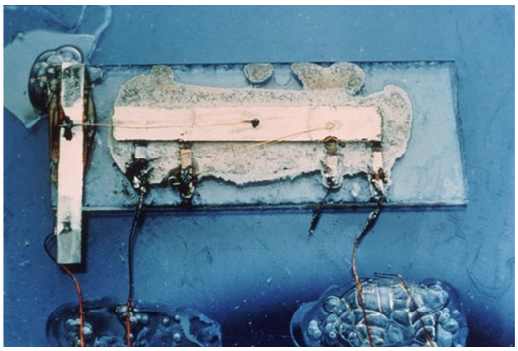
[9] OSAT = Outsource Semiconductor Assembly and Test.

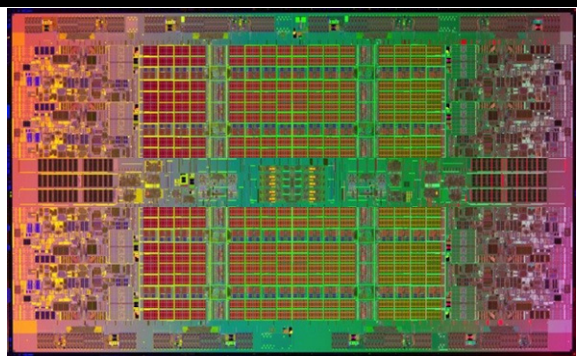
Unlike Wafer Manufacturing, the Semiconductor Packaging Industry Does Not Have the Equivalent of Moore's Law

Unlike wafer manufacturing that enjoys decades of constant cost, performance and power efficiency improvement from Moore's Law (at least until we begin to mourn its slow death lately), the semiconductor packaging industry does not have the equivalent of Moore's Law.

Since the first transistor was invented by Texas Instruments' Jack Kilby in 1958, Moore's Law has been going like clockwork and has shrunk transistor size by ~100 million times (see Exhibit 244). More and more transistors are packed in a chip to deliver ever-rising performance and functionality to consumers with more affordable pricing (see Exhibit 245).

Exhibit 244 Over the Last 50+ Years, Transistor Count Has Doubled Every Two Years





54yrs

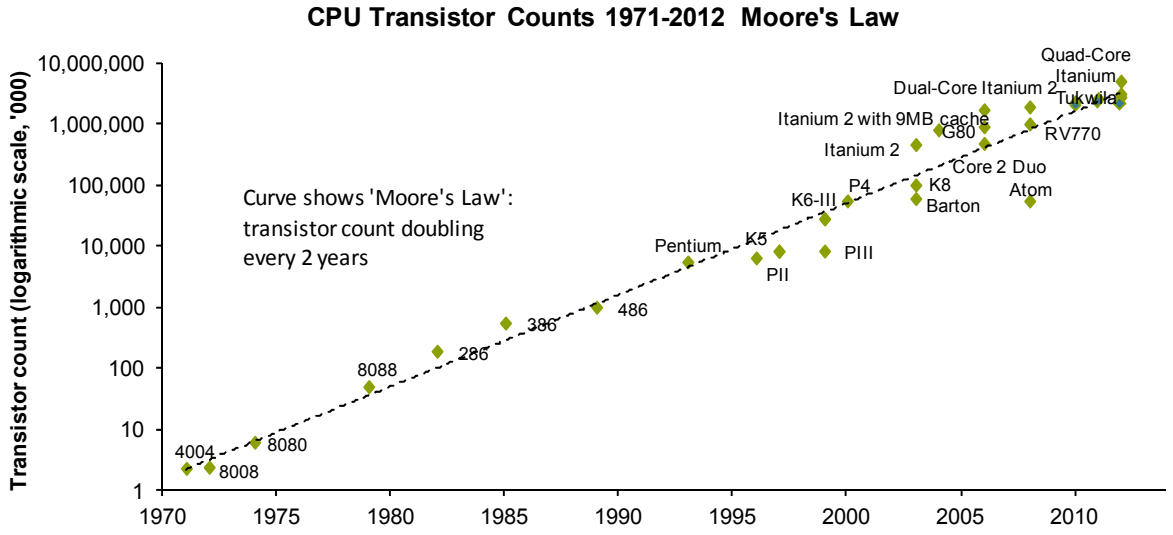
1958
Jack Kilby's design of first IC
1 transistor
~18mm^2 area

2012
Intel's 8-Core Itanium Poulson
3.1bn transistors
544mm^2 area

0.06 transistor per mm^2 → **~6 million transistor per mm^2**

Source: Intel, Wikimedia Commons and Bernstein estimates and analysis.

Exhibit 245 **Moore's Law Held True Throughout This Period, as Transistor Count Inside a CPU Continued to Double Roughly Every Two Years**

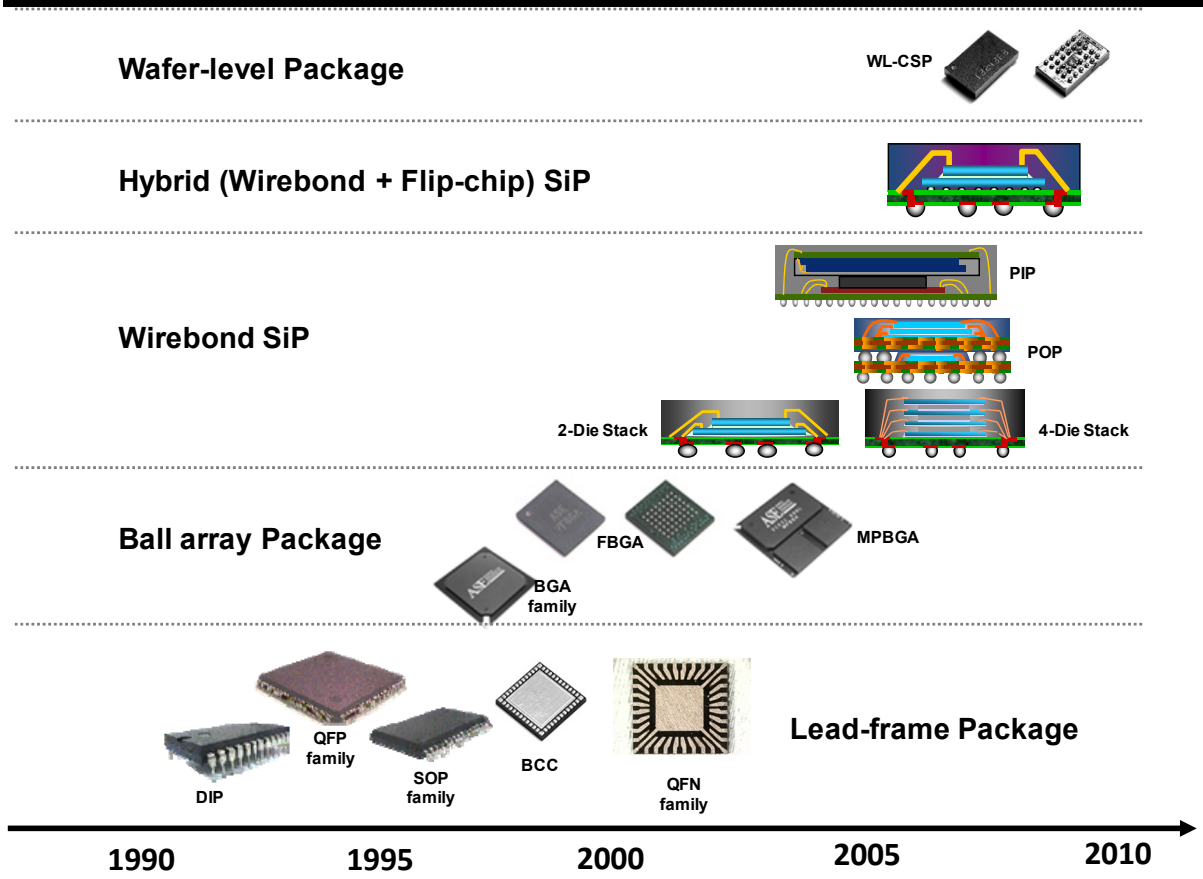


Source: Intel and Bernstein analysis.

However, the semiconductor packaging industry, like many other industries, does not enjoy the luxury of Moore's Law. One reason why Moore's Law works in wafer manufacturing is that digital logic in the integrated circuit is an abstraction, so the physical size does not matter and can be shrunk. Packaging instead has to physically connect the integrated circuit to the external world and has to observe certain size restrictions. Wafer manufacturing also enjoys the benefit of wafer-level batch processing: as many chips are manufactured on one wafer, the cost of each chip decreases as wafer size increases and chip size shrinks. IC packaging, on the other hand, has to individually handle each chip for most of the process until the recent emergence of wafer-level package (WLP) (see Exhibit 246).

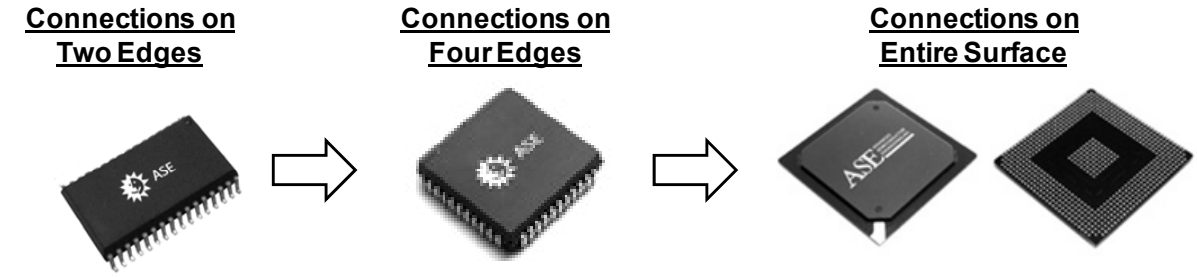
The semiconductor packaging industry indeed has been steadily innovating and creating value. For example, by moving the connection pins on two edges to four edges and to the entire surface, more connections can be made in the same IC area (see Exhibit 247). Moving from wirebond to flip chip is another innovation to further reduce the entire packaged IC size (see Exhibit 248). The development of SiP (system-in-package) further enhanced the capability to package multiple dies together, achieving higher levels of integration and increased functionality (see Exhibit 249), etc. The pace of technology advancement, however, is slower than that of Moore's Law.

Exhibit 246 Until the Recent Emergence of Wafer-Level Package (WLP), IC Packaging Has Been Done Most on "Unit" Basis and Does Not Leverage Wafer Manufacturing Infrastructure and the Advances of Moore's Law



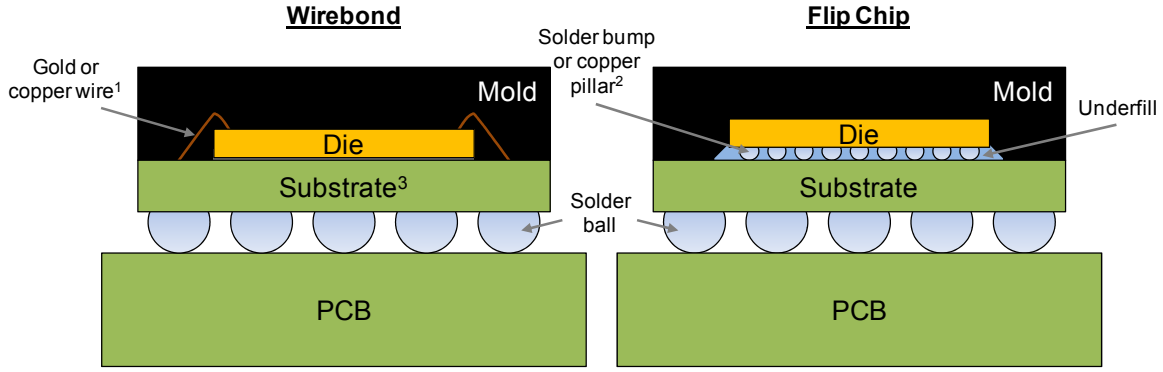
Source: ASE and Bernstein research.

Exhibit 247 Technology Moved from Connections on Just Two Edges, to Four Edges and Now to the Entire Surface of the Package



Source: ASE and Bernstein research.

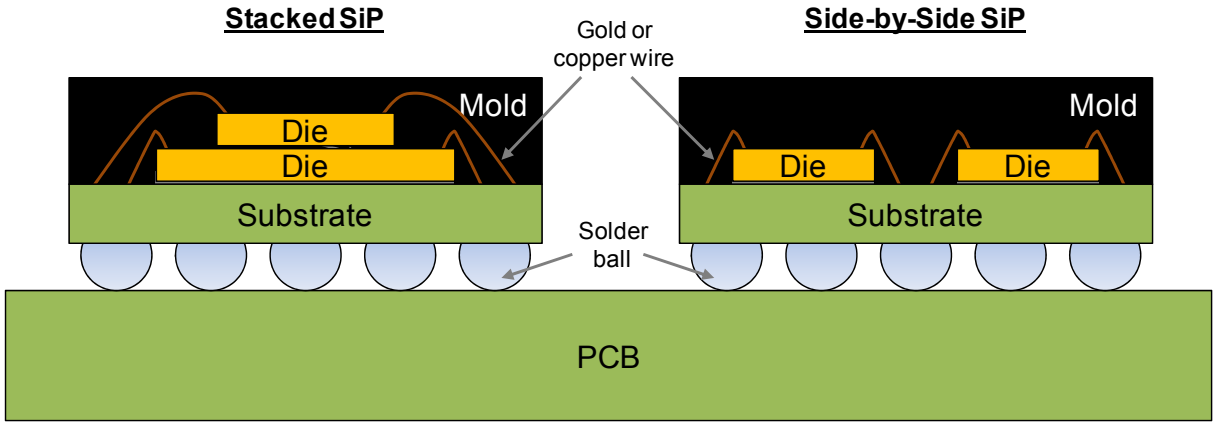
Exhibit 248 **Flip Chip Can Support Much More Complex Chips With More Connections Than Wirebond by Utilizing the Entire Silicon Surface**



Note: 1) Gold and copper wires are commonly used in wirebond. 2) "Bumps" in flip chip are mostly made of solder. Solder bumps can also be replaced with copper and then are referred as "copper pillars." 3) Both substrate and leadframe can be the package carrier in an IC package. Substrate is used in this chart for illustration purposes.

Source: Bernstein research.

Exhibit 249 **SiP (System-in-Package) Handles More Interconnections Inside a Package But Is Not Based on Shrinking Physical Feature Size in Silicon (i.e., Moore's Law)**



Source: Bernstein research.

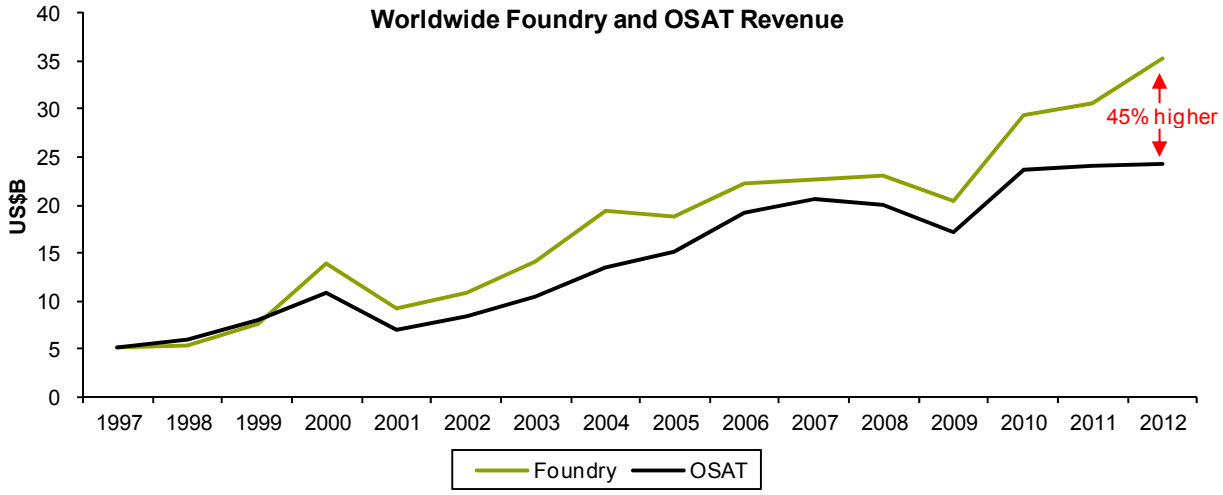
As a Result, the Two Industries Have Different Growth, Market Valuation and Economics

The wafer manufacturers, i.e., foundries, therefore demonstrate much stronger growth than the IC assemblers (i.e., OSAT). fifteen years ago, the two industries were equal in size. But as of 2012, foundries have grown to be 45% larger than OSATs (see Exhibit 250). The difference is even more pronounced when profitability is considered. TSMC, the leader in foundries, has enjoyed 28% ROIC on average in the past 10 years, while ASE, the leader in OSAT, only had 7% (see Exhibit 251).

As the result, the two industries are rewarded very differently by investors as well. The combined market cap of TSMC, UMC and SMIC is almost 10 times bigger than that of ASE, Amkor, SPIL and STATS ChipPAC[10] (see Exhibit 252).

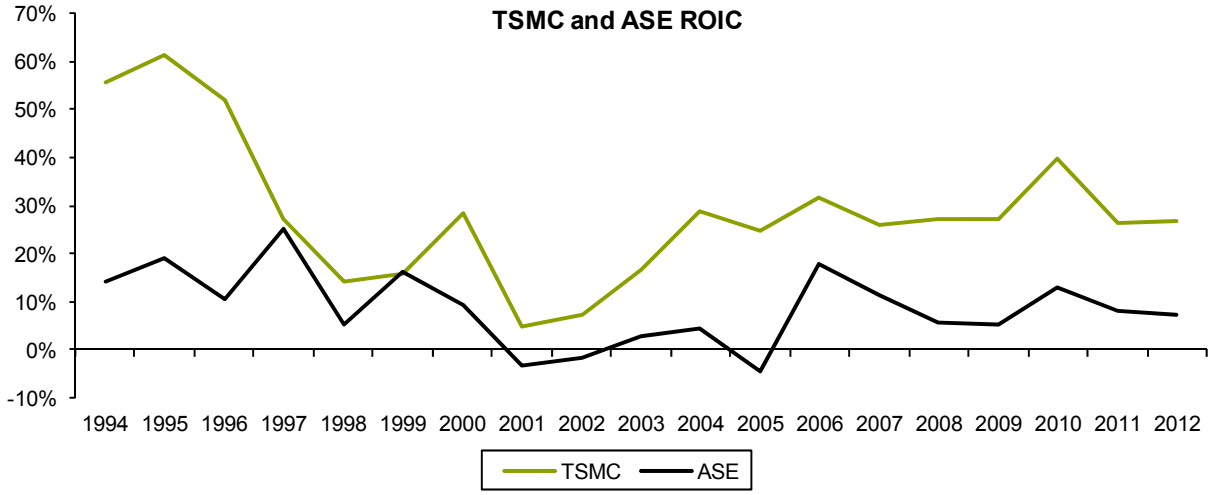
[10] TSMC, UMC, and SMIC are No. 1, No. 3 and No. 4 foundry companies in terms of 2012 revenue. Collectively, they have 73% of market share. No. 2 foundry, GlobalFoundries, is private and therefore is not included in market cap calculation. ASE, Amkor, SPIL and STATS ChipPAC are the top four OSATs and collectively had 46% of market share in 2012.

Exhibit 250 **In the Past 15 Years, Foundry Industry Has Grown to be 45% Bigger Value Than OSAT**



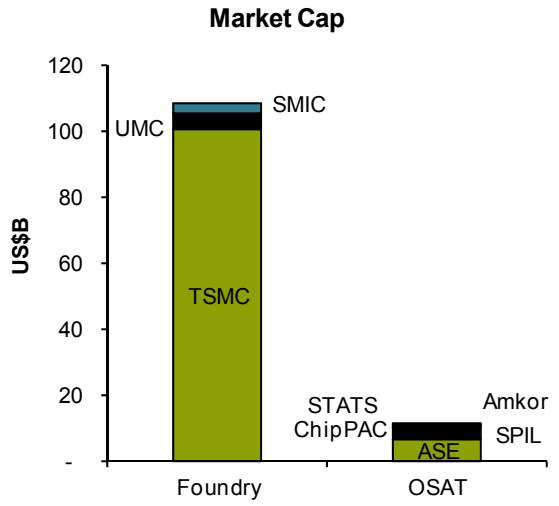
Source: Gartner and Bernstein analysis.

Exhibit 251 **TSMC Has Enjoyed 28% ROIC on Average in the Past 10 Years, While ASE Only Had 7%**



Source: Corporate data and Bernstein analysis.

Exhibit 252 The Combined Market Cap of TSMC, UMC and SMIC Is Almost 10 Times Bigger Than That of ASE, Amkor, SPIL and STATS ChipPAC

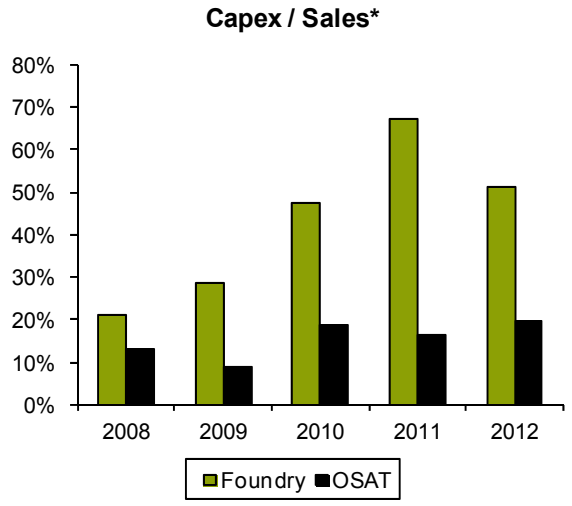


Note: Market caps are as of May 14, 2013.

Source: Capital IQ and Bernstein analysis.

Looking closer, we also find very divergent economics in the two industries. Foundries are much more capital intensive as technologies require highly complex equipment to implement (see Exhibit 253), and depreciation naturally becomes the largest cost component (see Exhibit 254). OSATs, on other hand, have heavier material and labor costs (see Exhibit 255), leading the top four players — all with operations in China — to leverage China's lower labor cost.

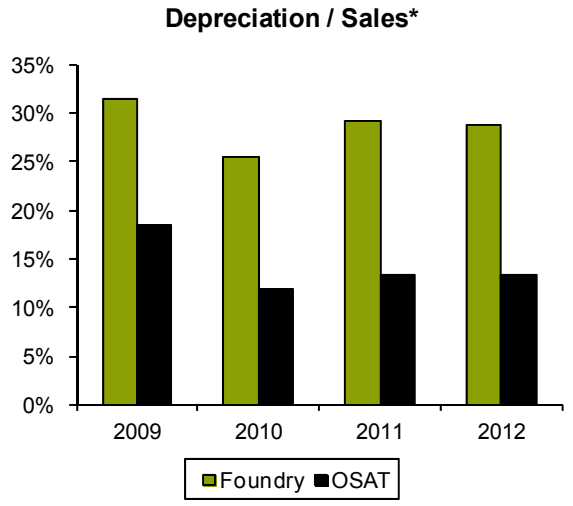
Exhibit 253 Foundry Business Model Requires Higher Capex Intensity…



* Capex/sales for foundry and OSAT are calculated using sales-weighted average of representative companies. Foundry representative companies include TSMC, UMC, GlobalFoundries and SMIC; OSAT representative companies include ASE, SPIL, Amkor and STATS ChipPAC.

Source: Corporate data and Bernstein analysis.

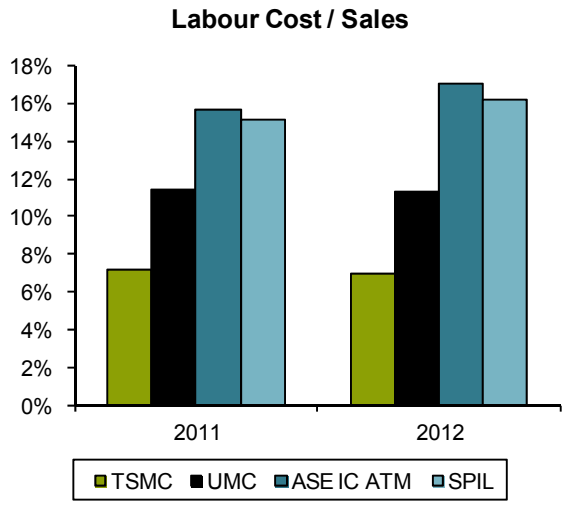
Exhibit 254 …and Hence Higher Depreciation Cost



* Depreciation/sales for foundry and OSAT are calculated using sales-weighted average of representative companies. Foundry representative companies include TSMC, UMC, GlobalFoundries and SMIC; OSAT representative companies include ASE, SPIL, Amkor and STATS ChipPAC.

Source: Corporate data and Bernstein analysis.

Exhibit 255 Labor Cost Is a Bigger Cost Component to OSAT Than to Foundry

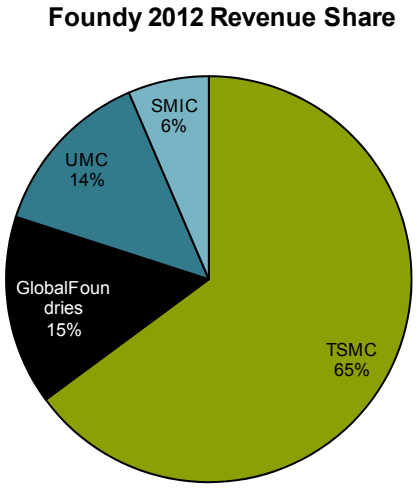


Source: Corporate data and Bernstein analysis.

More Importantly, the Lack of Moore's Law Makes OSATs Compete More on Operation Efficiency vs. Foundry Competing on Technology and Scale

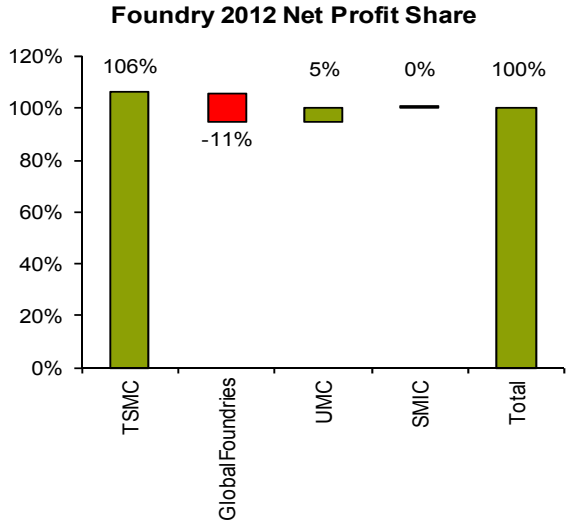
Foundry, in our view, is a business in which the winner takes all. This is evidenced by the fact that TSMC has 65% revenue share but more than 100% net profit share in 2012[11] (see Exhibit 256 and Exhibit 257). In this business, technology leadership is critical to deliver the benefits of Moore's Law earlier than rivals in order to gain share and obtain economy of scale. The profits from economy of scale then enable the leaders to fund next-generation R&D to sustain technology leadership. This creates a positive feedback loop that makes the strong foundry players even stronger (see Exhibit 258). TSMC's rising market share attests to this observation (see Exhibit 259).

Exhibit 256 TSMC Only Has 65% Revenue Share...



Source: Corporate data and Bernstein analysis.

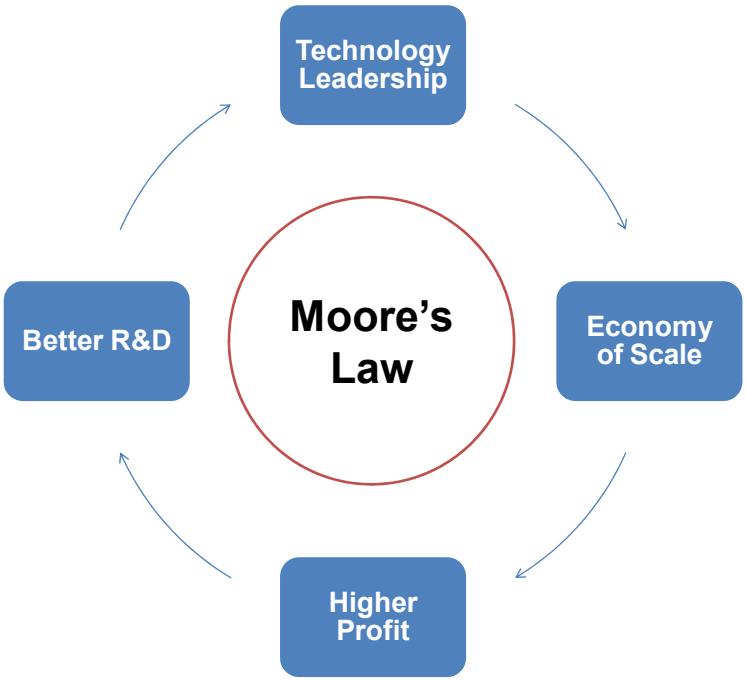
Exhibit 257 ...But Takes More Than 100% of the Profit in the Foundry Industry



Source: Corporate data and Bernstein analysis.

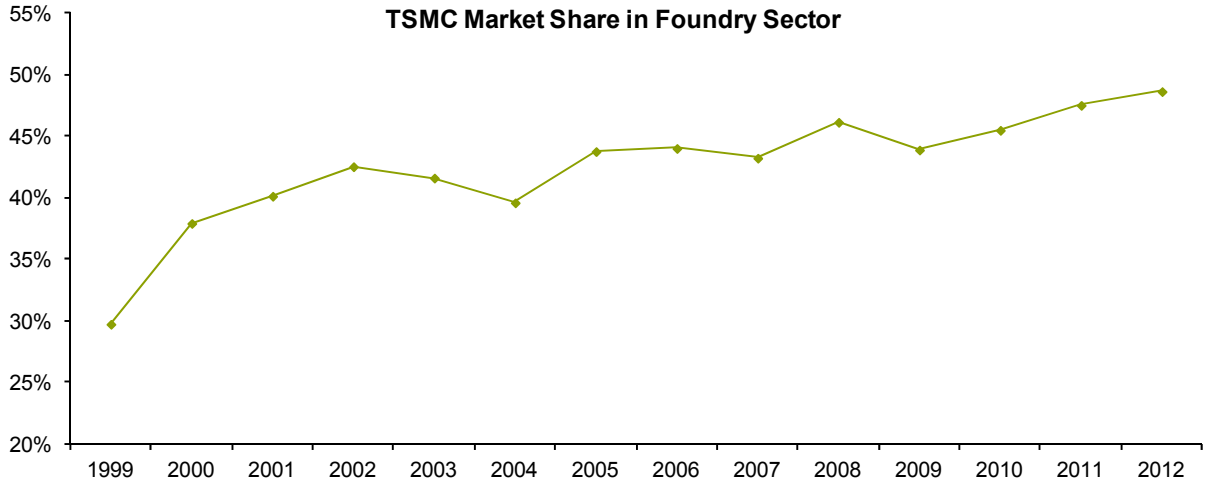
[11] Net profile share is calculated by the total net profile of TSMC, GlobalFoundries, UMC and SMIC.

Exhibit 258 The Positive Feedback Loop Makes the Strong Foundry Players Even Stronger



Source: Bernstein research.

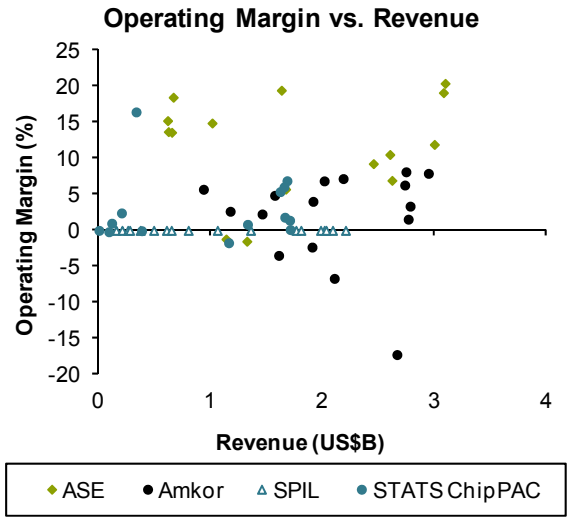
Exhibit 259 TSMC's Market Share Grows Higher and Higher Over Time



Source: Gartner, corporate data and Bernstein estimates and analysis.

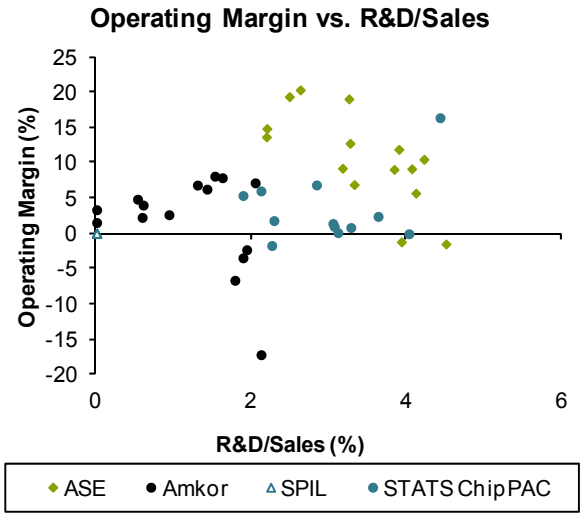
On the other hand, the absence of Moore's Law and the lower capital requirements make technology and scale much less critical in OSAT. Neither R&D intensity nor revenue scale has strong correlation with profitability (see Exhibit 260 and Exhibit 261). There is no sign of the big OSAT players growing bigger either (see Exhibit 262). On the other hand, our long-term analysis shows operation efficiency is the key factor in the return on investment (see Exhibit 263).

Exhibit 260 No Clear Correlation Between Revenue Scale and Operating Margin



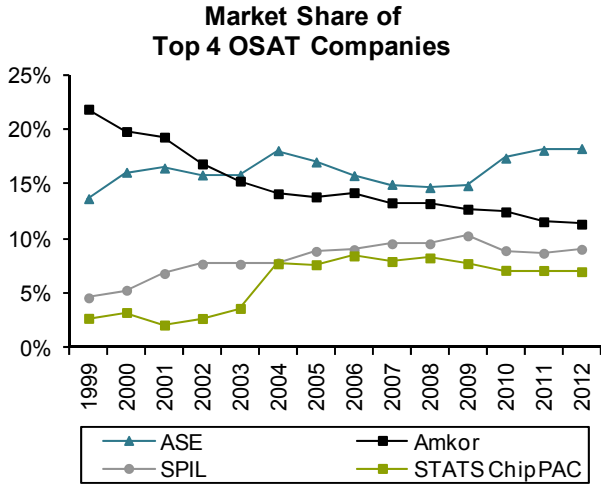
Source: Capital IQ, corporate data and Bernstein analysis.

Exhibit 261 No Clear Correlation Between R&D Intensity and Operating Margin Either



Source: Capital IQ, corporate data and Bernstein analysis.

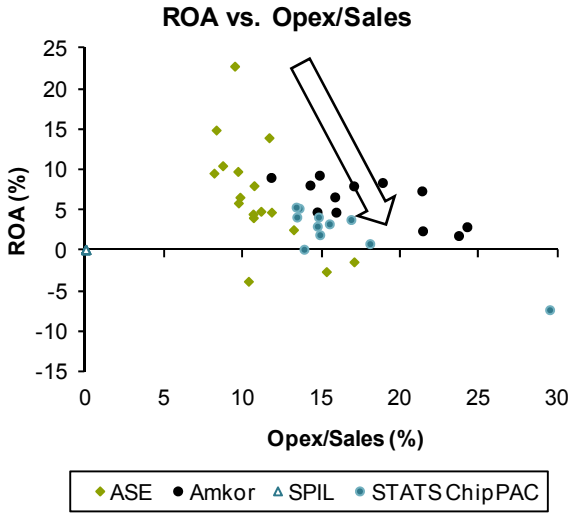
Exhibit 262 Among the Top Four OSAT Players, Market Share Split Is Relatively Stable, Except That SPIL Gains Share and Amkor Loses Share Slowly



Note: STATS and ChipPAC merged into STATS ChipPAC and ASE consolidated subsidiary ASE (Chung Li) and ASE Material in 2004. ASE share post 2010 is ASE IC ATM only (does not count in USI).

Source: Gartner and Bernstein estimates and analysis.

Exhibit 263 The Higher the Operational Efficiency, the Better the ROA Performance



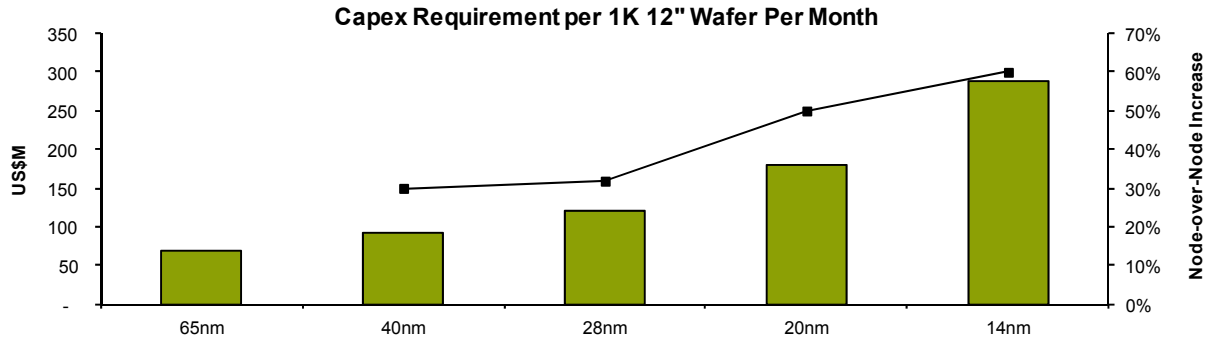
Source: Capital IQ, corporate data and Bernstein analysis.

As the Challenges of Moore's Law Mount, Foundries Have Begun to Explore Bringing Wafer-/Silicon-Based Technologies Into Packaging

Recently, as the challenges of Moore's Law mount, foundries have begun to explore other means to sustain the growth momentum, most notably by bringing wafer-/silicon-based technologies into packaging. As a result, the long-held symbiotic relationship between foundries and OSATs is put under unprecedented stress.

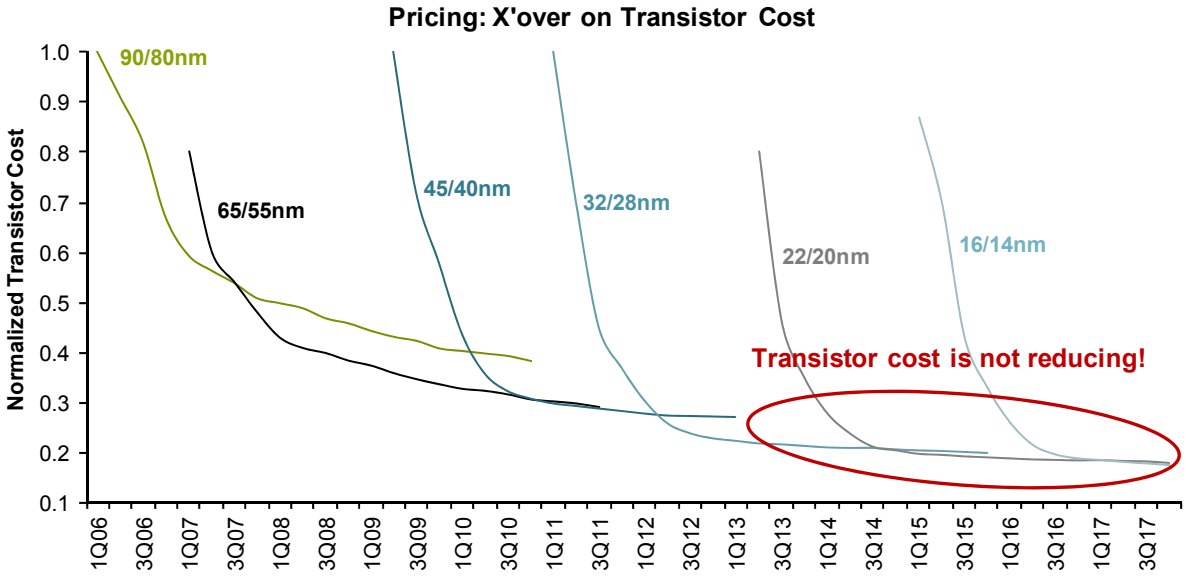
As we discussed in prior chapters, the economy of Moore's Law is suffering a slow death. R&D and capex requirement escalates (see Exhibit 264). The higher capex requirement would transfer to higher wafer cost, which would cut the usual reduction in transistor cost brought by smaller geometry. This diminishing transistor cost reduction has already been felt by fabless companies including Nvidia (see Exhibit 265), AMD, and Qualcomm (see Exhibit 266).

Exhibit 264 **Capex Requirement for Leading Nodes Rises Much Faster Than Before After 28nm**



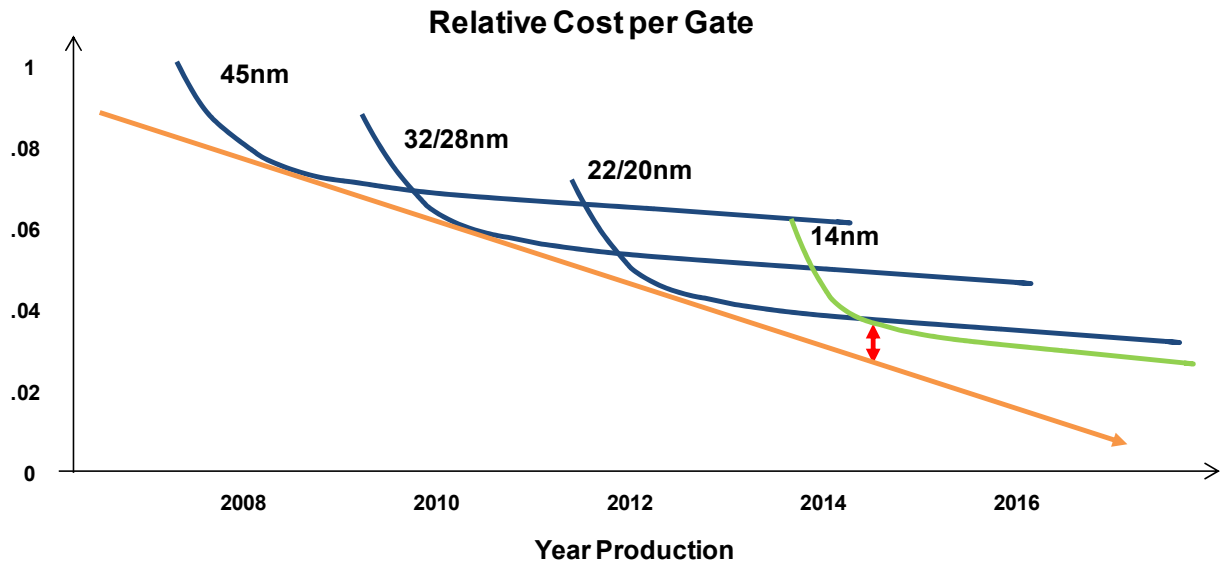
Source: Bernstein estimates and analysis.

Exhibit 265 **Nvidia Finds the Transistor Cost Not Reducing, After Considering Yield, Wafer Cost and Geometry Scaling**



Source: Nvidia and Bernstein analysis.

Exhibit 266 **The Largest IC Fabless, Qualcomm, Also Finds the Cost Reduction Curve from Moore's Law Is Flattening**

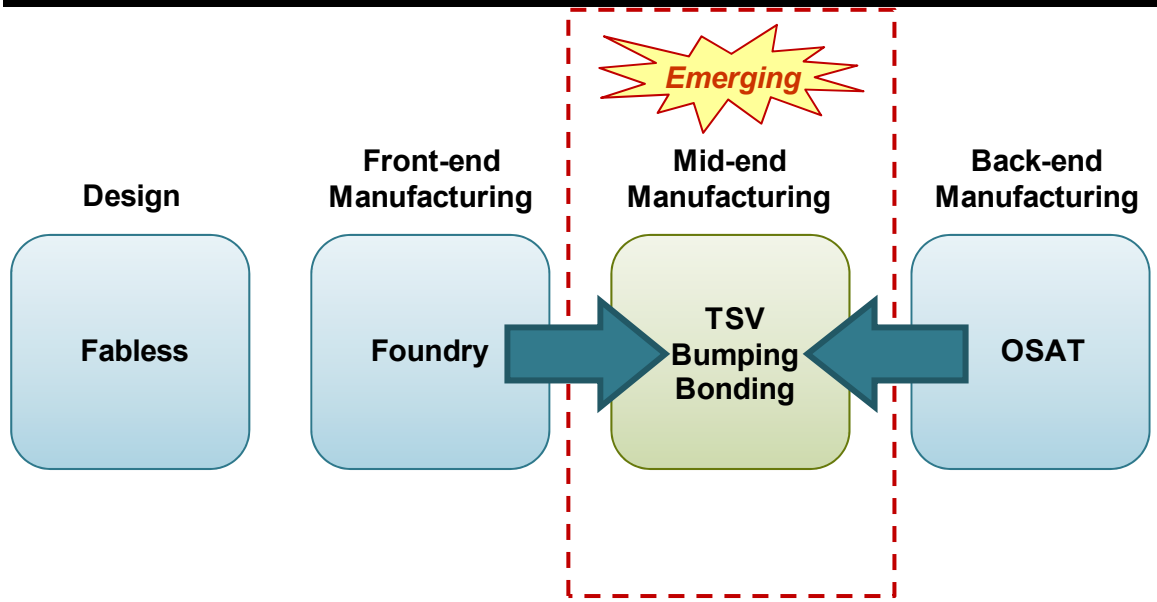


Source: Qualcomm and Bernstein analysis.

Facing the vast uncertainty down the road, foundries begin to explore alternatives to maintain the current trajectory, most notably by introducing Moore's Law into the backend. The fast-advancing silicon technology also naturally finds many possible valuable uses in packaging too. As the result, at the intersection of front-end (i.e., wafer manufacturing) and back-end (i.e., semiconductor packaging), "mid-end" emerges. The mid-end is viewed an important source of growth in the future, but also inevitably becomes the source of rising contention between the two traditionally symbiotic industries today (see Exhibit 267).

Many wafer-/silicon-based technologies are therefore getting more attention from the semiconductor industry and the investor community. We will now discuss two of the most important ones.

Exhibit 267 **As 2.5D/3D IC Technology Incurs New Process Steps in the Middle (i.e., Mid-End), Both Foundry (Front-End) and OSAT (Back-End) Industry Are Vying for That Business**



Source: Bernstein research.

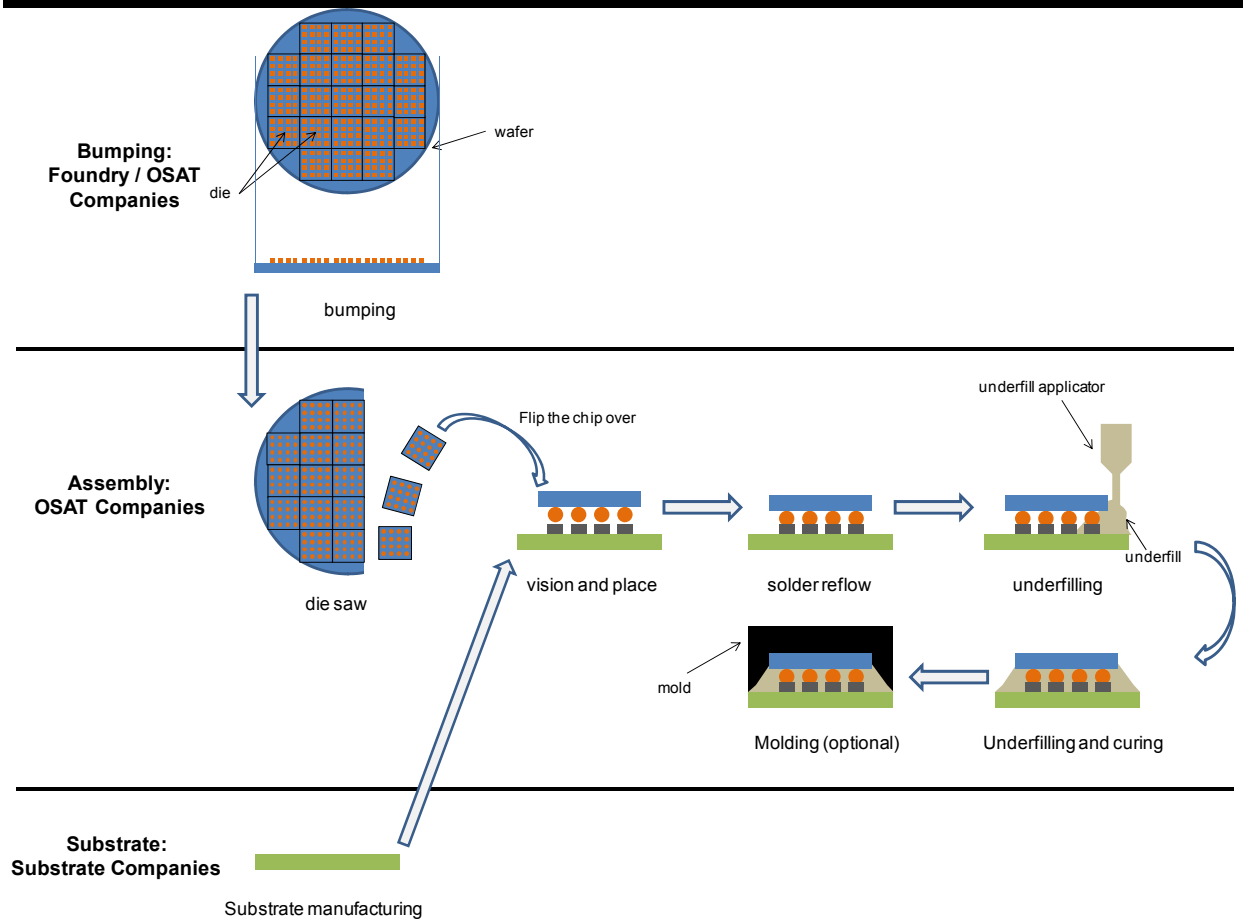
Bumping Is Gaining Popularity Due to the Adoption of Flip Chip, But Its Low Profitability Prevents the Intense Competition Between Foundries and OSATs

In the near term, bumping, a wafer-based process, is gaining popularity due to the adoption of flip chip. Like wirebond, bumping provides interconnections between the die and the package substrate. It is a necessary step of flip chip manufacturing and enables flip chip to support higher interconnection density (see Exhibit 268). The small profiles of today's mobile devices require the ICs to be packaged in smaller sizes. At the same time, the complex logic in the ICs often adds more pin count. The combined effect is the demand of higher interconnection density. In wirebonding, the connection points can only be placed around the edges of a silicon die. Flip chip uses the bumping process to create connection points on the entire surface of a die, increasing the interconnection density and decreasing the package size (see Exhibit 269). As flip chip adoption expands in mobile applications, bumping demand also increases.

In contrast with the unit-based wirebond process, bumping is a wafer-based process and can be performed at foundries or OSAT companies. However, it counter-intuitively does not create tension between foundry and OSAT because of low margins and very interesting competitive dynamics.

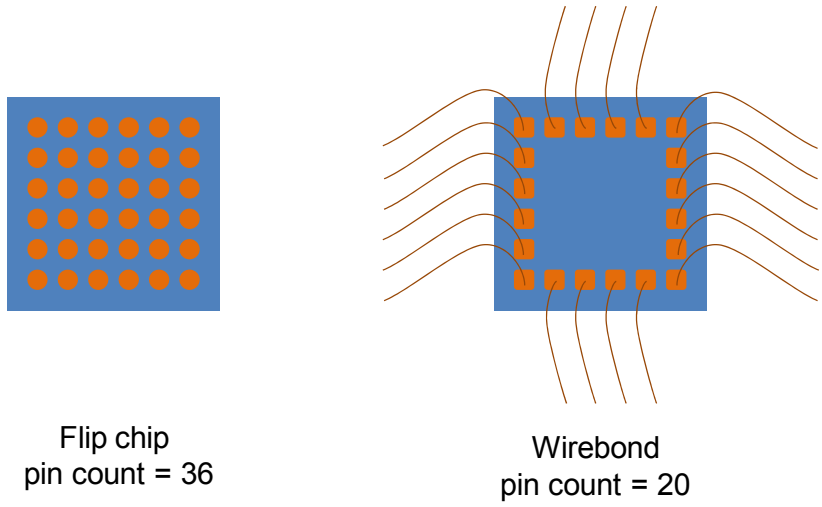
Bumping requires higher capex intensity than most other packaging processes, which drives margins low. However, interestingly, both foundries and OSATs are in this business even with lower margins. For foundries, as accountability is hard to define when third-party bumping damages foundries' costly silicon structure, they, especially TSMC, often provide bumping service just to avoid liability dispute. Low profitability of bumping is a small price to pay when compared with the much more expensive wafer cost. Similarly, OSAT companies, in order to win the lucrative flip chip business, also can tolerate the margin dilution of bumping. These interesting dynamics keep sufficient bumping capacity in the market without animosity between foundry and OSAT.

Exhibit 268 Bumping Is an Important Step in Flip Chip Packaging



Source: Bernstein research.

Exhibit 269 A Simplified Illustration That Flip Chip Pin Count Is Higher Than Wirebond on a Certain Die Size



Source: Bernstein research.

The rest of flip chip package process is quite profitable, but foundries have no interest in this, as its unit-based process does not align with foundry's technologies and infrastructure.

As shown in Exhibit 270, flip chip packaging commands higher margin than wirebonding, even with the zero-margin substrate included. Its higher value added, mostly in performance, protects its higher margin. We believe that flip chip adoption in mobile applications is the most important technology trend in the OSAT industry in the next one to two years. SPIL, in particular, has high exposure to this trend and therefore is the top pick of our coverage (see Exhibit 271).

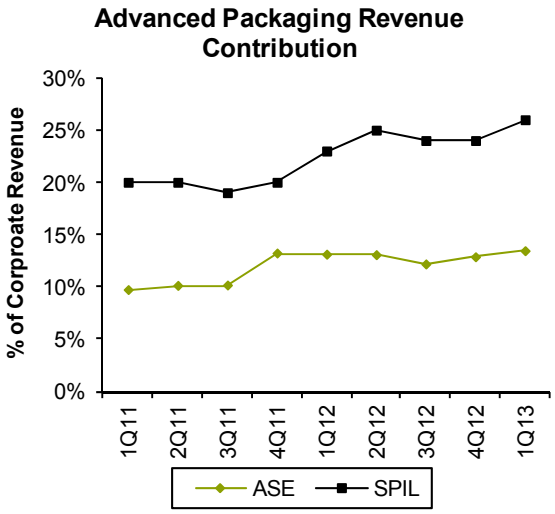
Detailed analysis of flip chip technology and economics can be found in **OSAT: Why Flip Chip Is Important & How It Impacts the OSAT Industry (Part I)** and **(Part II)**.

Exhibit 270 Flip Chip Commands Better Margin and Hence Higher Profit

	Wirebond	Bumping & Assembly	Substrate	Flip Chip Total
Capex	$100	$100	$0	$100
Annual Revenue	$120	$62	$38	$100
COGS	$98	$38	$38	$76
Gross Profit	$22	$24	$0	$24
Gross Margin	19%	39%	0%	24%
Gross Profit/Capex	**22%**	**24%**	**N.A.**	**24%**

Source: Bernstein research.

Exhibit 271 SPIL Has Higher Exposure to Flip Chip



Source: Corporate data and Bernstein analysis.

In the Long Run, 2.5D/3D IC Shifts Value from OSAT and Substrate Sector to Foundry, But High Cost Will Keep It from Mass Adoption in the Near Future

2.5D[12]/3D IC is arguably the most promising technology in the "mid-end." Relying on silicon as package material, 2.5D/3D IC can deliver much higher performance that flip chip, wirebond and other current packaging technologies can't possibly achieve. All major semiconductor companies, including Intel, Samsung and TSMC are investing significantly in this technology.

Its process consists of TSV (through silicon via), microbump (similar to flip chip bump but with smaller dimension), bonding, etc., which enable much denser and faster interconnections between dies. 2.5D/3D IC technology will deliver very significant advantages. According to Samsung, compared to PoP (a SiP technology that is currently used in the processor of iPhone/iPad), the 2.5D/3D IC technology can deliver 8x bandwidth, 50% lower power consumption and 35% smaller package size (see Exhibit 272).

As many wafer manufacturers invest heavily to develop this technology, we've seen growing friction between foundries and the OSAT companies. Many investors also begin to be concerned about the long-term prospects of the OSAT industry.

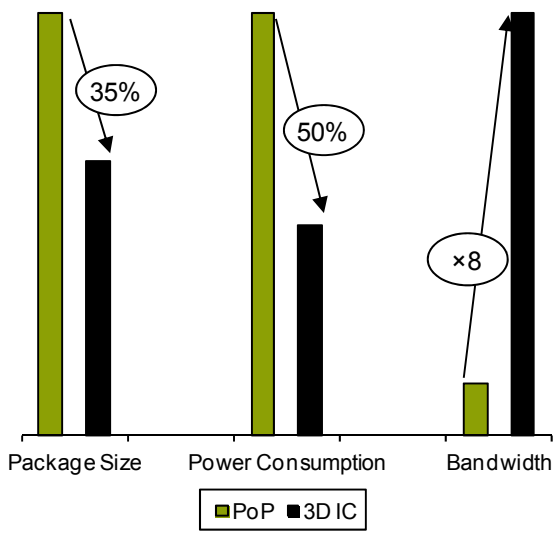
We recognize that 2.5D/3D IC will shift value from OSAT and substrate companies to foundries as it fundamentally is a silicon-based technology. Our analysis, however, finds that its cost would remain much higher than the typical cost range of a mobile chip even in a few years (see Exhibit 273). We believe that its applications would be very limited and the aforementioned value shift will be immaterial in the next three years. We thus think it's too early to de-rate OSAT or substrate companies for this reason.

Among Intel, TSMC and Samsung, we think the vertical integration at Intel and Samsung will help them bring 2.5D/3D technology earlier to the market. Samsung in particular is very well positioned as it has design, front-end to back-end manufacturing and memory all in-house. Intel is also well positioned as an IDM with design, front-end and back-end manufacturing all in-house (Intel also has a close relationship with its U.S. memory partner Micron). TSMC, on the other hand, will need to work with partners for memory and flip-chip substrate. Without all the capabilities in-house, it is challenging for TSMC to move as fast as Samsung and Intel in the 2.5D/3D technology, as it will have to deal with the different paces of customers & partners (see Exhibit 274).

Detailed analysis of 2.5D/3D can be found in **Foundry and OSAT: 2.5D/3D IC - Leapfrog Ahead of Moore's Law? (Part I)** and **Foundry, OSAT and Samsung: 2.5D/3D IC - Leapfrog Ahead of Moore's Law? (Part II) Economics and Competition**.

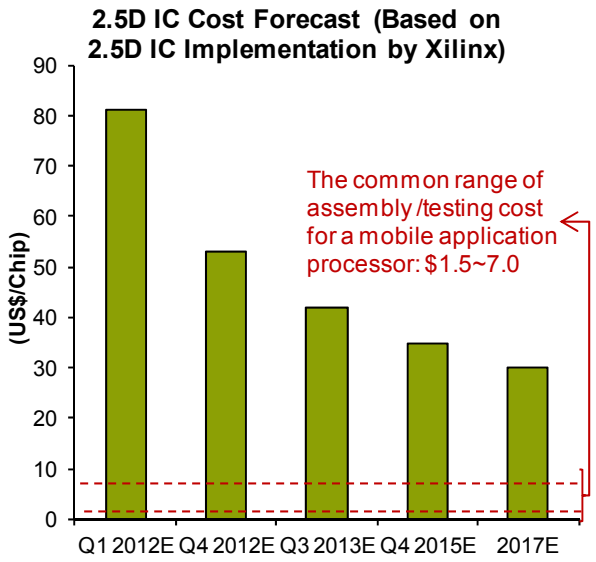
[12] Often referred to by TSMC as CoWoS (Chip on Wafer on Substrate).

Exhibit 272 3D IC Promises to Deliver 8x of Bandwidth with Lower Power Consumption and Smaller Footprint



Source: Samsung and Bernstein analysis.

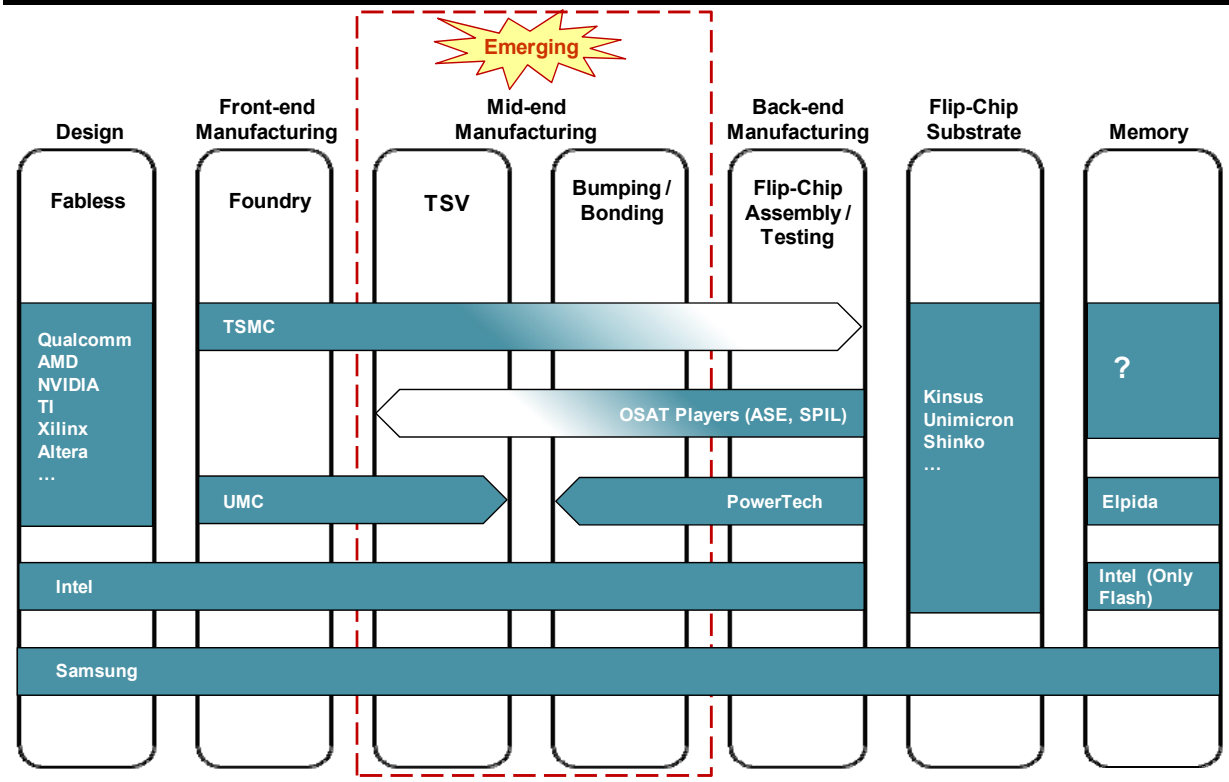
Exhibit 273 The 3D/2.5D Cost Is Expected to Remain Much Higher Than the Package Cost That a Mobile Chip Can Afford



Note: Numbers represent the costs to Xilinx or other IC vendors, or the prices from 2.5D IC manufacturers. Using Xilinx's Virtex-7 FPGA in this example.

Source: Yole and Bernstein analysis.

Exhibit 274 With Vertically Integrated Model, Samsung and Intel Are in a Better Position to Deliver 2.5D/3D IC



Source: Bernstein research.

The Back-End Industry Will Still Be Impacted by the Slowing Moore's Law, Although the Ramifications Can Be Very Different Depending on Investment Horizon

In conclusion, the absence of Moore's Law is no guarantee that the back-end industry can survive the slowing of Moore's Law unscathed. The ramifications, however, can be very different depending on investment horizon.

Near term, we're comfortable with the growth outlook of ASE and SPIL in light of their exposure to mobile applications and flip chip. We expect the subtle balance between foundries and OSATs in bumping will remain.

Medium term, 2.5D/3D IC will remain too expensive to become a meaningful headwind on OSATs. We project it will not be a significant growth area for foundries either.

Long term, the emergence of "mid-end" likely will tilt the competitive landscape to favor foundries. However, we remain doubtful this will be able to fully offset the mounting burden in the core business as the slow death of Moore's Law takes its toll.

Appendix: Risks

U.S. Semiconductors

Intel Corp. Beyond the macro, upside risk to our price target on INTC includes greater-than-expected PC growth, lack of microprocessor ASP pressure, substantial success in smartphones and/or tablets (without corresponding cannibalization), or further share gains.

Qualcomm Inc: Downside risks to our outperform rating and price target on QCOM include widespread "revolt" by customers resulting in lower royalty rates, 3G penetration and ramp slower than we model, resulting in less device or chipset unit growth, or device and/or chipset ASPs declining faster than we model.

Broadcom Corp: Downside risk to our price target on BRCM include increased competition in core markets driving share loss and/or multiple compression, potential changes to corporate tax laws influencing BRCM's tax-advantaged status, further pressure on gross margins, lack of opex control, the investment community re-evaluating BRCM on a GAAP rather than a pro-forma basis, or management failing to follow through on stated objectives to reduce share-based compensation and other goals.

Asian Semiconductors

Taiwan Semiconductor Manufacturing Co Ltd: There are a number of risks to our TSMC target price: 1) unexpected innovations that significantly change the capex requirements of leading technologies; 2) competition, especially any accelerated capacity expansion or price competition, will lead to spare capacity and weak price; 3) macroeconomic risk would change end-market demand and eventually impact the upstream players such as TSMC; 4) exchange rate fluctuation poses substantial risk to TSMC's revenue and profit; and 5) disruption and imbalance in the electronics supply chain — either on TSMC, on its suppliers/distributors, or on its customers — will create a chain effect and impact the company's ability to fully utilize its capacity.

United Microelectronics Corp: The following are the risks to our UMC target price: 1) possible share dilution effect from offering very attractive prices to get strategic investors; 2) substantial improvement in utilization and profitability by securing major volume with strategic investors; 3) unexpected innovations that significantly change the capex requirements of leading technologies; 4) competition, especially any faster-than-expected capacity expansion or price competition, will lead to spare capacity and weak price; 5) macroeconomic risk would change end-market demand and eventually impact the upstream players such as UMC; 6) exchange rate fluctuation poses substantial risk to UMC's revenue and profit; 7) disruption and imbalance in the electronics supply chain — either on UMC, on its suppliers/distributors, or on its customers — will create a chain effect and impact the company's ability to fully utilize its capacity.

Semiconductor Manufacturing International Corp: Demand Risk — Macroeconomic environment will seriously affect the semiconductor industry as the industry is more volatile and cyclical in general. This risk mostly manifests itself in a change in end market demand first and then gradually ripples throughout the electronics supply chain and eventually impacts the upstream players such as SMIC. This can be an upside risk to our forecasts. **Regulation / Government Risk** — China is still developing its infrastructure and regulations to support its domestic market. Currently SMIC enjoys government R&D subsidies and tax benefits. The funding from CIC and Datang also demonstrates the endorsement on SMIC from Chinese government. If the Chinese government provides more favorable support to SMIC, it would be an upside risk to our forecasts. **Competition Risk** — Competition, especially any accelerated capacity expansion, will lead to spare

capacity in the semiconductor industry. As competitors may cut price in order to grab demand to fill idle capacity, SMIC might suffer lower price and margin as a result. On the other hand, if the capacity expansion from competitors takes place more slowly than expected, SMIC may be able to grow faster and generate better profits. **Supply Risk** — Disruption and imbalance in the electronics supply chain, either on SMIC, on its suppliers/distributors, or on its customers, will create a chain effect and impact the company's ability to fully utilize its capacity and deliver its financial performance as planned. **Technology Risk** — SMIC's technology migration may fall behind the requirement of its customers. This would result in market share loss, price erosion and profitability deterioration worse than our expectations.

Advanced Semiconductor Engineering Inc: There are a number of risks to our ASE target price: 1) macroeconomic risk would change end-market demand and eventually impact the upstream players such as ASE; 2) competition, especially any accelerated capacity expansion, will lead to spare capacity in the semiconductor industry; 3) exchange rate fluctuation poses substantial risk to ASE's revenue and profit; and 4) disruption and imbalance in the electronics supply chain — either on ASE, on its suppliers/distributors, or on its customers — will create a chain effect and impact the company's ability to fully utilize its capacity.

Siliconware Precision Industries Co: The risks to our SPIL target price include: 1) macroeconomic risk that would change end-market demand and eventually impact the upstream players such as SPIL; 2) competition, especially any accelerated capacity expansion, will lead to spare capacity in the semiconductor industry; 3) exchange rate fluctuation poses substantial risk to SPIL's revenue and profit; and 4) disruption and imbalance in the electronics supply chain — either on SPIL, on its suppliers/distributors, or on its customers — will create a chain effect and impact the company's ability to fully utilize its capacity.

European Semiconductors

ASML Holding NV: ASML has been historically sensitive to the Semi cycle, and this is still a risk. In the current context, we are not worried about a weakness in Lithography spending in the next two to three years. In Memory, with industry capacity becoming concentrated, we expect the cycles to be less extreme than in the past. But, a possible slowdown in Semi represents a news flow and sentiment risk for the next six months. We work on the assumption that ASML is going to be able to progressively introduce E.U.V into the market, based on the very material progresses the company has achieved in the technology. We see limited risks associated with further delays in the ramp-up of the technology, but recognize a risk for the entire industry on a three- to five-year horizon if E.U.V. were eventually recognized not fit for purpose. Alternatives to E.U.V. would nevertheless become a limited threat to ASML, as the company remains open, as a system integrator, to adopt these technologies in its Tools.

ARM Holdings PLC: The biggest upside risk to our target price on ARM is greater-than-expected success in the PCs & Servers segment. As ARM remains a concept stock, we also see upside risks around announcements of design wins or product launches that drive positive sentiment or increased expectation of success in the future. Following a success in PCs & Servers, ARM may gain much greater penetration within Windows tablets than we expect. Other risks include continued design activity driving strong licensing revenues, a stable high semi channel inventory level, or incremental royalty revenues coming in at a significantly higher royalty rate than we expect.

Global Memory & Consumer Electronics

Samsung Electronics: The biggest risks to the downside on our price target for Samsung Electronics are: 1) heightened competition and reduced margins in the handset business; 2) loss of technology leadership in memories to competitors; 3) a contracting of margins in the NAND industry contrary to our thesis; 4) a sell-off in

Korean and/or Asian equities, as SEC is the largest component of the KOSPI; 5) reductions in handset subsidies, which would adversely impact high-end smartphone profits; 6) a delayed DRAM recovery due to worsening cannibalization of PCs by tablets; 7) an abrupt strengthening of the Korean won, which would reduce revenue and increase costs; or 8) litigation/component risks from Apple.

SanDisk Corp: The biggest risk to the downside for SanDisk is reduced margins for NAND, which would lead to lower earnings and a lower valuation for the business. Additionally, there is risk that future royalty streams may be reduced through renegotiation with royalty payers or reduced revenues throughout the industry. SanDisk also faces headwinds from further strengthening in the JPY.

SK Hynix Inc: The biggest risk to the downside for SK Hynix is a weaker-than-expected DRAM recovery, resulting from a delay in industry consolidation or independent restructuring of Elpida. The biggest risk to the upside is a better-than-expected shrink achieved by the company as well as stronger-than-expected NAND business growth.

Micron Technology Inc.: The biggest risk to the downside for Micron is a weaker-than-expected DRAM recovery, or a consolidation/restructuring scenario for the industry that is unfavorable to Micron. Micron may also invest substantial further equity in Inotera, which may require additional cash in the next 12 months. Furthermore, following Micron's announcement in July 2012, it is the most likely suitor in an acquisition of Elpida, Rexchip or their assets; there are significant consequences to current shareholders in the price and the deal structure at which Micron may end up acquiring some or all of these assets.

Inotera Memories Inc: The biggest risk to the downside for our outperform rating on Inotera is a correction in the DRAM pricing environment, which would lower both the profitability and the valuation of the company.

Nanya Technology Corp: The biggest risk to the upside for our underperform rating on Nanya is an upturn in the DRAM pricing environment, which would raise both the profitability and the valuation of the company. Additionally, Nanya's parent company and/or the Taiwanese government may inject significant equity at above-market prices.

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Disclosure Appendix

VALUATION METHODOLOGY

Our price target for ASML at €70 corresponds to 15x 2014 earnings. For ARM, we arrive at £5.50 target at 31x 2013 earnings. For INTC, we apply a ~10x multiple to our 2014 EPS estimate ($1.85), yielding a price target of $18. We value QCOM by setting target multiples of 17x P/FE and set our target price at $80. We value BRCM by applying a ~18x multiple (~1.4x relative on a ~13x market multiple) to our "adjusted GAAP" EPS resulting in a $41 target price. We value TSMC at 3.2x NTM BV excluding intangible assets and goodwill. We value UMC at 0.55x NTM BV and SMIC at 1x NTM BV. We use historical average price to one-year forward earnings of 14.8x to value SPIL. Our target multiple for ASE is based on P/FE of 12x. Our KRW 2.5 million target price for Samsung represents ~10x our 2014 diluted EPS. Our $75 TP for SNDK is based on a 2014 P/E of 12.7x. Our KRW 35,000 target price for SK Hynix Inc. is based on 2.1x 2Q:14 book value of KRW17K. For MU, our $14.0 TP is equivalent to 8.5x CY 2014 EPS and 1.7x one year forward tangible BVPS. Our NT$14.0 price for Inotera Memories Inc. is based on 7x 2014 EPS and 2.2x 2Q:14 BVPS. Our NT$1.2 price for Nanya Technology Corp is based on a P/B multiple of 1.3x applied to book value per share forecast for 2Q:14.

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Semiconductor, memory, and semi-cap equipment sectors are exposed to general macroeconomic risks, which ultimately influence end-market demand and can positively or negatively affect the entire electronics supply chain. In addition, the industry has historically been subject to seasonal and cyclical demand fluctuations for its products or services as well as technological, competitive, execution, and currency risks among others. Beyond the broader macro environment, several company-specific risks may influence the stocks in our coverage. (Please see Appendix for company-specific risks.)

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005935.KS	O (IC) 08/10/11		
2303.TT	U (RC) 08/09/12	M (IC) 08/02/11	
2311.TT	M (RC) 05/09/13	O (RC) 11/16/12	M (IC) 08/02/11
2325.TT	O (RC) 08/10/12	M (IC) 08/02/11	
2330.TT	M (RC) 01/30/12		
2408.TT	U (IC) 08/10/11		
3474.TT	O (RC) 03/13/13	U (IC) 08/10/11	
981.HK	U (RC) 05/30/13	M (RC) 11/09/12	U (IC) 08/02/11
ARM.LN	U (RC) 01/16/13	M (RC) 05/10/12	
ASML	O (IC) 06/21/12	M (DC) 04/04/08	
ASML.NA	O (IC) 06/21/12	M (DC) 04/04/08	
ASX	M (RC) 05/09/13	O (RC) 11/16/12	M (IC) 08/02/11
BRCM	O (RC) 08/10/12	M (IC) 06/04/09	
INTC	U (RC) 10/09/12	M (IC) 06/04/09	
MU	O (RC) 03/14/12		
QCOM	O (IC) 06/04/09		
SMI	U (RC) 05/30/13	M (RC) 11/09/12	U (IC) 08/02/11
SMSN.LI	O (IC) 08/10/11		
SNDK	O (IC) 08/10/11		
SPIL	O (RC) 08/10/12	M (IC) 08/02/11	
TSM	M (RC) 01/30/12		
UMC	U (RC) 08/09/12	M (IC) 08/02/11	

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