Institutionen för systemteknik
Department of Electrical Engineering

Examensarbete

An FPGA implementation of a digital FM modulator

Examensarbete utfört i elektroniksystem
vid Tekniska högskolan vid Linköpings universitet
av

Henrik Boström

LiTH-ISY-EX--11/4481--SE

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Sammanfattning
Abstract

The increase in speed and density of programmable logic devices such as Field Programmable Gate Arrays (FPGA) enables ever more complex designs to be constructed within a short time frame. The flexibility of a programmable device eases the integration of a design with a wide variety of components on a single chip.

Since Frequency Modulation (FM) is an analog modulation scheme, performing it in the digital domain introduces new challenges. The details of these challenges and how to deal with them are also explained. This thesis presents the design of a digital stereo FM modulator including necessary signal processing, such as filtering, waveform generation, stereo multiplexing etc. The solution is comprised of code written in Very high speed integrated circuit Hardware Description Language (VHDL) and a selection of free Intellectual Property (IP)-blocks and is intended for implementation on a Xilinx FPGA.

The focus of the thesis lies on area efficiency and a number of suggestions are given to maximize the number of channels that can be modulated using a single FPGA chip. An estimation of how many channels that can be modulated using the provided FPGA, Xilinx XC6SXL100T, is also presented.

Nyckelord
Keywords FPGA,FM, SDR, frequency modulation, software defined radio

Abstract

The increase in speed and density of programmable logic devices such as FPGA enables ever more complex designs to be constructed within a short time frame. The flexibility of a programmable device eases the integration of a design with a wide variety of components on a single chip.

Since FM is an analog modulation scheme, performing it in the digital domain introduces new challenges. The details of these challenges and how to deal with them are also explained. This thesis presents the design of a digital stereo FM modulator including necessary signal processing, such as filtering, waveform generation, stereo multiplexing etc. The solution is comprised of code written in VHDL and a selection of free IP-blocks and is intended for implementation on a Xilinx FPGA.

The focus of the thesis lies on area efficiency and a number of suggestions are given to maximize the number of channels that can be modulated using a single FPGA chip. An estimation of how many channels that can be modulated using the provided FPGA, Xilinx XC6SXL100T, is also presented.

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Acronyms

AM Amplitude Modulation

ASRC Arbitrary Sample Rate Converter

BPSK Binary Phase-Shift Keying

BRAM Block Random Access Memory

CLB Configurable Logic Block

CPU Central Processing Unit

CRC Cyclic Redundancy Check

DAC Digital to Analog Converter

DDS Direct Digital Synthesizer

DSBSC Dual SideBand Suppressed Carrier

DSP Digital Signal Processor

EM Electro Magnetic

FFT Fast Fourier Transform

FIR Finite length Impulse Response

FM Frequency Modulation

FPGA Field Programmable Gate Array

IDE Integrated Development Environment

IIR Infinite length Impulse Response

IP Intellectual Property (ambiguity, can also mean Internet Protocol)

ITU-R International Telecommunication Union - Radiocommunication Sector

kB kiloByte

kSPS kiloSamples Per Second

LFSR Linear Feedback Shift Register

LUT LookUp Table

MPEG Moving Picture Experts Group

MSB Most Significant Bit

MSPS MegaSamples Per Second

PM Phase Modulation

QPSK Quadrature Phase-Shift Keying

RAM Random Access Memory

RC Resistive Capacitive

RCA Radio Corporation of America

RDS Radio Data System

RDY Ready

RF Radio Frequency

RFD Ready For Data

RMS Root Mean Square

SDR Software Defined Radio

SNR Signal-to-Noise Ratio

VHDL Very high speed integrated circuit Hardware Description Language

VHF Very High Frequency

Symbols

A: Amplitude

B: Number of bits

c: Speed of light [m/s]

f: Frequency [Hz]

m: Modulation index

λ: Wavelength [m]

ω: Angular frequency [rad/s]

Θ: Phase increment

Chapter 1

Introduction

This chapter presents the purpose, goal, delimitations and method of design used in this master thesis. It also discusses some background material and the tools needed for implementation.

1.1 Purpose

The purpose of this master thesis is to define, analyze, and implement a generic Field Programmable Gate Array (FPGA)-based multichannel Frequency Modulation (FM) modulator to be used in a cable TV broadcast environment. A typical application for this FM modulator is Internet Protocol (IP)-to-FM modulation for large cable TV networks (edge-FM) where often both TV and radio content are distributed over IP and modulated on the "edges" of the network as shown in Fig. 1.1. The typical input signal consists of audio samples from a Moving Picture Experts Group (MPEG) decoder, and the output signal is multichannel FM to a Digital to Analog Converter (DAC).

1.2 Goal

The goal of this thesis is to analyze the signal requirements and optimize the system with respect to area usage to be able to make an implementation that modulates as many channels as possible using the available FPGA resources.

1.3 Method

The first step in the thesis is to perform a pilot study to find out which components are needed in order to construct a fully functional FM transmitter capable of operating in a professional environment. The pilot study also includes an analysis of the FM standard to ensure that the design fulfills certain performance metrics since the Very High Frequency (VHF) band, in which FM radio is transmitted, is governed by law. The second step is implementing all the sub-systems using

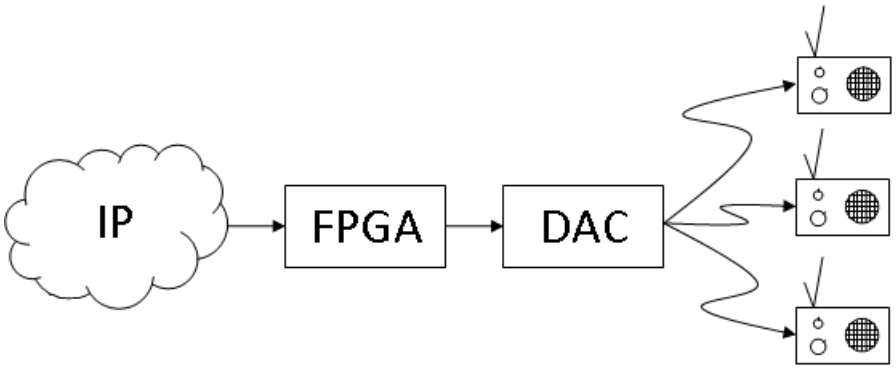

Figure 1.1. Typical application.

VHDL and also to simulate them using the ModelSim simulation software. The simulations can then be analyzed using MATLAB. This process is iterated until the simulations are consistent with the expected outcome, at which point, all the sub-systems are put together to form a complete FM transmitter.

Some of the sub-systems might be implementable with the help of Intellectual Property (IP)-blocks. When such a solution exists for a given problem, it will be evaluated with respect to the area consumption and the design time compared to the case of building such a component without the use of a pre-fabricated block. The complete system is simulated and again analyzed using MATLAB. A standard off-the-shelf FM receiver, available at any consumer electronics store, is used to validate the simulation results.

1.4 Delimitations

The FPGA chip is a Xilinx XC6SLX100T and is predetermined by the client although the overall structure of the system is generic and should work with any kind of Xilinx FPGA with a sufficient amount of area and clock frequency.

To avoid the implementation of an Arbitrary Sample Rate Converter (ASRC) which would most likely be quite time consuming, the input sample rate is limited to 48 kHz.

Two different systems are available for achieving stereo transmission, the pilot-tone system and the polar-modulation system [5]. The pilot-tone system is the most common [5] and it is therefore chosen for implementation in this thesis. Other parameters such as pre-emphasis characteristics and maximum carrier deviation are chosen to comply with Swedish regulations.

1.5 Background

The need for modulation arises from the fact that an antenna needs to have roughly the same dimension as the wavelength of the transmitted Electro Magnetic (EM) wave [13]. The wavelength depends on the speed of light and the frequency of the wave as

$$\lambda = \frac{c}{f}. \tag{1.1}$$

Given a baseband signal consisting of a 10kHz sinusoid and $c \approx 3 \cdot 10^8\ m/s$, the resulting wavelength and, hence, antenna dimension is approximately 30 km which is obviously not feasible. Therefore, a carrier is used to convey the information at a more suitable frequency. Another reason for modulation is that the same carrier can be utilized to transmit additional information, for instance traffic reports using RDS.

1.6 Tools

This section gives a brief explanation of the tools needed for implementation, simulation, and validation.

1.6.1 FPGA

An Field Programmable Gate Array (FPGA) is an integrated circuit consisting of interconnected blocks called Configurable Logic Blocks (CLB). Each CLB is composed of slices and each slice is composed of digital building blocks such as LookUp Tables (LUT), flip-flops etc. A LUT can be programmed to realize combinational logic and when combined with flip-flops and other hardware resources, almost any kind of digital system can be synthesized, ranging from the simplest circuit to a Central Processing Unit (CPU) or a full scale computer capable of running an operating system.

FPGAs are designed to be reconfigurable using a hardware description language such as VHDL or Verilog. They are similar to programming languages in syntax, but to correctly capture the nature of hardware, statements are executed concurrently instead of sequentially. Due to their reconfigurability, FPGAs are sometimes referred to as programmable logic. Figure 1.2 shows a typical floor plan of an FPGA, in this case a Spartan II [10].

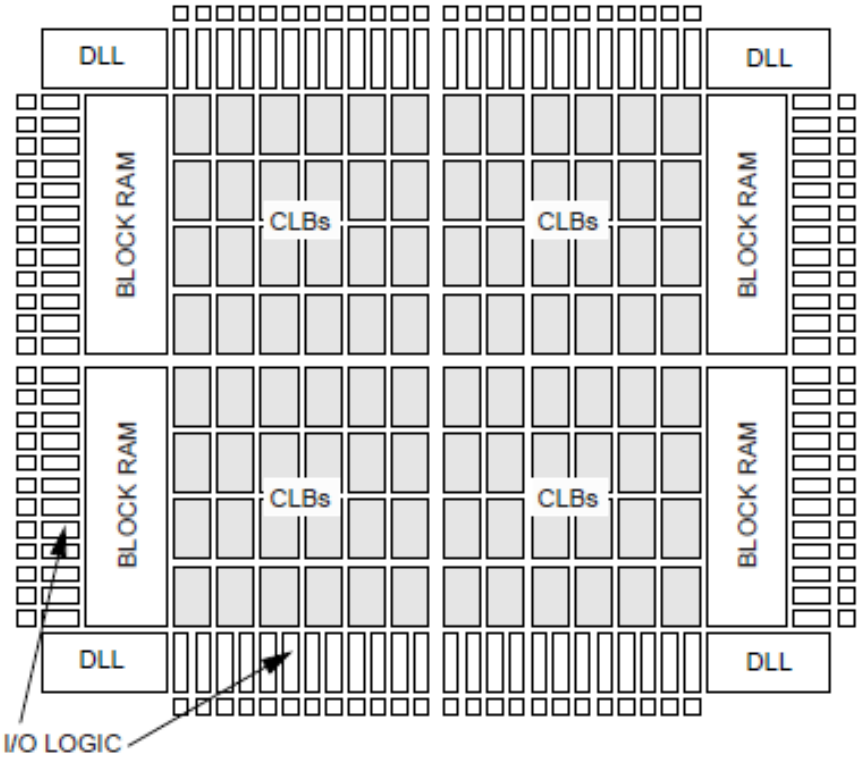

Figure 1.2. Spartan-II family FPGA floor plan.

1.6.2 Xilinx ISE webpack

Xilinx ISE webpack is a free Integrated Development Environment (IDE) distributed by Xilinx for use with their FPGAs. Apart from managing projects and synthesizing code, it also contains a selection of free IP-blocks [18].

1.6.3 ModelSim

ModelSim is a simulation and debugging software for digital circuits written in a hardware description language such as VHDL [6]. It is used for validating the code before it is synthesized to the FPGA.

1.6.4 ChipScope

ChipScope is a logic analyzer that can be embedded in the FPGA design to enable debugging after synthesis [3].

1.6.5 MATLAB

MATLAB is a software tool for computations, data analysis, signal processing etc. It is used throughout the development process for filter design and analysis of data collected from ModelSim and ChipScope.

1.6.6 Other tools

In addition to the above mentioned tools, a selection of other tools is also used. This includes an oscilloscope, a spectrum analyzer, an FPGA development board, and an off-the-shelf FM receiver.

1.7 Report disposition

Chapter 1: Introduction gives an introduction to the thesis including its purpose and goal, background, method, delimitations, and the tools needed for implementation. This chapter also explains what an FPGA is and how it is used.

Chapter 2: Prerequisite knowledge explains the FM system on the transmitter side along with some brief history and advantages over other modulation techniques. Some formulas, definition of terms, and important measures of performance are also included.

Chapter 3: The FM standard presents the FM standard and the demands which a transmitter needs to fulfill in order to comply with VHF regulations. This is meant to serve as an introduction to the demands and recommendations for FM transmitters. No information is given as to how these recommendations are met by the implementation presented in this thesis.

Chapter 4: Implementation presents the system architecture and implementation details of all sub-systems. Included are also estimations on important parameters for each sub-system and how well the implementation complies with the recommendations presented in Chapter 3.

Chapter 5: Results and performance gives an account of overall system performance in terms of signal quality and resource utilization. It includes area reports for all sub-systems and suggestions for optimization as well as an estimate of the maximum number of channels that can be modulated given the resources available for the FPGA used in this thesis.

Chapter 6: Summary summarizes the work and provides suggestions for future improvement and optimization.

Chapter 2

Prerequisite knowledge

This chapter presents the history and background of FM, the theory behind it, and its advantages and disadvantages.

2.1 FM – a brief history

The history of radio broadcasting started in the beginning of the 20th century [13] with the introduction of the Amplitude Modulation (AM) system in which the amplitude of the carrier is modulated by the amplitude of the message signal as demonstrated in Fig.2.1 [2]. Albeit relatively simple in both theory and practice, AM suffers more from additive noise than FM does [13].

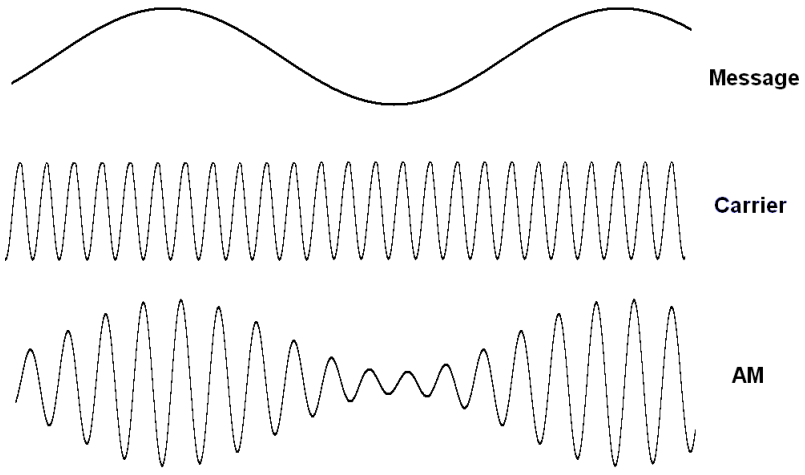

Figure 2.1. Amplitude modulated carrier.

The method of FM was patented by Edwin Howard Armstrong in 1933 and became popular due to its superior fidelity and noise immunity compared to AM. Unfortunately for Armstrong, the Radio Corporation of America (RCA), using the AM system, successfully lobbied for a change in law regulations, moving the FM band from 42 – 50 MHz to 88 – 108 MHz effectively rendering 500000 receivers useless [13]. The FM system eventually recovered and it is widely used today.

2.2 Analysis of FM

Unlike AM, where the amplitude of the carrier is modulated, the FM system conveys information by altering the instantaneous frequency of a carrier according to the amplitude of the message signal. Given a modulating signal $v_m(t)$ and a sinusoidal carrier $v_c(t) = A_c \sin(\omega_c t)$, the resulting frequency modulated carrier is described as [13]

$$v_{FM}(t) = A_c \sin\left(\omega_c + 2\pi \int_0^t \delta(\tau) d\tau\right). \tag{2.1}$$

The frequency deviation, $\delta(t)$, alters the frequency of the carrier [13] as

$$f(t) = f_c + k v_m(t) = f_c + \delta(t). \tag{2.2}$$

Assuming a sinusoidal message $v_m(t) = \cos(\omega_m t)$ and the carrier previously mentioned, (2.1) can be rewritten as [13]

$$v_{FM}(t) = A_c \sin\left(\omega_c + 2\pi \int_0^t \delta(\tau) d\tau\right) = A_c \sin(\omega_c t + m \sin \omega_m t). \tag{2.3}$$

A graphical representation of (2.3) is shown in Fig. 2.2 [2].

The modulation index, m, is defined by the maximum frequency deviation δ_{max} and the largest frequency component in the modulating signal, f_m, as [13]

$$m = \frac{\delta_{max}}{f_m} \tag{2.4}$$

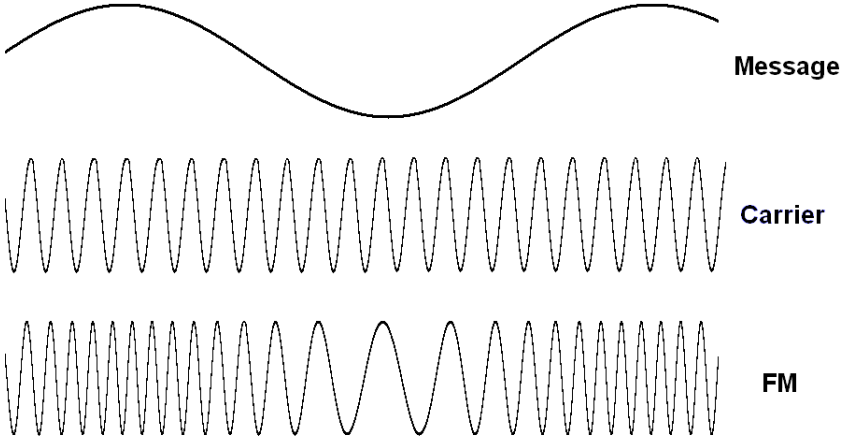

Figure 2.2. Frequency modulated carrier.

2.2.1 Bandwidth

Apart from the carrier and message signal, the spectrum of the modulated signal will contain numerous other components called sidebands. Using Bessel functions of the first kind, (2.3) can be expressed as a series of sinusoids as

$$\begin{aligned} v_{FM}(t) =& A_c \sin(\omega_c t + m \sin \omega_m t) = A_c\{J_0(m) \sin \omega_c t - \\ & - J_1(m)[\sin(\omega_c - \omega_m)t - \sin(\omega_c + \omega_m)t] + \\ & + J_2(m)[\sin(\omega_c - 2\omega_m)t + \sin(\omega_c + 2\omega_m)t] - \\ & - J_3(m)[\sin(\omega_c - 3\omega_m) - \sin(\omega_c + 3\omega_m)t] + \ldots\}, \end{aligned} \tag{2.5}$$

where the coefficients $J_i(m)$ represent the normalized voltages of the frequency components included in the modulated signal [12].

Assuming a fixed maximum baseband frequency, (2.4) states that an increased modulation index results in an increased frequency deviation of the carrier. This creates a stronger signal and allows easier and clearer reception. However, this has a drawback as it also increases the bandwidth as shown in (2.5) and Fig. 2.3 [8]. Using Carson's rule, the bandwidth can be approximated as [13]

$$\text{BW} \approx 2(\delta + f_m) = 2f_m(m+1),\ m \ll 1 \text{ or } m \gg 1, \tag{2.6}$$

$$\text{BW} \approx 2(\delta + 2f_m) = 2f_m(m+2),\ 2 < m < 10. \tag{2.7}$$

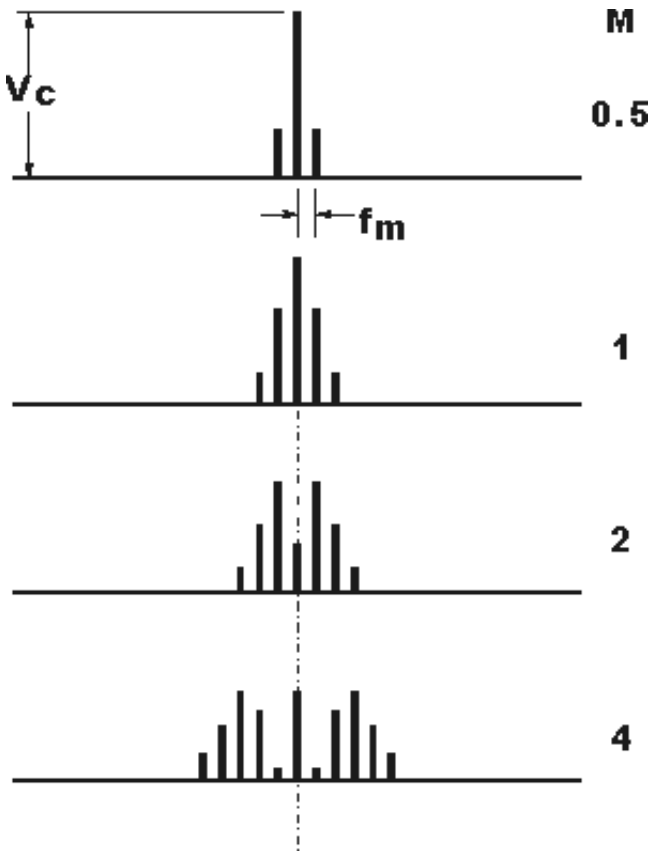

Figure 2.3. FM bandwidth.

2.2.2 Stereo FM

Stereo FM was introduced in 1961 and the system was designed so as to maintain compatibility with mono receivers [12]. This is accomplished using frequency division multiplexing, altering the baseband spectrum as shown in Fig. 2.4 [9]. A mono signal is formed by adding left and right channels (L+R) and a difference signal by subtracting the right channel from the left (L-R). The signal L-R is modulated around a 38 kHz sub-carrier using Dual SideBand Suppressed Carrier (DSBSC) AM and then added to the signal L+R and a 19 kHz pilot tone. The pilot tone is in-phase with the sub-carrier and accountable for 10% of the total deviation of the main FM carrier frequency. The pilot tone is used for demodulation of the signal L-R and also to notify the receiver that there is stereo information available. A mono receiver is designed to work with frequencies up to about 15 kHz and hence will only detect the mono part of the transmission [12].

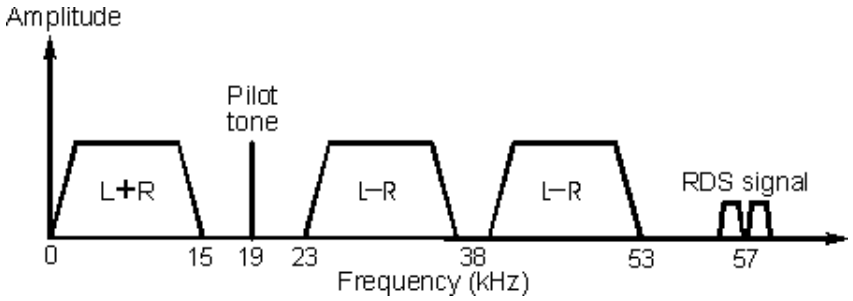

Figure 2.4. Baseband spectrum of stereo FM.

2.2.3 Radio Data System (RDS)

As Fig. 2.4 shows, there is some additional spectral content centered around 57 kHz (third harmonic of 19 kHz). Apart from broadcasting audio, the FM system can also be used to transmit data by adding AM modulated Binary Phase-Shift Keying (BPSK) codes to the multiplex signal [5]. Figure 2.5 shows the bi-phase coded symbols and Fig. 2.6 shows the AM modulated 57 kHz RDS sub-carrier [7].

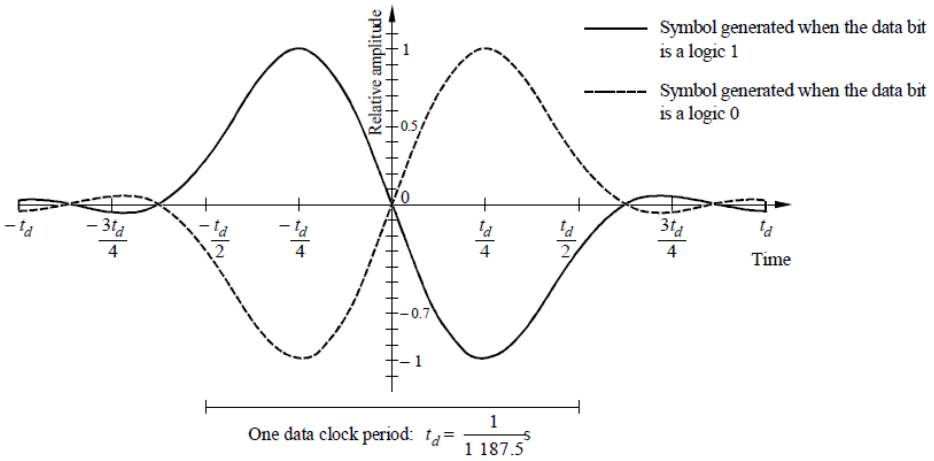

Figure 2.5. Bi-phase coded RDS symbols.

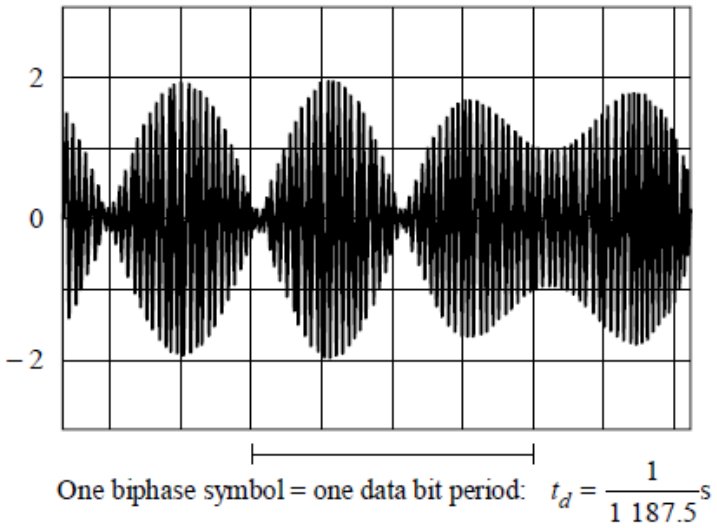

Figure 2.6. AM modulated RDS sub-carrier.

BPSK

BPSK is a one-dimensional digital modulation scheme where the symbols are represented by the signals

$$s_0(t) = \sqrt{E_{max}} \cdot \phi_0(t) \text{ and } s_1(t) = -\sqrt{E_{max}} \cdot \phi_0(t)$$

where $\phi_0(t)$ is the normal basis function

$$\phi_0(t) = \sqrt{\frac{2}{T}} \cdot \cos(2\pi f_c t) \cdot I_{0 \leq t < T}(t)$$

and $I_{\{0 \leq t < T\}}(t)$ denotes the indicator function explained in def. 2.1 [15].

Definition 2.1 (Indicator function)
The function $I_A(t)$ is the indicator function of the set A with the following interpretation.

$$I_A(t) = \begin{cases} 1, \ t \in A, \\ 0 \ \textit{elsewhere} \end{cases}$$

Both signals have energy E_{max} and the phase difference is π radians. To ensure that the signal interval $0 \leq t < T$ contains a whole number of half-periods of the cosine and that the basis function is normal, f_c is chosen so that $2f_cT$ is a positive integer [15]. The geometrical interpretation is shown in the signal space diagram in Fig. 2.7.

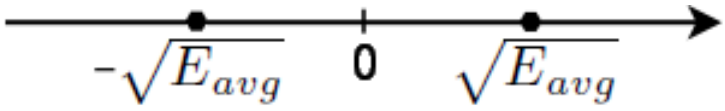

Figure 2.7. BPSK signal space diagram.

Cyclic Redundancy Check

Before modulation, the RDS data is encoded using Cyclic Redundancy Check (CRC) [7] which is a linear error correcting code where linearity is defined by def. 2.2 [15].

Definition 2.2 (Linearity)
Consider a binary code $\mathcal{C}$, and two codewords $\overline{c_1}, \overline{c_2} \in \mathcal{C}$. Then $\mathcal{C}$ is said to be linear if $\overline{c_1} + \overline{c_2} \in \mathcal{C}$ holds for all $\overline{c_1}, \overline{c_2} \in \mathcal{C}$.

To explain how a CRC codeword is generated, we need the following theorem which is the binary version of the well known division algorithm for integers.

Theorem 2.1 (Division algorithm for binary polynomials)
Given binary polynomials $a(x)$ and $b(x)$, with $b(x) \neq 0$, there exist uniquely determined binary polynomials $q(x)$ and $r(x)$, with $degree\{r(x)\} < degree\{b(x)\}$, such that

$$a(x) = q(x)b(x) + r(x).$$

Now, consider a message consisting of k bits. Let those bits be the coefficients of the binary polynomial $m(x)$ of degree at most $k-1$. For a CRC code, there exists a binary polynomial $p(x)$ of degree $n-k$. This fixed polynomial is used to generate parity bits from $m(x)$ by dividing $x^{n-k}m(x)$ by $p(x)$ [15]. Theorem 2.1 then states that there exist uniquely determined polynomials $q(x)$ and $r(x)$ with $degree\{r(x)\} < degree\{p(x)\}$, such that

$$x^{n-k}m(x) = q(x)p(x) + r(x). \tag{2.8}$$

The codeword $c(x)$ is then given as [15]

$$c(x) = x^{n-k}m(x) + r(x). \tag{2.9}$$

So, polynomial division is needed only to calculate the remainder $r(x)$ which can be easily accomplished using a Linear Feedback Shift Register (LFSR) such as the one in Fig. 2.8. After resetting the shift register, the coefficients of $m(x)$ are shifted in with Most Significant Bit (MSB) first. After n clock cycles, $r(x)$ is in the register and can shifted out as a sequence of bits [15].

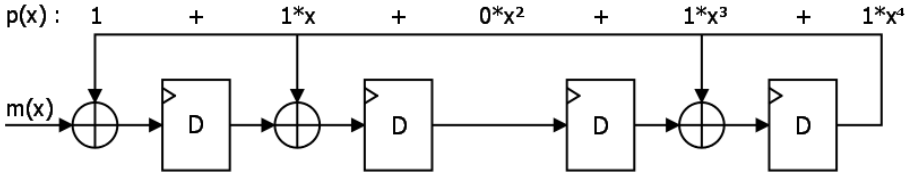

Figure 2.8. LFSR with $p(x) = x^4 + x^3 + x + 1$.

For error detection, consider a sent codeword,

$$c(x) = x^{n-k}m(x) + r(x).$$

Identifying with (2.8) and using addition modulo 2, since the polynomials are binary, we get

$$c(x) = q(x)p(x) + r(x) + r(x) = q(x)p(x).$$

Dividing $c(x)$ by $p(x)$ yields a remainder of zero which is exactly what is done by the CRC decoder. The received sequence of bits is interpreted as a polynomial, $y(x)$, consisting of the codeword $c(x)$ and an error polynomial $w(x)$ where [15]

$$y(x) = c(x) + w(x) = q(x)p(x) + w(x). \tag{2.10}$$

The decoder calculates the remainder of $y(x)/p(x)$ which is, according to (2.10), also the remainder of $w(x)/p(x)$. It can be shown that this remainder is zero if and only if $w(x)$ is a codeword, or in other words, if the remainder is non-zero then $w(x)$ is also non-zero. Thus, if $w(x)$ is a non-zero codeword, the error will pass undetected [15].

Chapter 3

The FM standard

This chapter deals with the recommendations for FM sound broadcasting in the VHF band provided by the International Telecommunication Union - Radiocommunication Sector (ITU-R) [5]. It is intended as a presentation of the standard, all results regarding how these recommendations are met are presented in Chapter 4 and summarized at the end of Chapter 5.

3.1 Monophonic transmissions

3.1.1 Radio Frequency (RF) signal

The RF signal consists of a carrier frequency modulated by a pre-emphasized sound signal with a maximum frequency deviation of ± 75 kHz or ± 50 kHz [5]. The maximum allowed deviation is dependent on which country the broadcasting station is located in.

3.1.2 Pre-emphasis

The pre-emphasis characteristic of the sound signal is identical to the admittance-frequency curve of a parallel resistance-capacitance circuit having a time constant of 50 μs or 75 μs [5]. As for frequency deviation, the time constant is also different for different countries.

3.2 Stereophonic transmissions using the pilot-tone system

3.2.1 RF signal

The RF signal consists of a carrier frequency modulated by a baseband signal known as the stereophonic multiplex signal. The maximum allowed frequency deviation is the same as for monophonic transmissions [5].

3.2.2 Stereophonic multiplex signal

This signal is produced as follows, compare with Fig. 4.11.

1. A signal M is formed equal to one half of the sum of the left-hand signal, A, and the right-hand signal, B, as

$$M = \frac{1}{2}(A + B), \tag{3.1}$$

where A and B correspond to the two stereophonic channels. This signal, M, is pre-emphasized in the same way as monophonic signals [5].

2. A signal S is produced equal to one half of the difference between signals A and B as

$$S = \frac{1}{2}(A - B) \tag{3.2}$$

and pre-emphasized in the same way as signal M. The pre-emphasized signal S is used for the suppressed-carrier amplitude modulation of a sub-carrier at 38 kHz ±4 Hz [5].

3. The stereophonic multiplex signal is the sum of:

   - The pre-emphasized signal M.
   - The sidebands of the sub-carrier, modulated by the pre-emphasized signal S, using suppressed-carrier amplitude modulation.
   - A pilot signal with a frequency of 19 kHz ± 2 Hz, exactly one-half the sub-carrier frequency.

   The stereo multiplex signal is described mathematically as

$$M + S + \sin(2\pi \cdot 19 \cdot 10^3 \cdot t). \tag{3.3}$$

4. The amplitudes of the various components of the stereophonic multiplex signal in relation to the maximum amplitude of that signal (which corresponds to the maximum frequency deviation) are [5]:

   - Signal M: maximum value is 90% (A and B being equal and in phase), meaning that

$$\frac{A_M}{A_M + A_S + A_{pilot}} = \frac{A_M}{A_M + A_{pilot}} \leq 0.9 \tag{3.4}$$

   since $A_S = 0$.

   - Signal S: maximum value of the sum of the amplitudes of the two sidebands is 90% (which corresponds to A and B being equal and of opposite phase), meaning that

$$\frac{A_S}{A_M + A_S + A_{pilot}} = \frac{A_S}{A_S + A_{pilot}} \leq 0.9 \tag{3.5}$$

   since $A_M = 0$.

- Pilot signal: 8 to 10%, meaning that

$$0.08 \leq \frac{A_{pilot}}{A_M + A_S + A_{pilot}} \leq 0.1 \tag{3.6}$$

- Sub-carrier at 38 kHz suppressed: maximum residual amplitude 1%, meaning that the sub-carrier must be suppressed with a factor of at least 100.

5. The relative phase of the pilot signal and the sub-carrier is such that, when the transmitter is modulated by a multiplex signal for which A is positive and $B = -A$, this signal crosses the time axis with a positive slope each time the pilot signal has an instantaneous value of zero. The phase tolerance of the pilot signal should not exceed ±3° from the above state. Moreover, a positive value of the multiplex signal corresponds to a positive frequency deviation of the main carrier [5]. The situation is depicted in Fig. 3.1.

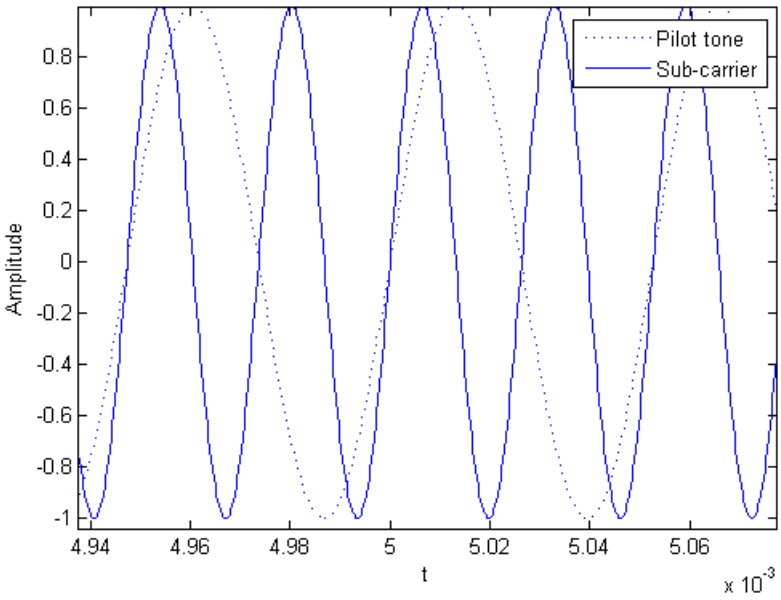

Figure 3.1. Relative phase of sub-carrier and pilot tone.

3.2.3 Supplementary signal transmission

If, in addition to the monophonic or stereophonic programme, a supplementary monophonic programme and/or supplementary information signals are transmitted and the maximum frequency deviation is ±75 kHz, the following additional conditions must be met [5].

- The insertion of the supplementary programme or signals in the baseband signal must permit compatibility with existing receivers, i.e., these additional signals must not affect the reception quality of the main monophonic or stereophonic programmes.

- The baseband signal consists of the monophonic signal or the stereophonic multiplex signal described above and having an amplitude of not less than 90% of that of the maximum permitted baseband signal value, and of the supplementary signals having a maximum amplitude of 10% of that value.

- For a supplementary monophonic programme, the sub-carrier and its frequency deviation must be such that the corresponding instantaneous frequency of the signal remains between 53 and 76 kHz.

- For supplementary information signals, the frequency of any additional sub-carrier must be between 15 and 23 kHz or between 53 and 76 kHz.

- Under no circumstances may the maximum deviation of the main carrier by the total baseband signal exceed ±75 kHz.

3.3 RDS

The ITU-R recommends that broadcasters, wishing to introduce the transmission of supplementary information for station and programme identification, should use the RDS [7].

3.3.1 Modulation of the data channel

- Sub-carrier frequency: 57 kHz ±6 Hz, locked in phase to the third harmonic of the 19 kHz pilot tone.

- Sub-carrier level: the recommended nominal deviation of the main FM carrier due to the modulated sub-carrier is ± 2 kHz.

- Method of modulation: the sub-carrier is amplitude modulated by the shaped and biphase-coded data signal. The sub-carrier is suppressed.

- Clock frequency and data rate: the basic clock frequency is obtained by dividing the transmitted sub-carrier frequency by 48, thereby providing a data rate of 1187.5 bits/s ± 0.125 bits/s.

- Differential coding: when the input data level from the coder at the transmitter is 0, the output remains unchanged from the previous output bit. When an input 1 occurs, the new output bit is the complement of the previous output bit.

3.3.2 Baseband coding

- Coding structure: the largest element in the structure is called a group and consists of 104 bits. Each group comprises 4 blocks of 26 bits. Each block comprises a 16-bit information word and a 10-bit CRC checkword.
- Order of bit transmission: all information words, checkwords and addresses have their most significant bit transmitted first.
- Error protection: The 10-bit CRC checkword, to which a 10-bit offset word is added, enables error detection and correction at the receiver side.
- Synchronization of blocks and groups: the data transmission is fully synchronous and there are no gaps between the groups or blocks. The beginning and end of the data blocks may be recognized in the decoder by using the fact that the error-checking decoder will, with a high level of confidence, detect block synchronization slips. The blocks within each group are identified by different offset words added to the respective 10-bit checkwords.
- Message format: the first five bits of the second block of every group are allocated to a five-bit code which specifies the application of the group and its version.

The coding structure is presented graphically in Fig. 3.2 [7].

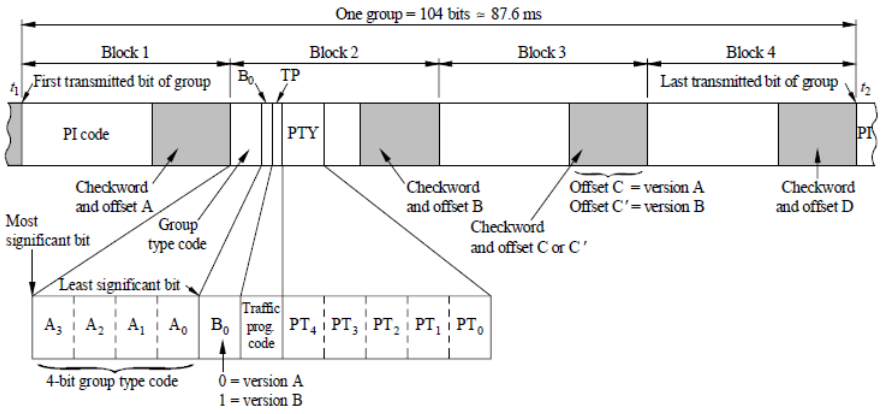

Figure 3.2. RDS code structure.

Chapter 4

Implementation

This chapter presents the structure of the complete system as well as implementation details for all sub-systems.

4.1 Overview

Figure 4.1 shows a block diagram of the implemented system. The buffers at input and output as well as in between the blocks provide handshaking and keep the dataflow consistent. When the signal Full is activated, the previous block needs to wait before producing new data. In the same way, the next block in the chain can not read data from the buffer if the signal Empty is activated. Not all signals are shown here.

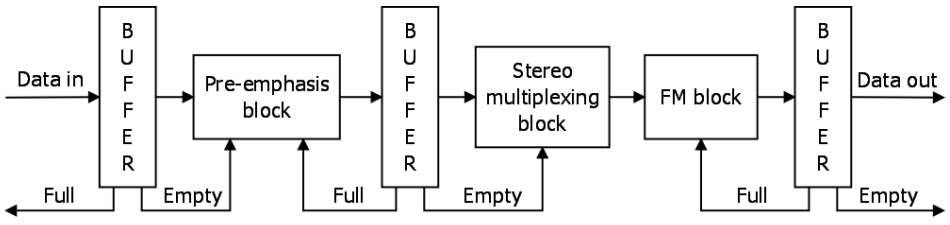

Figure 4.1. Implementation overview.

4.2 Pre-emphasis block

The pre-emphasis block contains an upsampling and bandlimiting Finite length Impulse Response (FIR) filter and a pre-emphasizing Infinite length Impulse Response (IIR) filter.

4.2.1 Upsampling and bandlimiting

Before pre-emphasis, the input is up-sampled to a sample rate of 96 kHz and bandlimited to 15 kHz. Making sure that the signal is bandlimited is very important since the stereo multiplexing unit adds additional spectral content between 19 kHz and 57 kHz for stereo and RDS signals. These signals might become noisy or completely destroyed if frequencies higher than 15 kHz are let through.

The filter was implemented using Xilinx FIR IP-block with coefficients extracted from MATLABs filter design toolbox resulting in a filter order of 42. Since the clock frequency is much higher than the sample frequency, the filter could be time-multiplexed enabling filtering of both the left and the right channel with the same filter. The frequency response is shown in Fig. 4.2.

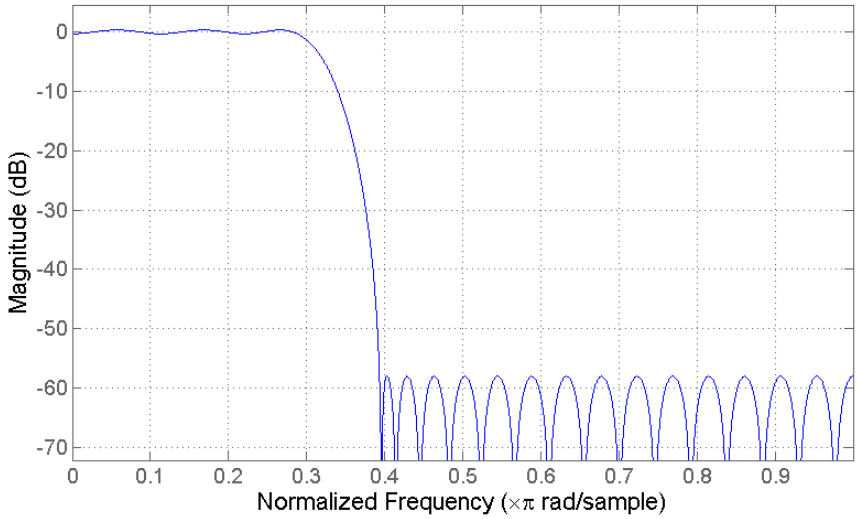

Figure 4.2. Upsampler and bandlimiter frequency response.

4.2.2 Pre-emphasizing

The digital IIR filter was obtained using bilinear transformation of a first order time continuous high-pass filter with an admittance-frequency curve identical to that of the passive parallel Resistive Capacitive (RC)-circuit with a time constant of 50 μs shown in Fig. 4.3. According to the well-known formula [17], the 3 dB cut-off frequency is

$$\frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 50 \cdot 10^{-}6} \approx 3183\ Hz \approx 20000\ rad/s. \tag{4.1}$$

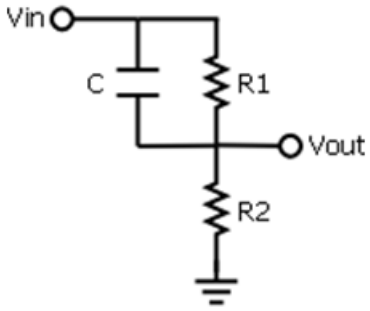

Figure 4.3. Time continuous pre-emphasis filter

Transformation to the z-domain yields the transfer function

$$H(z) = \frac{Az - B}{z - C}$$

which can be expressed as the difference equation

$$y[n] = Ax[n] - Bx[n-1] + Cy[n-1]$$

where $A \approx 0.7396, B \approx 0.6001$ and C ≈ 0.3397. The realization of the filter is shown in Fig. 4.4.

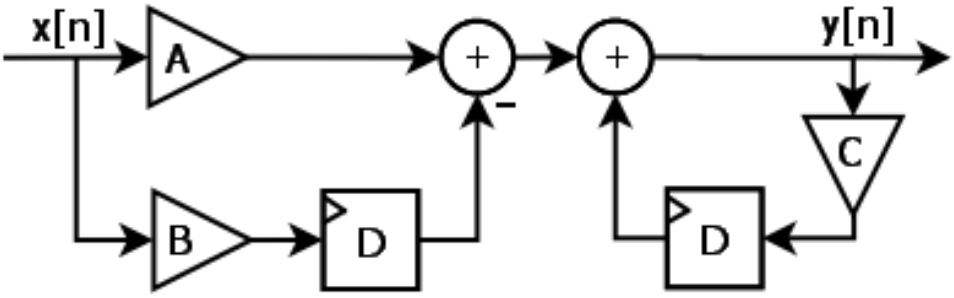

Figure 4.4. Time discrete pre-emphasis filter

Due to finite word length, the coefficients can not be exactly represented and have to be quantized. This causes the frequency response of the implemented filter to differ somewhat from the ideal response which is shown in Figs. 4.5 and 4.6.

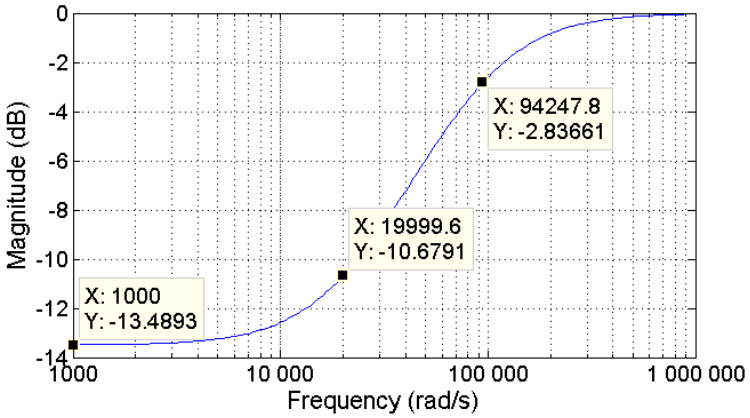

Figure 4.5. Ideal analog filter response.

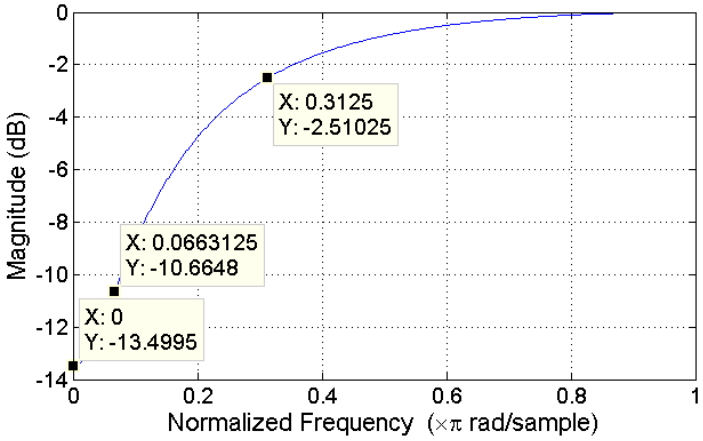

Figure 4.6. Digital filter with quantized coefficients.

Comparing the filters at the calculated cut-off frequency, 3183 Hz, and using the values presented in the above plots, the analog filter has a gain of

$$-10.6791 - (-13.4893) \approx 2.81dB$$

while its digital counterpart has a gain of

$$-10.6648 - (-13.4995) \approx 2.83dB$$

showing a very good agreement between the filters. Comparing the gain of both filters at the edge of the bandwidth, 15000 Hz, the numbers reported in the above

figures show that the analog filter has gained an additional

$$-2.83661 - (-10.6791) \approx 7.84dB$$

while the digital filter has gained

$$-2.51025 - (-10.6648) \approx 8.15dB$$

differing with approximately 0.31 dB from the ideal value. No tolerance is specified in [5] so the consequences of this variation is hard to determine.

4.3 Stereo multiplexing block

A block diagram of the complete stereo multiplexing block is shown in Fig. 4.7. When the first interpolation stage is finished, the Ready (RDY) signal is activated enabling a write to the buffer. From the other side, a read is enabled when the second interpolation stage is ready for data and activates Ready For Data (RFD).

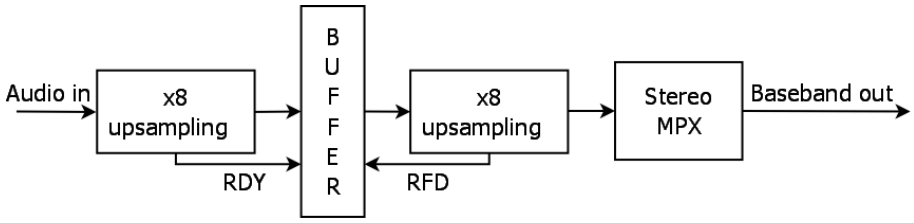

Figure 4.7. Stereo multiplexer including upsampling filters.

4.3.1 Sample rate considerations

The pilot tone and two sub-carriers are synthesized with a Direct Digital Synthesizer (DDS) running at the clock frequency, 125 MHz, with a throughput of one sample per clock cycle giving a sample rate of 125 MegaSamples Per Second (MSPS) while the audio input has a sample rate of 96 kiloSamples Per Second (kSPS). Although it is possible to combine signals of different sample rates, it creates some undesired effects. In the case of AM, these take the form of images of the modulated signal placed at integer values of the sample frequency away from the desired AM signal. Figure 4.8 shows a 5 kHz sinusoid sampled at 96 kHz and amplitude modulated around a 38 kHz carrier sampled at 1.25 MHz. The images of the desired modulated signal can be clearly seen at multiples of 96 kHz. This issue is well described in [14] regarding Phase Modulation (PM) and FM. The reason for showing the spectrum of an AM modulated signal instead of FM is that the effects of different sample rates are easier to see.
Due to the Nyquist theorem [16], stating that the sample frequency must be twice as high as the highest frequency component to avoid aliasing, the pilot tone and

the sub-carriers can not be synthesized with a sample rate of 96 kSPS since the frequency of the RDS sub-carrier is 57 kHz. Thus, the input must be upsampled to at least 114 kSPS and the DDS must be controlled with an enable signal to lower its sample rate to make it coherent with the input.

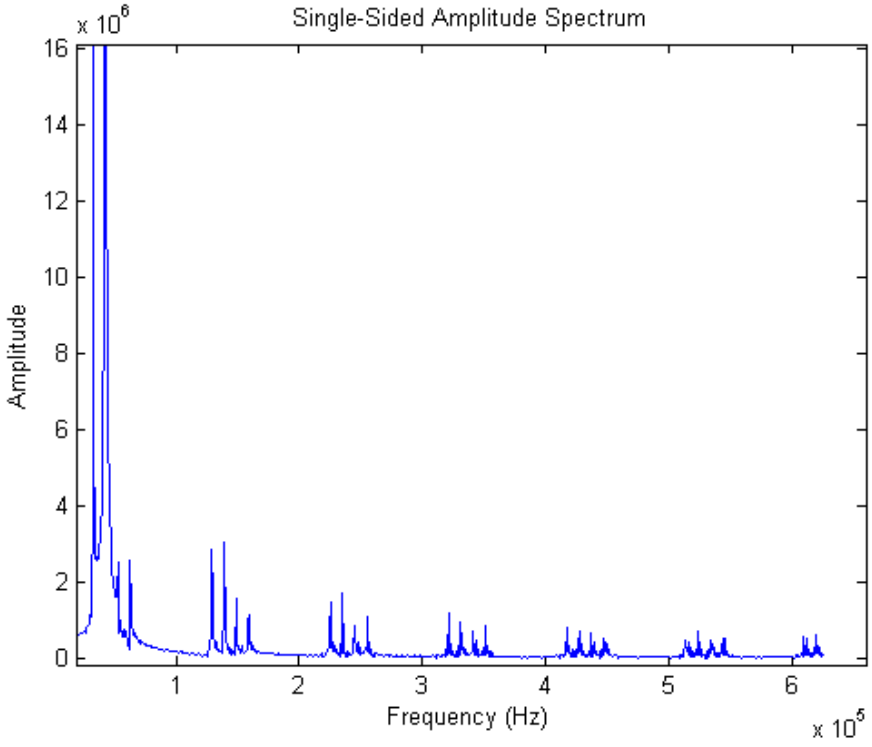

Figure 4.8. AM using different sample rates of carrier and message.

4.3.2 Upsampling

Using integer upsampling, a factor of two would suffice to fulfill the Nyquist theorem. However, an FM carrier with an even higher frequency will have to be generated in a later stage which demands a higher sample rate. In addition, the DAC provided by the client has both upper and lower limits on sample rate forcing an upsampling factor of at least 64, yielding a sample rate of 6.144 MSPS. To ease the requirements, the filter was split into two stages, each with an upsampling factor of eight. For implementation, the same procedure was used as for the bandlimiting filter, i.e., a Xilinx FIR IP core with coefficients extracted from MATLABs filter design toolbox. This resulted in a filter order of 25 for the first stage and 18 for the second stage, both time-multiplexed to enable filtering

of interleaved stereo sound samples. The frequency responses are shown in Figs. 4.9 and 4.10.

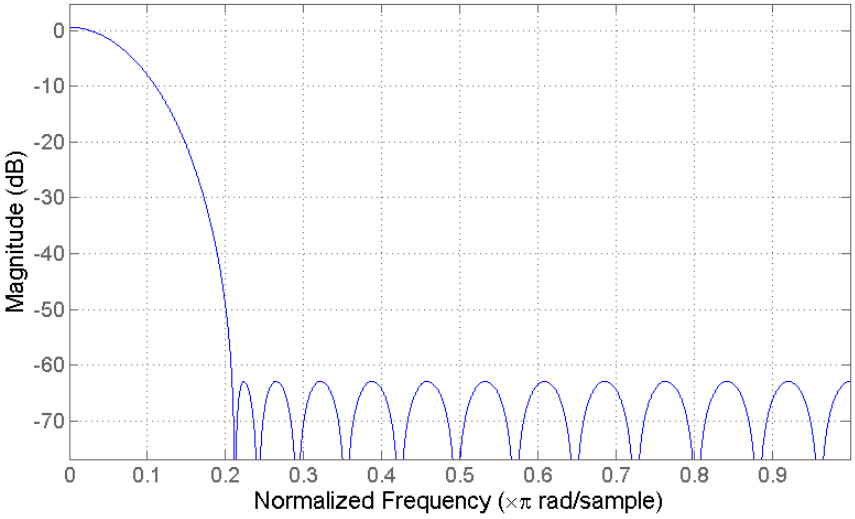

Figure 4.9. First filter stage frequency response.

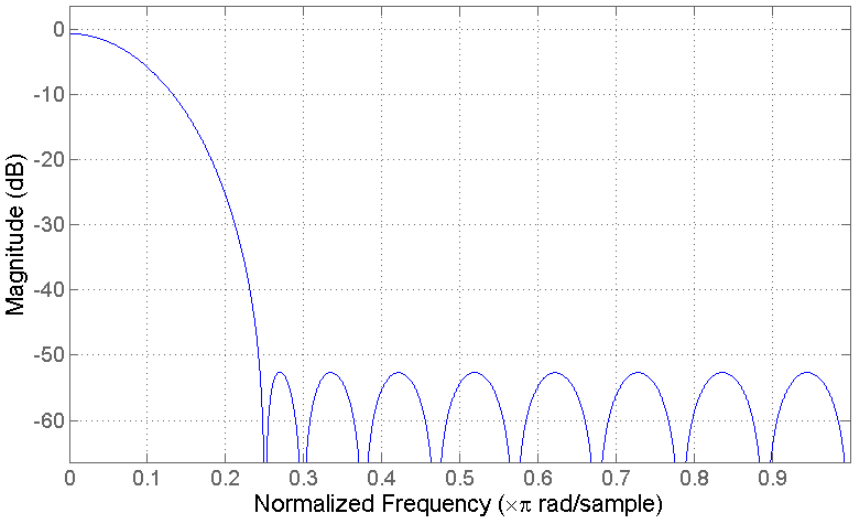

Figure 4.10. Second filter stage frequency response.

4.3.3 Stereo multiplexer

The architecture of the multiplexing unit is shown in Fig. 4.11.

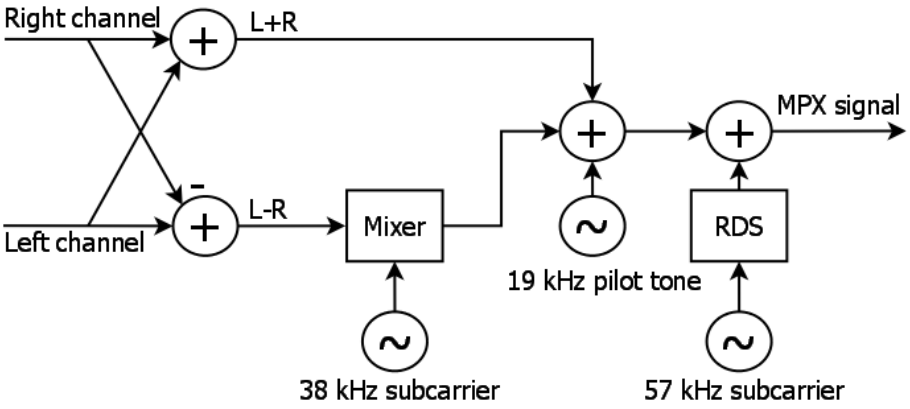

Figure 4.11. Stereo multiplexing architecture.

According to the recommendations from ITU-R, the amplitudes of the mono signal and stereo signal should represent no more than 90 % of the total baseband amplitude in the case of left and right channels being equal and in-phase and equal and opposite-phase, respectively. The pilot tone should have a relative amplitude of 8 to 10 % and the 38 kHz sub-carrier 1 % with a precision of 2 Hz and 4 Hz, respectively. All plots presented hereafter in this section are based on actual data extracted from the FPGA using ChipScope. Figure 4.12 shows the frequency spectrum of the stereo multiplex baseband when 15 kHz in-phase sinusoids are applied to the input. Using the values presented in the plot, the relative amplitude of the pilot tone can be estimated to

$$\frac{869948}{869948 + 7.16174 \cdot 10^6} \approx 10.83\%$$

and the mono signal to

$$\frac{7.16174 \cdot 10^6}{869948 + 7.16174 \cdot 10^6} \approx 89.17\%$$

indicating that the amplitude of the pilot tone is slightly higher than the specified 10 %.

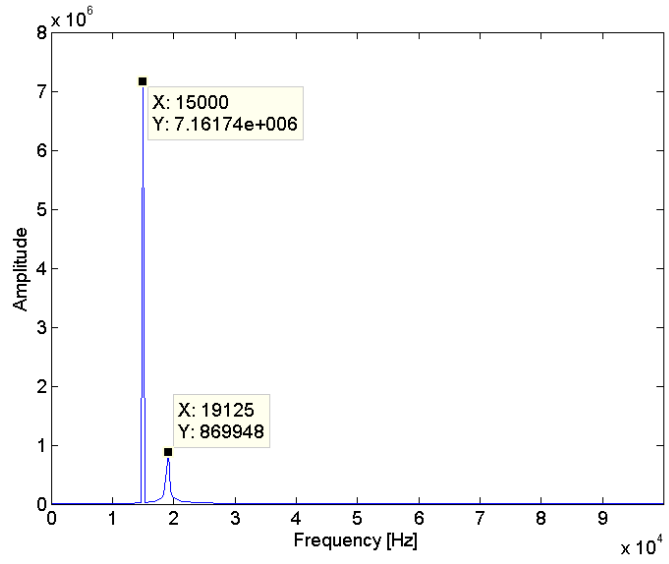

Figure 4.12. Mono-only baseband spectrum.

Figures 4.13 and 4.14 show the unmodulated and AM modulated sub-carrier in the case of 15 kHz opposite-phase sinusoids.

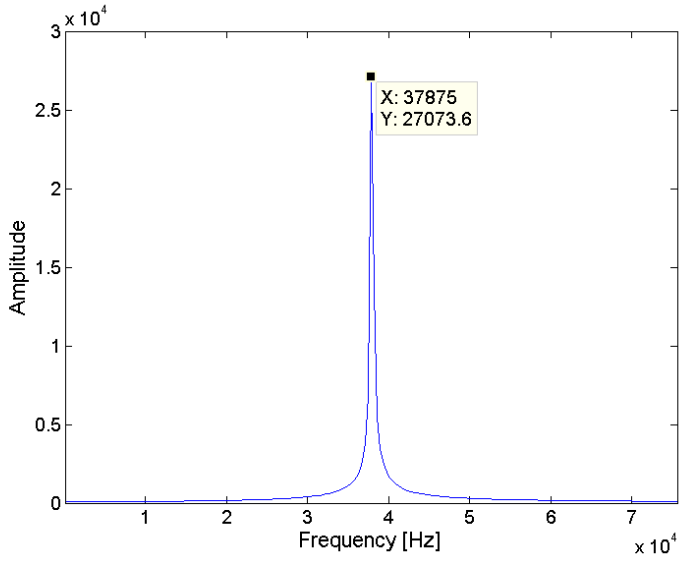

Figure 4.13. Unmodulated sub-carrier.

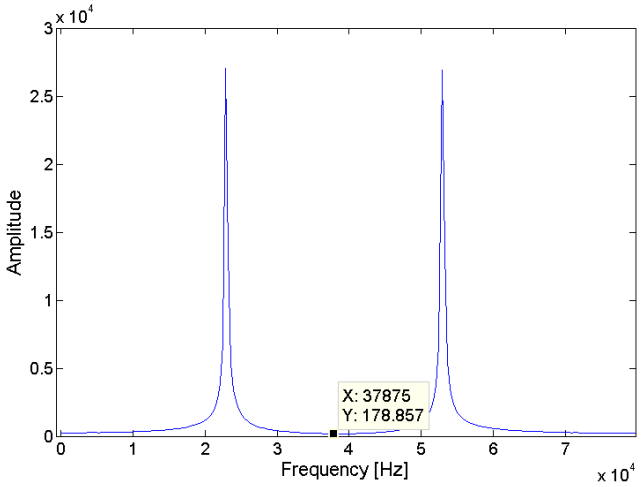

Figure 4.14. AM modulated sub-carrier.

The residual amplitude of the sub-carrier is estimated to

$$\frac{178.857}{27073.6} \approx 0.66\%$$

hence fulfilling the recommended maximum of 1 %.

Figure 4.15 shows the stereo-only baseband spectrum.

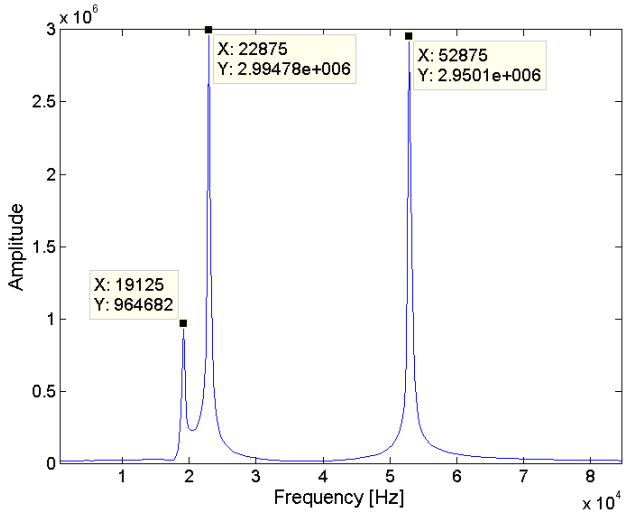

Figure 4.15. Stereo-only baseband spectrum.

Analagous to the previous cases, the relative amplitude of the sidebands is estimated to

$$\frac{2.99478 \cdot 10^6 + 2.9501 \cdot 10^6}{2.99478 \cdot 10^6 + 2.9501 \cdot 10^6 + 964682} \approx 86.04\%$$

and the pilot tone is estimated to

$$\frac{964682}{2.99478 \cdot 10^6 + 2.9501 \cdot 10^6 + 964682} \approx 13.96\%.$$

Again the amplitude of the pilot tone is higher than that recommended, the effect of which is uncertain. No discernable disturbances can be heard when listening to the modulated audio samples through a standard FM receiver, but that is of course a highly subjective assessment. No specifications are given as to why the pilot tone should have a relative amplitude of 10 %, but one possibility is that the amplitude should be large enough to correctly recreate the sub-carrier but not so large that power is wasted.

The frequency spectrums shown in Figs. 4.12 – 4.15 indicate another interesting issue, namely that the precision of the pilot tone and sub-carrier is quite poor. To investigate this fact, the Fast Fourier Transform (FFT) of a stereo multiplex baseband, created directly in MATLAB, was calculated. The result was that even though close to ideal signals were used, the exact values are still not shown in the plot as seen in Fig. 4.16. This error occurs due to leakage and when transforming a signal that does not contain an integer number of periods and a number of samples that is not a power of two.

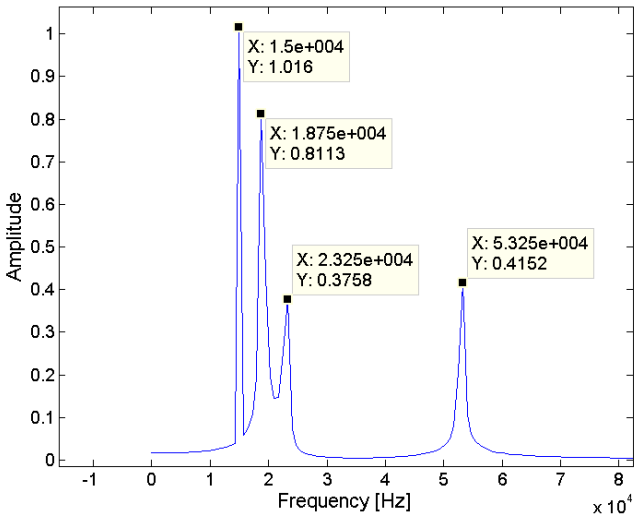

Figure 4.16. Ideal baseband spectrum.

ChipScope was again used to extract data samples from the pilot tone and the stereo sub-carrier. Using the plots shown in Figs. 4.17 and 4.18, the frequency was calculated in the time domain over 50 periods.

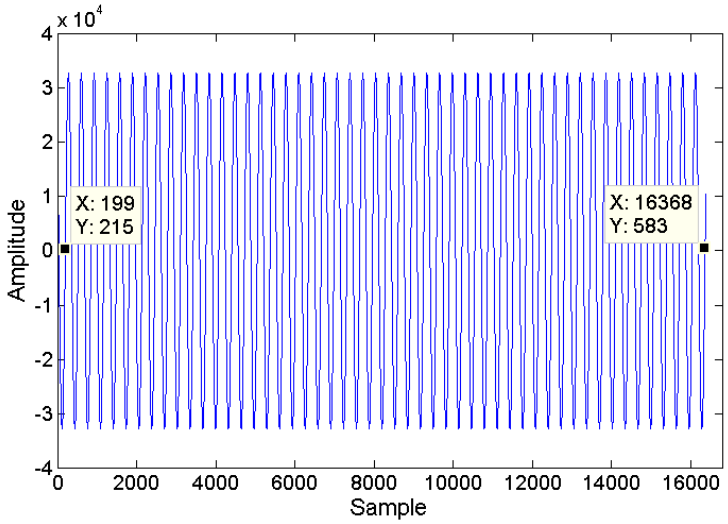

Figure 4.17. Pilot tone in the time domain.

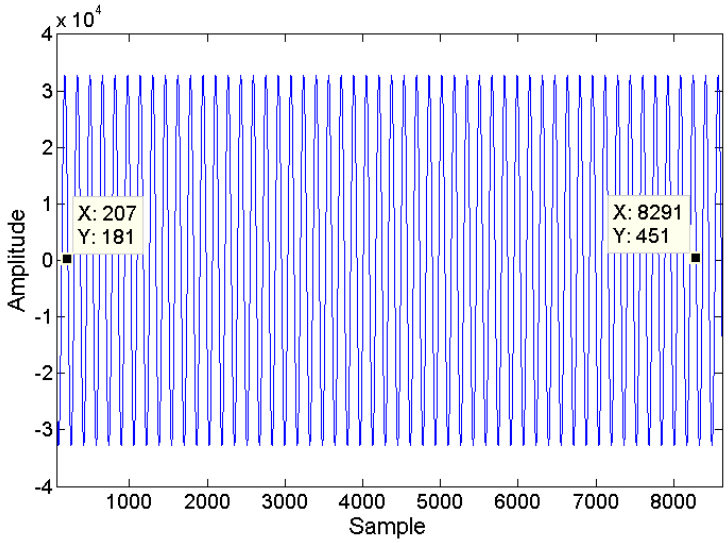

Figure 4.18. Stereo sub-carrier in the time domain.

With the values presented in Figs. 4.17 and 4.18, the pilot tone frequency is calculated to be

$$\frac{50 \cdot 6144000}{16368 - 199} = 18.9993196... \cdot 10^3 \approx 18999 \text{ Hz}$$

and the sub-carrier frequency is calculated to be

$$\frac{50 \cdot 6144000}{8291 - 207} = 38.0009896... \cdot 10^3 \approx 38001 \text{ Hz}$$

According to the time domain calculations, the pilot tone and sub-carrier both have an error of 1 Hz instead of 125 Hz as suggested by the frequency domain plots which is more than sufficient since the ITU-R recommendations specify 2 Hz and 4 Hz, respectively, with a phase difference of no more than 3°. Figure 4.19 shows a plot of the pilot tone and sub-carrier where the zero crossings seem to indicate that they are in-phase.

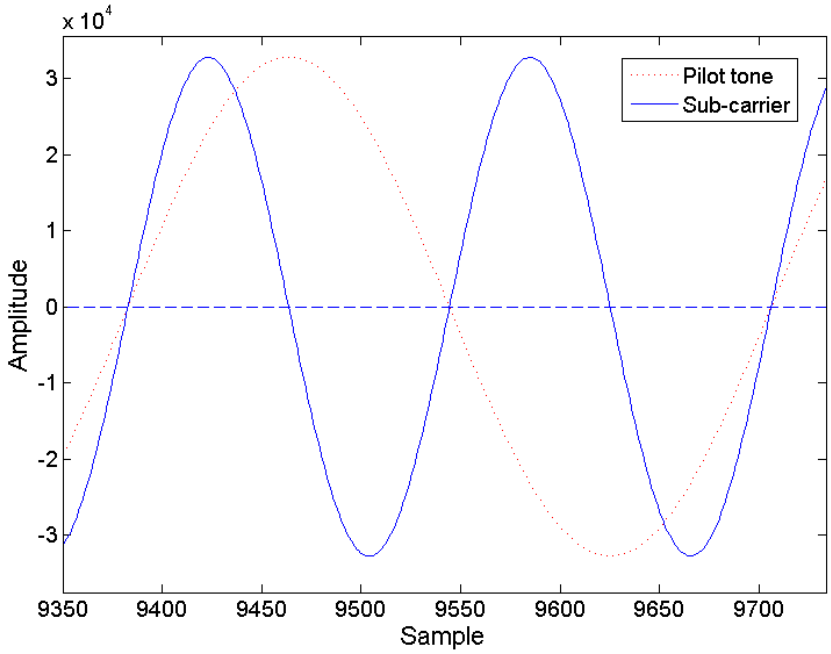

Figure 4.19. Zero crossings of pilot tone and sub-carrier.

Figure 4.20 shows a close-up of one of the zero crossings and it is clearly seen that both signals change sign from one sample to the next.

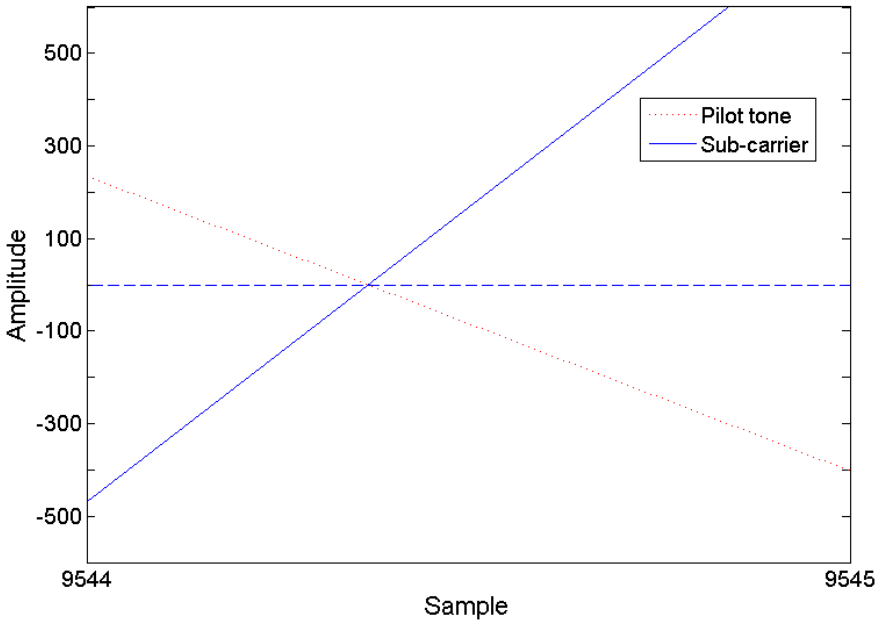

Figure 4.20. Close-up of zero crossing.

Since the signals are discrete, it is not really meaningful to calculate the phase difference exactly since it would require calculations with fractions of samples. It is at least certain that both signals change sign within one sample which sets a bound on the phase error to

$$\text{error} \leq \frac{360^\circ \cdot \text{signal frequency}}{\text{sample frequency}} = \frac{360^\circ \cdot 38000}{6144000} \approx 2.23^\circ$$

and thus falls within the tolerance specified by ITU-R.

4.4 FM block

The main component in a digital FM modulator is a DDS which achieves waveform synthesis by addressing a LUT that stores samples of the desired waveform, in this case a sinusoid. The address is continuously accumulated to step through the entire LUT. To frequency modulate a signal, a control word corresponding to the desired carrier frequency is added to the modulating signal before accumulation as shown in Fig. 4.21. Although the main concept is simple, designing a high quality DDS would be a quite complex and time consuming task, leaving a Xilinx IP core as the only feasible choice for this thesis.

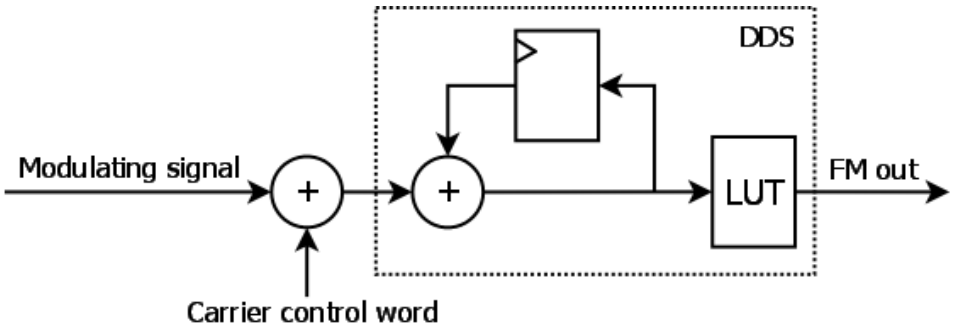

Figure 4.21. Simplified DDS architecture.

Since it is very important for the frequency deviation not to exceed 75 kHz in order to maintain a 200 kHz bandwidth, the phase increment input to the accumulator of the DDS is continously fed back and compared with the maximum allowed value. If the signal is too strong, it is adjusted to an acceptable level. The setup is shown in Fig. 4.22.

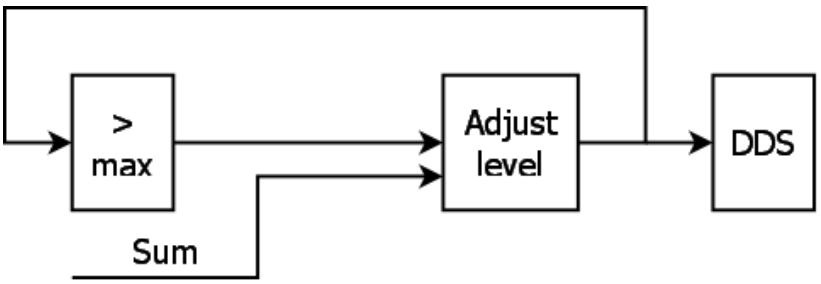

Figure 4.22. Level adjustment feedback loop.

Using ChipScope, the FM signal and the maximum value of the phase increment input at the accumulator was extracted. The maximum value of the phase increment was reported as 609660245. According to [4], the output frequency can be calculated as

$$f_{out} = \frac{f_{clk} \cdot \Delta\Theta}{2^B}$$

where $\Delta\Theta$ is the phase increment and B is the number of bits. The clock frequency, f_{clk}, is 125 MHz but in this case, the DDS is only enabled when a new sample is to be produced which means the effective f_{clk} is the same as the sample frequency. Inserting the extracted values gives the maximum output frequency as

$$f_{out} = \frac{6.144 \cdot 10^6 \cdot 609660245}{2^{32}} \approx 872.126\ kHz.$$

In this case, the frequency of the carrier was chosen to 800 kHz, giving a maximum deviation of 72.126 kHz. The modulating signal is mono, consisting of a 15 kHz sinusoid, giving a modulation index of

$$m = \frac{72.126}{15} \approx 4.8.$$

According to (2.4) and using this value, the bandwidth can be approximated using (2.7) presented in Chapter 2. Hence,

$$\text{BW} \approx 2(\delta + 2f_m) = 2f_m(m+2) = 2 \cdot 15 \cdot 10^3(4.8+2) \approx 204kHz.$$

Figure 4.23 shows the frequency spectrum of the FM signal whose bandwidth agrees rather well with the above approximation.

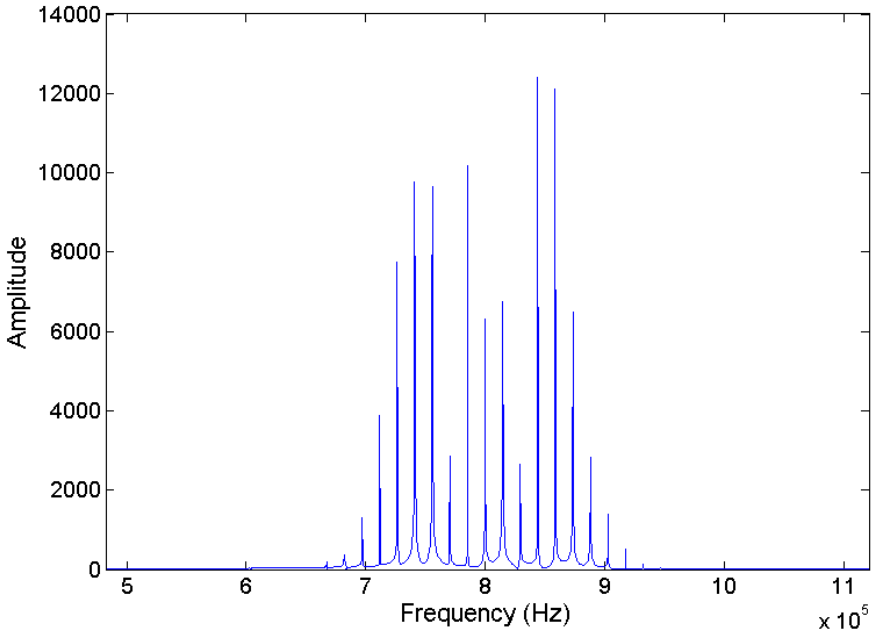

Figure 4.23. FM spectrum.

4.5 RDS block

Due to time considerations, the RDS functionality had to be omitted. The same component that generates the pilot tone and stereo sub-carrier is prepared to also generate the 57 kHz RDS sub-carrier but the modulator itself is not implemented.

Chapter 5

Results and performance

This chapter presents the results and performance of the final implementation along with area reports. The area usage, reported in Table 5.2, implies that it would be possible to modulate eight FM channels using the targeted FPGA with the Block Random Access Memory (BRAM)s being the bottleneck. Through some simple optimizations, presented throughout the chapter, this number can be increased.

5.1 Resource utilization

The resources available on the FPGA are summarized in Table 5.1 [11].

Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kiloByte (kB) BRAMs**
15822	126576	31644	180	268

Table 5.1. Available FPGA resources.

5.1.1 Complete design

Due to additional control logic between the blocks, which is not visible in the area reports, the sum of area utilization for all blocks does not add up to the total usage reported in Table 5.2.

	Slices	Flip-flops	LUTs	DSP48A1 slices	18 kB BRAMs
Amount used	743	2560	1613	12	30
Percentage of available resources	4.70 %	2.02 %	5.10 %	6.67 %	11.19 %

Table 5.2. Resources used by the complete design.

5.1.2 Pre-emphasis block

The pre-emphasis block uses a relatively high number of multipliers compared to other blocks. One of the multipliers is used by the bandlimiting filter IP and cannot be removed through optimization. However, because the pre-emphasis filter runs at a very low sample rate compared to the clock frequency, it would be possible to utilize time-multiplexing control logic and let one filter process both the right and the left channel instead of using one filter for each channel, thereby reducing the number of multipliers by 50 %.

Complete block

Table 5.3 shows the area usage for the complete pre-emphasis block.

	Slices	Flip-flops	LUTs	DSP48A1 slices	18 kB BRAMs
Amount used	212	891	434	7	0
Percentage of utilized resources	28.53 %	34.81 %	26.91 %	58.33 %	0 %
Percentage of available resources	1.34 %	0.70 %	1.37 %	3.89 %	0 %

Table 5.3. Resources used by the pre-emphasis block.

Bandlimiting filter

Table 5.4 shows the area usage for the bandlimiting filter.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	68	226	137	1	0
Percentage of utilized resources	9.15 %	8.83 %	8.49 %	8.33 %	0 %
Percentage of available resources	0.43 %	0.18 %	0.43 %	0.56 %	0 %

Table 5.4. Resources used by the bandlimiting filter.

The bandlimiting filter could be further time-multiplexed to process more channels.

Pre-emphasis filter

Table 5.5 shows the area usage for the pre-emphasis filter.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	102	540	223	6	0
Percentage of utilized resources	13.73 %	21.10 %	13.83 %	50 %	0 %
Percentage of available resources	0.64 %	0.43 %	0.70 %	3.33 %	0 %

Table 5.5. Resources used by the pre-emphasis filter.

It might be possible to utilize time-multiplexing logic for the pre-emphasis filter to replace the three multipliers with just one.

Pre-emphasis buffer

Table 5.6 shows the area usage for the buffer inside the pre-emphasis block.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	14	68	36	0	0
Percentage of utilized resources	1.88 %	2.66 %	2.23 %	0 %	0 %
Percentage of available resources	0.09 %	0.05 %	0.11 %	0 %	0 %

Table 5.6. Resources used by the pre-emphasis buffer.

The buffer is an IP block and cannot be further optimized due to the fact that the code is not available for editing.

Control logic

Table 5.7 shows the area usage of the logic that controls the modules in the pre-emphasis block.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	28	57	38	0	0
Percentage of utilized resources	3.77 %	2.23 %	2.36 %	0 %	0 %
Percentage of available resources	0.18 %	0.05 %	0.12 %	0 %	0 %

Table 5.7. Resources used by control logic.

It might be possible to partly reduce the control logic with the use of Karnaugh maps [1].

5.1.3 Stereo multiplexer block

From Table 5.8, it becomes evident that the stereo multiplexer is very resource demanding compared to the rest of the design which leaves a lot of room for optimization.

Complete block

Table 5.8 shows the area usage of the complete stereo multiplexer block.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	317	1108	603	5	15
Percentage of utilized resources	42.67 %	43.28 %	37.38 %	41.67 %	50 %
Percentage of available resources	2 %	0.88 %	1.91 %	2.78 %	5.60 %

Table 5.8. Resources used by the stereo multiplexer block.

First interpolator stage

Table 5.9 shows the area usage of the first interpolator stage.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	76	242	163	2	0
Percentage of utilized resources	10.23 %	9.45 %	10.11 %	16.67 %	0 %
Percentage of available resources	0.48 %	0.19 %	0.52 %	1.11 %	0 %

Table 5.9. Resources used by the first interpolator stage.

Second interpolator stage

Table 5.10 shows the area usage of the second interpolator stage.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	62	218	130	2	0
Percentage of utilized resources	8.34 %	8.52 %	8.06 %	16.67 %	0 %
Percentage of available resources	0.39 %	0.17 %	0.41 %	1.11 %	0 %

Table 5.10. Resources used by the second interpolator stage.

The interpolation filters could be further time-multiplexed to fit more than one stereo input. The IP core has a limit of 64 channels but since the second stage has an output sample rate of 6.144 MSPS and the clock frequency is 125 MHz, the maximum number of channels for each filter is

$$\left\lfloor \frac{125000000}{6144000} \right\rfloor = 20$$

or ten FM channels since input to the system is stereo. These blocks can of course also be duplicated to further increase the number of channels.

Stereo multiplexer

Table 5.11 shows the area usage of the stereo multiplexer.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	128	490	232	1	15
Percentage of utilized resources	17.23 %	19.14 %	14.38 %	8.33 %	50 %
Percentage of available resources	0.81 %	0.39 %	0.73 %	0.56 %	5.60 %

Table 5.11. Resources used by the stereo multiplexer.

The DDS that generates the stereo pilot tone and the sub-carrier resides within the stereo multiplexer but there is no need to duplicate it for each FM channel. Moving it further up in the design hierarchy allows all stereo multiplexers to share just one DDS, increasing the number of FM channels from 8 to 16.

Stereo multiplexer buffer

Table 5.12 shows the area usage of the buffer inside the stereo multiplexer block.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	10	68	36	0	0
Percentage of utilized resources	1.35 %	2.66 %	2.23 %	0 %	0 %
Percentage of available resources	0.06 %	0.05 %	0.11 %	0 %	0 %

Table 5.12. Resources used by the stereo multiplexer buffer.

The buffer is an IP block and it cannot be further optimized due to the fact that the code is not available for editing.

Control logic

Table 5.13 shows the area usage of the logic that controls the modules in the stereo multiplexer block.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	41	90	42	0	0
Percentage of utilized resources	5.52 %	3.52 %	2.60 %	0 %	0 %
Percentage of available resources	0.26 %	0.07 %	0.13 %	0 %	0 %

Table 5.13. Resources used by control logic.

It might be possible to partly reduce the control logic with the use of Karnaugh maps [1].

5.1.4 FM block

	Slices	Flip-flops	LUTs	DSP48A1 slices	18 kB BRAMs
Amount used	30	164	91	0	15
Percentage of utilized resources	4.04 %	6.41 %	5.64 %	0 %	50 %
Percentage of available resources	0.19 %	0.13 %	0.29 %	0 %	5.60 %

Table 5.14. Resources used by the FM block.

There is no easy way to time-multiplex the DDS that takes care of the FM modulation and it is not entirely certain that it can be done at all. Due to time considerations, this possibility has not been thoroughly investigated. An alternative way of reducing resources is by reducing the output word length from 16 bits to 14 bits. That decreases the number of BRAMs to 14 but it also has a negative effect on the signal quality though not necessarily audible since it also depends largely on the receiver.

5.1.5 Input buffer

Table 5.15 shows the area usage of the input buffer.

	Slices	Flip-flops	LUTs	DSP48A1 slices	18 kB BRAMs
Amount used	15	68	36	0	0
Percentage of utilized resources	2.02 %	2.66 %	2.23 %	0 %	0 %
Percentage of available resources	0.09 %	0.05 %	0.11 %	0 %	0 %

Table 5.15. Resources used by the input buffer.

The buffer is an IP block and it cannot be further optimized due to the fact that the code is not available for editing.

5.1.6 Output buffer

Table 5.16 shows the area usage for the outpuf buffer.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	31	136	72	0	0
Percentage of utilized resources	4.17 %	5.31 %	4.46 %	0 %	0 %
Percentage of available resources	0.20 %	0.11 %	0.23 %	0 %	0 %

Table 5.16. Resources used by the output buffer.

The reason that the output buffer is more resource demanding than the input buffer is because it takes care of clock domain crossing. Data is written on the rising edge of the 125 MHz system clock and read on the rising edge of the 150 MHz DAC clock. It is not possible to make the output buffer less resource demanding due to intellectual property rights. Figures 5.1 – 5.6 show pie charts of how the resource utilization is divided among the blocks.

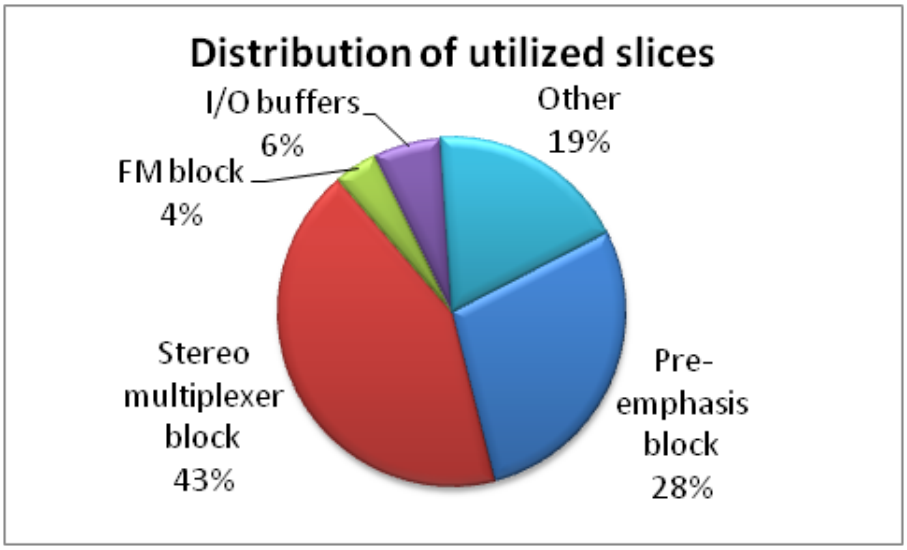

Figure 5.1. Distribution of utilized slices.

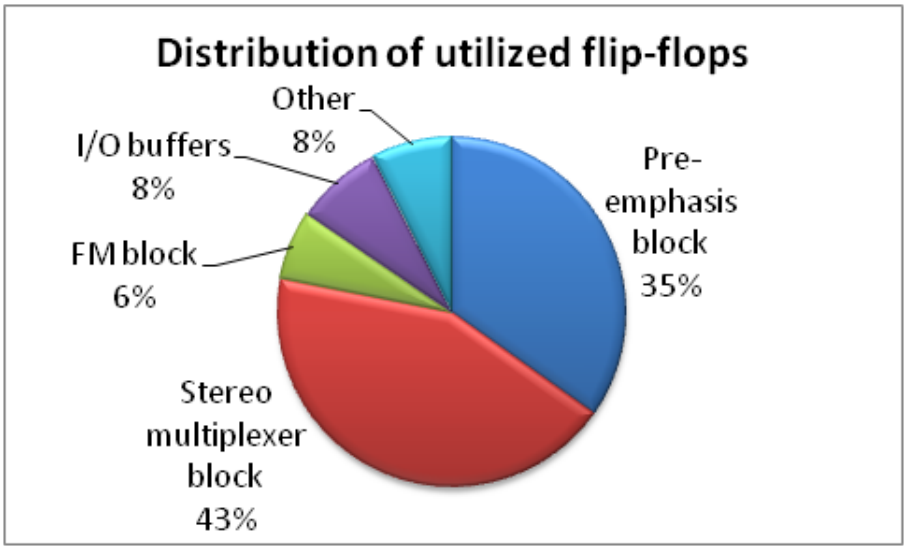

Figure 5.2. Distribution of utilized flip-flops.

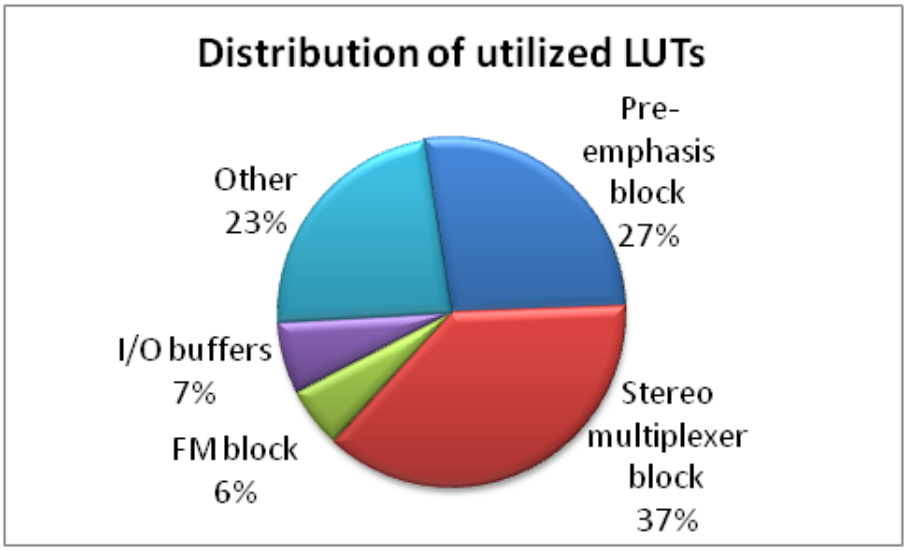

Figure 5.3. Distribution of utilized LUTs.

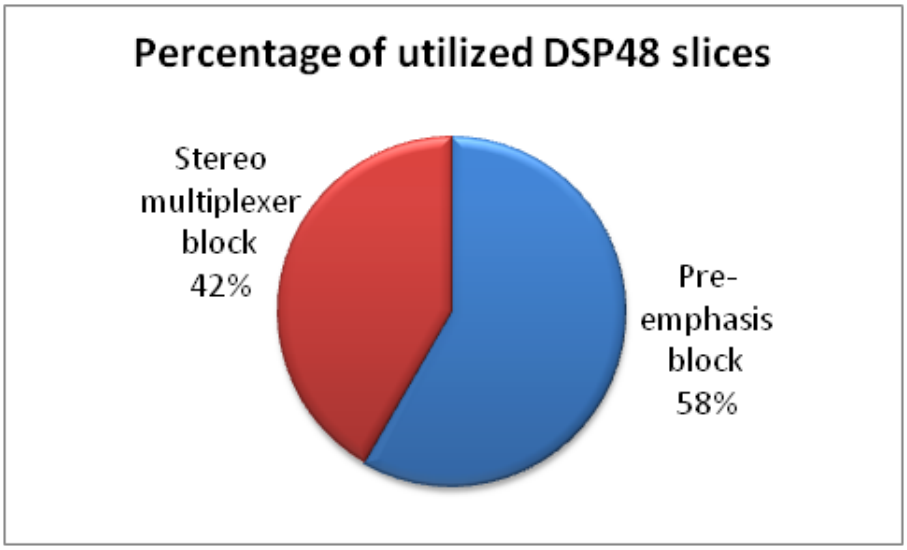

Figure 5.4. Distribution of utilized DSP48 slices.

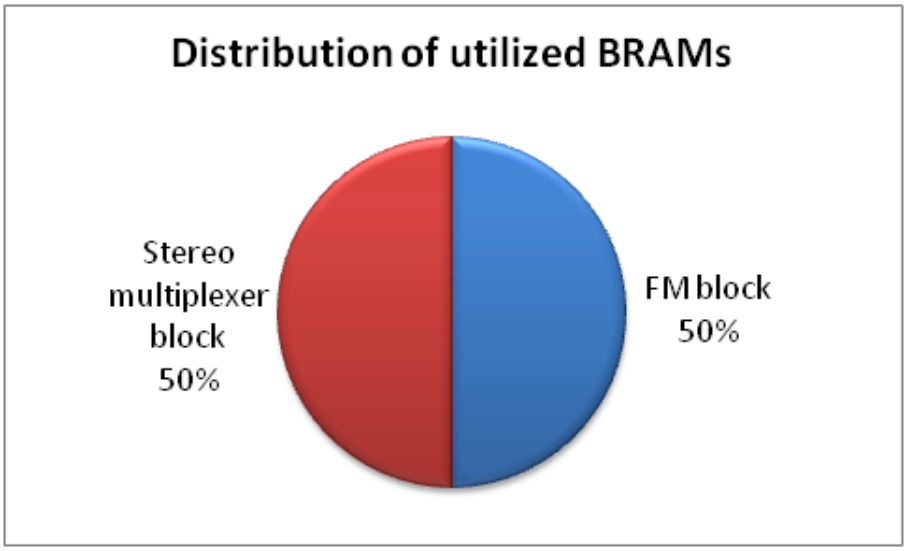

Figure 5.5. Distribution of utilized BRAMs.

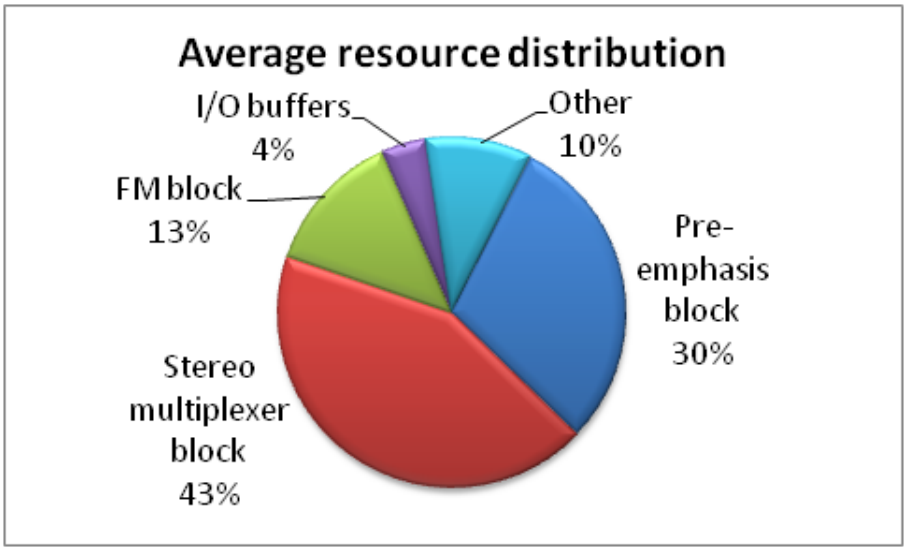

Figure 5.6. Average distribution of all utilized resources.

5.1.7 Resource estimation after optimization

Assuming the FM DDS can not be time multiplexed, it is instead optimized by reducing its output width from 16 bits to 14 bits. The area of the stereo multiplexer is reduced by moving the DDS, generating the pilot tone and sub-carrier, outside of the block and sharing it among all instances. The bandlimiting filter and the interpolation filters can not be further time multiplexed without using at least one BRAM. In order to fit more than ten FM channels, these filters also have to be duplicated which means the three filter IPs and the stereo multiplexer DDS will together use at least $2+2+2+15 = 21$ BRAMs, leaving 247 BRAMs for the FM modulation. These 247 available BRAMs yield

$$\left\lfloor \frac{247}{14} \right\rfloor = 17 \text{ channels.}$$

The pre-emphasis filter has not been time multiplexed or optimized with respect to the number of multipliers because that would produce an overhead in terms of slices which is difficult to estimate. Furthermore, it would not have any impact on the maximum number of channels since the bottleneck lies in the available number of BRAMs.

Table 5.17 shows the estimated resource utilization after optimization. To produce the estimation, all filter IPs have been synthesized with a 17-channel time multiplexing and duplicated once to get 17-channel stereo. All other blocks have simply been duplicated 17 times.

	Slices	**Flip-flops**	**LUTs**	**DSP48A1 slices**	**18 kB BRAMs**
Amount used	6889	28186	13256	131	259
Percentage of available resources	43.54 %	22.27 %	41.89 %	72.78 %	96.64 %

Table 5.17. Resource utilization after optimization.

5.2 Signal quality

It is far from trivial to derive an exact value of the Signal-to-Noise Ratio (SNR) for the entire system wherefore a lower-bound approximation is given instead. Using MATLAB to demodulate the signal, collected from ChipScope, the Root Mean Square (RMS) value of the noisy signal was calculated to 0.251333. To get the RMS of the signal without noise, the well-known formula [17] for the RMS of a sinusoid with amplitude A,

$$A_{RMS} = \frac{A}{\sqrt{2}}, \tag{5.1}$$

was used. Subtracting the ideal average signal amplitude from the average total amplitude gives the average noise amplitude. Figure 5.7 shows a close-up of one of the peaks of the demodulated signal and the value of A that was chosen. The actual peak value of the signal should reside somewhere within the box shown in the figure and the one chosen gives the worst-case approximation with an RMS of

$$\frac{0.351744}{\sqrt{2}} \approx 0.248721.$$

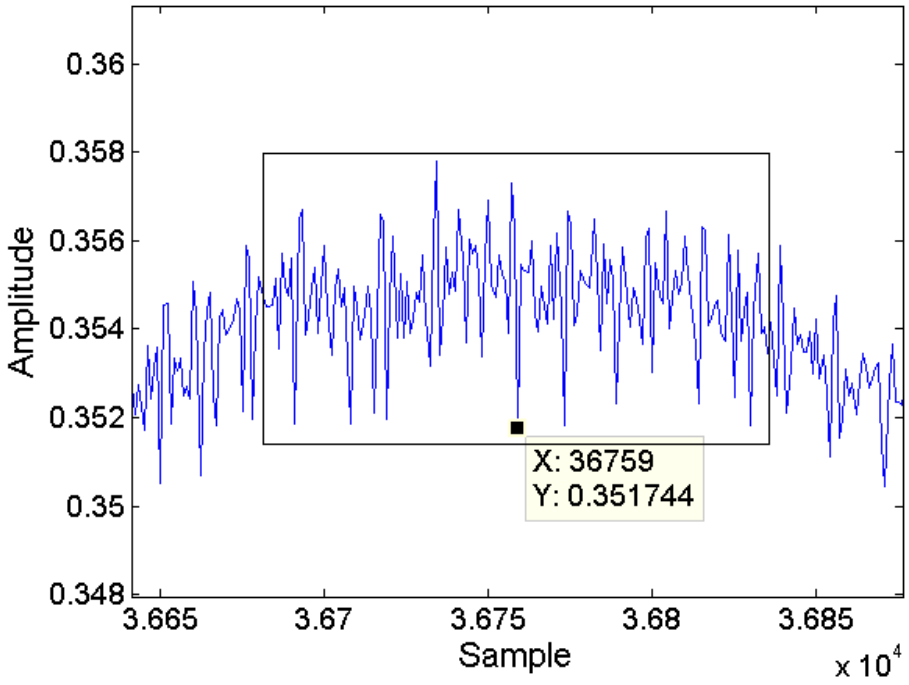

Figure 5.7. Noisy demodulated signal.

Using another well-known formula [16], the SNR can now be calculated to

$$20 \cdot \log_{10}\left(\frac{A_{signal}}{A_{noise}}\right) = 20 \cdot \log_{10}\left(\frac{0.248721}{0.251333 - 0.248721}\right) \approx 39.6dB.$$

By following the signal chain, it was found that the interpolation filters add a lot of noise. Figure 5.8 shows the signal right after it has been bandlimited and pre-emphasized, Fig. 5.9 after the first interpolation stage and Fig. 5.10 after the second stage. It is quite obvious that the first and second interpolation stages should be the focus for improving the SNR.

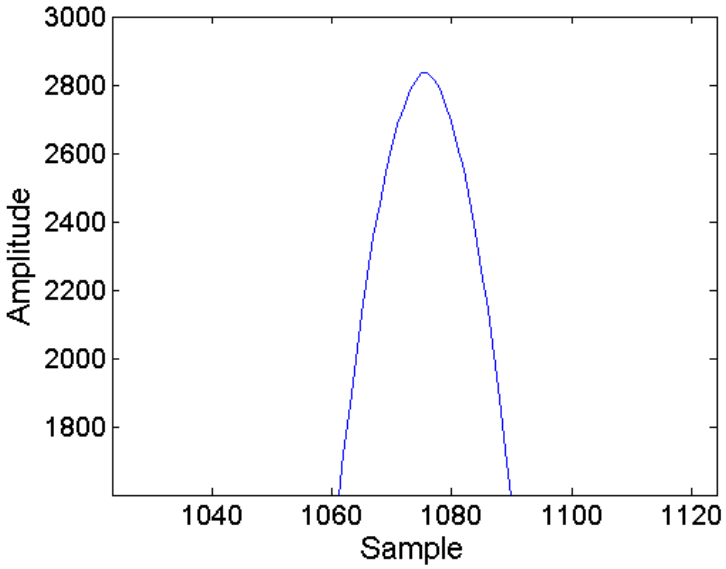

Figure 5.8. Signal after bandlimiting and pre-emphasis.

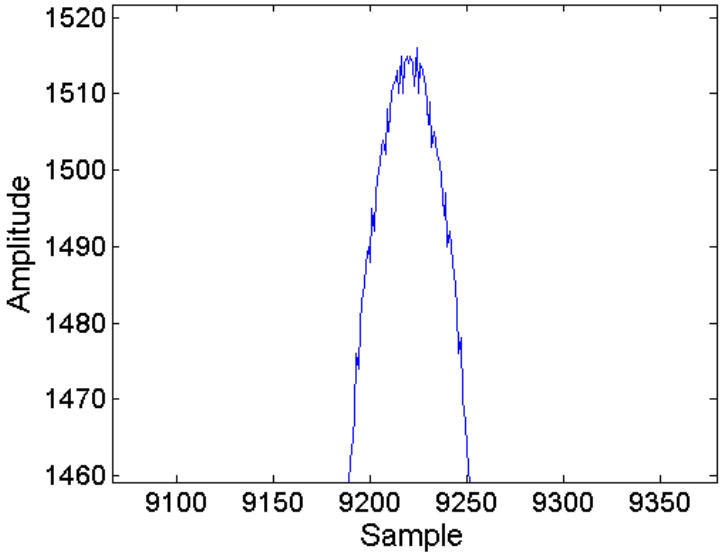

Figure 5.9. Signal after first interpolation stage.

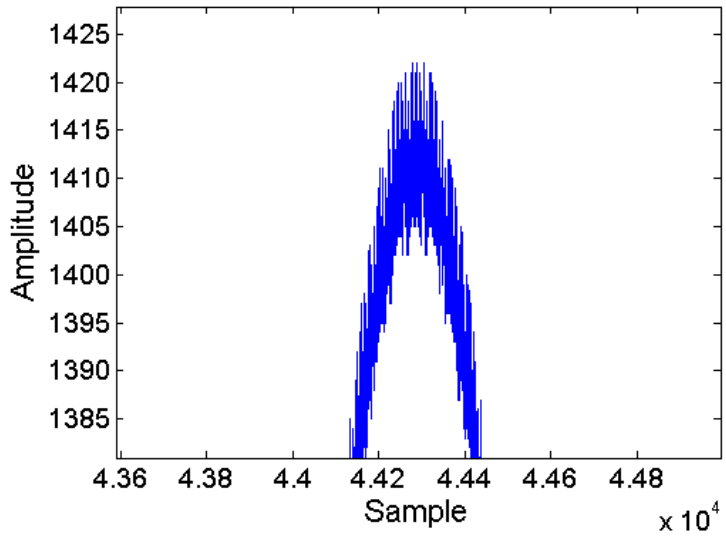

Figure 5.10. Signal after second interpolation stage.

5.3 Performance summary

Some important performance measures are summarized in Table 5.18.

Clock frequency	**Input sample rate**	**Output sample rate**	**SNR**	**Stereo**
125 MHz	48 kSPS	6.144 MSPS	$\approx$ 39.6 dB	Yes
Pilot tone frequency	**Sub-carrier frequency**	**Sub-carrier residual amplitude**	**Phase tolerance**	**RDS**
19001 Hz	38001 Hz	$\approx$ 0.66%	2.23°	No
Pilot tone modulation	**Audio modulation**	**FM carrier deviation**	**Pre-emphasis**	
$\leq$ 13.96 %	$\leq$ 89.17 %	$\leq$ 75 kHz	50 μs	

Table 5.18. Performance summary.

Chapter 6

Summary

The goal of this thesis was to produce a solution that can provide a signal quality good enough for distribution via cable while keeping area minimization as the main focus to allow for as many channels as possible to be modulated using the hardware provided.

The idea has been to first create a system for just one FM channel to prove the theory and the concept and also to reduce the time required to verify the functionality. Several suggestions are given in Chapter 5 as to how this number can be increased.

Although the complexity of an FM modulator is relatively low, the lack of a definitive worldwide standard has called for some delimitations in order to keep the workload to a reasonable level. With additional control logic, adjustable time-constant for the pre-emphasis filter and an implementation of the alternative way of achieving stereophonic transmission, the polar-modulation system, the modulator could be made parameterizable based on the recommendations for a specific country. The modulator presented in this thesis can only be used for broadcasting in Sweden and countries following the same specifications.

Another issue is that FM modulation is traditionally carried out in the analog domain and simply transferring the entire signal processing chain to the digital domain has proven to be a more challenging task than first anticipated. It should be pointed out that while the structure in itself is generic, the IP blocks included restricts the brand of FPGA to Xilinx only.

6.1 Future work

The performance of the implementation is acceptable but there is still room for improvements. Below is a list of suggestions for future work.

- Design a component that automatically adjusts the baseband components to a level that meets the specifications given by ITU-R.
- Implement the RDS modulator.

- Make a complete revision of all sub-systems and carry through with the optimization suggestions given in Chapter 5.
- Add parameters that allow for easy adjustment according to the country in which the modulator is located to make it multi-standard.
- Replace all IP cores with components built using pure VHDL code to provide a system that can be placed on an FPGA of any brand.
- Investigate the design of the interpolation filters to see if the SNR can be improved.

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Upphovsrätt

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