An Energy Efficient Time-Domain Temperature Sensor for Low-Power On-Chip Thermal Management

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***Abstract*— Because temperature variations significantly affect the performance and reliability of highly integrated chips, the thermal management of such chips is an important issue. In this paper, a time-domain process variation calibrated temperature sensor is proposed for on-chip thermal management. For a suitable on-chip implementation, the digitally converted temperature-dependent time signal is used to reduce the area and power consumption of the chip. The proposed temperature sensor is fabricated using a 0.13-μm CMOS technology and has an active area of 0.031 mm^2. Measurement results show an energy consumption of 0.67 nJ/conversion at a 430 kHz conversion rate, with 1.2 V supply voltage. Using one-point calibration, the sensing error is found to range from −0.63 °C to 1.04 °C over a temperature range of 20 °C to 120 °C.**

***Index Terms*— Temperature sensor, one-point calibration, process variation, thermal management, low power.**

I. Introduction

PERFORMANCE of state-of-the-arts microprocessor is substantially enhanced along with recent CMOS process technology scaling. However, it causes the higher temperature due to the larger scale integration than that in the previous CMOS process technology [1]–[3]. The high temperature environment causes the degradation in the efficiency of the power management due to the increased leakage current [4]. Besides, the life time of the product is closely related to its temperature level [5]. Therefore, the thermal management is essential for high performance microprocessors. If the chip temperature is measured at the surface of chip package, it is less accurate than on-chip measurement because of self-heating [6]. Thus, numerous commercial products adopt the on-chip temperature sensor for the effective thermal managements [7], [8]. The variation of the thermal gradient of the recent microprocessors is increasing due to their high integration [9] and thus numerous temperature sensors are implemented in a chip to find the hot-spots of a chip [10]–[12]. Thus, the energy efficiency of the on-chip temperature sensor is very important. The high energy efficiency of the temperature sensor can be achieved by 1) reducing the energy consumption per a single temperature sensing operation and 2) increasing the duration of the idle-state of the temperature sensor. These two requirements can be fulfilled by a high conversion rate. Because the sensing operation can be completed quickly with a high conversion rate, the energy consumption per a single temperature sensing can be reduced and the temperature sensor can secure more idle-state. Thus high conversion rate is required for the temperature sensors used in the microprocessors. In addition to the high conversion rate, the on-chip temperature sensor should have a compact size because numerous temperature sensors are used to find the hot-spots of microprocessors.

Previous temperature sensors can be categorized into two types: voltage- and time-domain temperature sensors. The voltage-domain temperature sensor converts the measured temperature into the BJT's base-emitter voltage or MOSFET's gate-source voltage, and then the voltage is converted into the digital code by an analog-to-digital converter (ADC) [13]–[17]. Recent voltage-domain temperature sensors achieve the higher sensing accuracy than ±0.25 °C with the higher resolution than 0.025 °C. The conversion rate of 10 Hz and the chip size of larger than 0.26 mm^2 were achieved [15]–[17]. However, the conversion rate of a few tens of Hz and the large chip area are not suitable for the on-chip thermal management in the high performance microprocessor. On the other hand, the time-domain temperature sensor converts the measured temperature into a delay which is proportional to temperature. The delay is converted into the digital code by a time-to-digital converter. The size of time-domain temperature sensor was reduced as low as 0.0324 mm^2 with 0.18-μm CMOS process and its conversion rate was improved to 1 kHz [18]. The time-domain temperature sensor using FPGA improves the conversion rate to 3 kHz [19]. Thus, the time-domain temperature sensor is more suitable for the on-chip thermal management in terms of the chip area and the conversion rate than voltage-domain temperature sensor. However, because the delay is not only affected by the temperature, but also the process variation, the previous time-domain temperature sensors perform the two-point calibration to calibrate the process variation [19], [20]. Since two-point calibration requires measurement results at two known temperature, it causes large production

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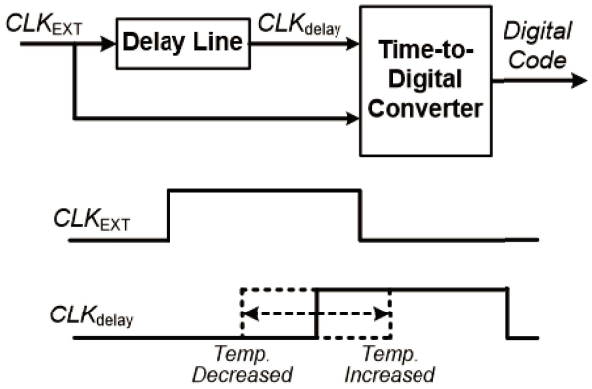

Fig. 1. Conceptual block diagram and waveform of the conventional time-domain sensor.

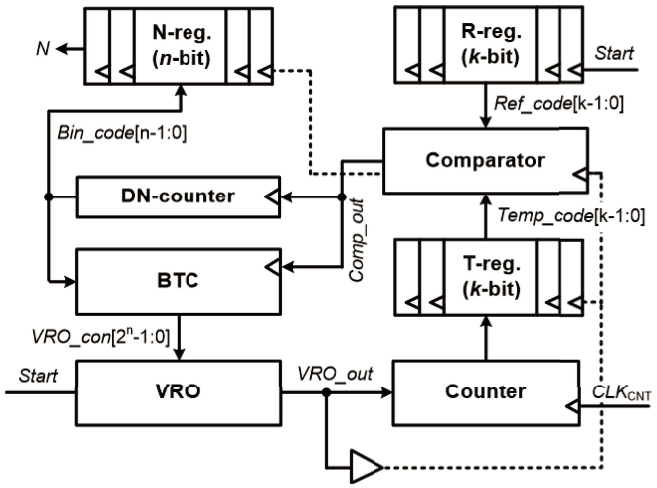

Fig. 2. Block diagram of proposed temperature sensor.

cost. To solve this problem, the temperature sensor adopting one-point calibration was suggested. It requires measurement result at only one known temperature point but it shows compatible measurement accuracy with temperature sensors with two-point calibration. Because of its simpler operation, it can save high-volume production cost by saving calibration time [21]. Thus, the recent time-domain temperature sensor adopts a one-point calibration [21]–[24].

In this paper, we propose a 0.67 nJ/conversion, 430 kHz process variation calibration time-domain temperature sensor for low power on-chip thermal management. For suitable low power on-chip composition with process variation calibration, the proposed temperature sensor uses the digital code difference between the measured code and externally applied code instead of the reference generator [21], [23] and the one-point calibration is adopted. This paper is organized as follows. Section II describes operation principle. Section III presents design implementations with operation details. Section IV shows the measurement results of the proposed temperature sensor and compares the results with those of previous time-domain temperature sensors. Finally, Section V concludes this paper.

II. Principles of Operation

The conceptual block diagram and operation of the conventional time-domain temperature sensor are shown in Fig. 1. The basic principle of the conventional time-domain temperature sensor is as follows. First, the external clock (CLK_{EXT}) is applied to the delay line and the delayed clock (CLK_{delay}) is generated. The delay line commonly consists of the set of CMOS gates. In this case, the delay between CLK_{EXT} and CLK_{delay} is dependent on the temperature variation [25]. The time-domain temperature sensor measures the temperature by measuring the delay between the CLK_{EXT} and the CLK_{delay}.

The proposed temperature sensor, shown in the Fig. 2, is the improved version of the conventional temperature sensor in Fig. 1. The proposed temperature sensor consists of five types of components; a VRO, a counter, three registers (N-register, T-register, and R-register), a comparator, a binary-to-thermometer converter (BTC), and a down counter (DN-counter). The VRO consists of 2^{n} variable delay cells, and the N-register, the DN-counter, and the BTC have n-bits to control the variable delay cells in the VRO. The T-register, the R-register, and counter are designed to have k-bits. The details about these building blocks will be described in the Section III.

In the proposed temperature sensor, a variable ring oscillator (VRO), which is composed of the set of CMOS gates, is used instead of the delay line in Fig. 1. The proposed temperature sensor measures the pulse width of the VRO's output (*VRO_out*). However, because the pulse width of the *VRO_out* ($PW_{\mathrm{VRO\_out}}$) is affected by not only the temperature variation but also the process variation, the latter should be compensated in order to sense the temperature accurately. Thus, the proposed temperature sensor senses the temperature during the sensing mode after compensating the effect of process variation using one-point calibration during the calibration mode. The following subsections describe the operation principles of the process variation compensation and temperature sensing of the proposed temperature sensor.

A. Calibration Mode

The delay of CMOS inverter can be simply represented by the temperature-only-dependent term and process-only-dependent term as below [21].

$$D_{\mathrm{inv}} = T^{-\alpha} \cdot P_{\mathrm{inv}} \tag{1}$$

where D_{inv} is the delay of CMOS inverter, T is the absolute temperature, α is a temperature coefficient that depends on the process technology, and P_{inv} is a process-only-dependent term in the delay of the inverter. In the same manner, the delay of the VRO, which is composed of the delay cells with equal NMOS and PMOS driving strengths, can be expressed by the temperature-only-dependent term and process-only-dependent. Thus, $PW_{\mathrm{VRO\_out}}$ is expressed as the following equation.

$$PW_{\mathrm{VRO\_out}} = N \cdot D_{\mathrm{cell}} = N \cdot T^{-\alpha} \cdot P_{\mathrm{cell}} \tag{2}$$

where N is the number of the activated delay cells in VRO, D_{cell} is the delay of a single delay cell, and the P_{cell} is the

process-only-dependent term in the delay of the delay cell. Since $PW_{\mathrm{VRO\_out}}$ is affect by the process variation, as shown in (2), the calibration needs to be performed to cancel out the effect of process variation. In the calibration mode, N is adjusted according to P_{cell} such that $PW_{\mathrm{VRO\_out}}$ has a specific value, T_{ref}, to cancel the effect of the process variation at the calibration temperature (T_{C}). Then, the adjusted $PW_{\mathrm{VRO\_out}}$ at T_{C} ($PW_{\mathrm{VRO\_outC}}$) can be written as

$$PW_{\mathrm{VRO\_outC}} = N_{\mathrm{C}} \cdot D_{\mathrm{cell\_C}} = N_{\mathrm{C}} \cdot T_{\mathrm{C}}^{-\alpha} \cdot P_{\mathrm{cell}} = T_{\mathrm{ref}} \quad (3)$$

where N_{C} is the number of activated delay cells in the VRO at T_{C}, and $D_{\mathrm{cell\_C}}$ is the delay of a single delay cell at T_{C}.

B. Sensing Mode

After the calibration mode, the proposed system enters the sensing mode. If the temperature changes from T_{C} to a certain operation temperature (T_{O}), $PW_{\mathrm{VRO\_out}}$ at T_{O} becomes different from $PW_{\mathrm{VRO\_outC}}$ owing to the temperature-dependent term T in (2). In the sensing mode, the proposed temperature sensor readjusts N to match $PW_{\mathrm{VRO\_out}}$ with T_{ref}. As a result, the adjusted $PW_{\mathrm{VRO\_out}}$ at T_{O} ($PW_{\mathrm{VRO\_outO}}$) is expressed as the following equation.

$$PW_{\mathrm{VRO\_outO}} = N_{\mathrm{O}} \cdot D_{\mathrm{cell\_o}} = N_{\mathrm{O}} \cdot T_{\mathrm{O}}^{-\alpha} \cdot P_{\mathrm{cell}} = T_{\mathrm{ref}} \quad (4)$$

where N_{O} is the number of activated delay cells in the VRO at T_{O} and $D_{\mathrm{cell\_O}}$ is the delay of a single delay cell at T_{O}. By solving (3) and (4), T_{O} becomes

$$T_{\mathrm{O}} = T_{\mathrm{C}} \left(\frac{N_{\mathrm{O}}}{N_{\mathrm{C}}} \right)^{\alpha} \quad (5)$$

Since the process-dependent term P_{cell} is eliminated in (5), T_{O} can be obtained by the known parameters T_{C}, N_{C}, and N_{O}, which are independent of the process variation.

In summary, the proposed temperature sensor runs in the calibration mode in advance and finds the N_{C}; the number of active delay cells in VRO when $PW_{\mathrm{VRO\_out}}$ equals to the specific time, T_{ref}, at the known temperature T_{C}. In the sensing mode, the proposed temperature sensor finds the N_{O}; the number of active delay cells in VRO when $PW_{\mathrm{VRO\_out}}$ equals to the T_{ref} at the unknown temperature T_{O}. By using (5), the unknown operating temperature T_{O} can be obtained regardless of the process variation.

III. Design Implementation With Operation Details

For suitable low-power on-chip implementation, the proposed temperature sensor is designed to achieve low energy consumption per conversion with a high conversion rate, as well as to eliminate the effect of process variation on the sensing accuracy using one-point calibration. Previous temperature sensors include a large power- and area-consuming reference generator to produce a process- and temperature- independent reference clock [21], [23]. To meet our design objectives, the proposed temperature sensor uses a digital code instead of this reference clock and thus saves significant power and area. In addition, the digital code-based processing decreases the time to determine how much the temperature varies. This allows the conversion rate to be improved to 430 kHz.

The number of bits of the N-register, DN-counter, and BTC, n, is determined by the maximum N_{O}, where N_{O} is the number of activated delay cells in VRO, and the number of bits for the T-register, R-register, and comparator, k, is determined by the *Ref_code*[k-1:0], where *Ref_code*[k-1:0] is the output of the R-register. The maximum N_{O} and *Ref_code*[k-1:0] are determined by the trade-off between sensing accuracy and area overhead.

The unknown temperature, T_{O}, is calculated from the ratio of N_{C} and N_{O} as in (5). To increase the sensing accuracy, large values of N_{C} and N_{O} are preferred because the ratio of N_{C} and N_{O} can be calculated more precisely with large values of N_{C} and N_{O}. Thus, from (3) and (4), a large T_{ref} is required to achieve a high sensing accuracy. The T_{ref} is determined by the *Ref_code*[k-1:0] and the period of the CLK_{CNT} (T_{CLKCNT}). The counter and T-register count the number of cycles of CLK_{CNT} during $PW_{\mathrm{VRO\_out}}$ (*Temp_code*[k-1:0]) and compare the counted number with *Ref_code*[k-1:0]. The control bit of the VRO (*Bin_code*[n-1:0]) is adjusted by the comparison results until *Temp_code*[k-1:0] equals to *Ref_code*[k-1:0]. When *Temp_code*[k-1:0] becomes equal to *Ref_code*[k-1:0], $PW_{\mathrm{VRO\_out}}$ becomes equal to the product of T_{CLKCNT} and *Ref_code*[k-1:0]. Thus the T_{ref} in (3) and (4) can be expressed as below.

$$T_{\mathrm{ref}} = T_{\mathrm{CLKCNT}} \cdot Ref\_code[\mathrm{k\text{-}1:0}] \quad (6)$$

Thus, a large *Ref_code*[k-1:0] is required to increase T_{ref} and the sensing accuracy. But the use of large *Ref_code*[k-1:0] requires the large number of bits for the R-register, T-register, comparator, and counter, leading to area overhead. In addition, the increased T_{ref} by using large *Ref_code*[k-1:0] also requires the large number of bits for the N-register, DN-counter, and BTC, leading to area overhead, too. By considering the trade-off between temperature sensing accuracy and area overhead, the *Ref_code*[k-1:0] is determined to 10 1011 1001. Thus, 10 bits is used for the T-register, R-register, comparator, and counter. On the other hand, T_{ref} is obtained from (6) using the *Ref_code*[k-1:0]. Then, the maximum value of N_{O} can be calculated from the obtained T_{ref}, (4), and $D_{\mathrm{cell\_O}}$ with T_{O} being the lowest temperature in the temperature sensing range; 0 °C in the proposed structure. The obtained maximum N_{O} is 8-bit binary number and thus 8 bits is used for the N-register, DN-counter, and BTC. Thus, n and k are determined to 8 and 10 respectively.

To implement variable delay cells in the VRO, a lattice delay unit is used [26], as shown in Fig. 3. The output node of the last NAND gate is tied to the input node of the first NAND gate, and thus, the NAND gate delay line operates as a ring oscillator during the high pulse width of the start signal. One delay cell is made up of four NAND gates, including one dummy NAND gate. The dummy NAND gate is used to maintain the fan-out of each NAND gate. For the n-bit N-register, the number of variable delay cells in a NAND gate delay line is 2^n, and delay cells are sequentially activated by a 2^n-bit thermometer code (*VRO_con*[2^n-1:0]). If *VRO_con*[2^n-1:0] is all-low (all-high), all delay cells are

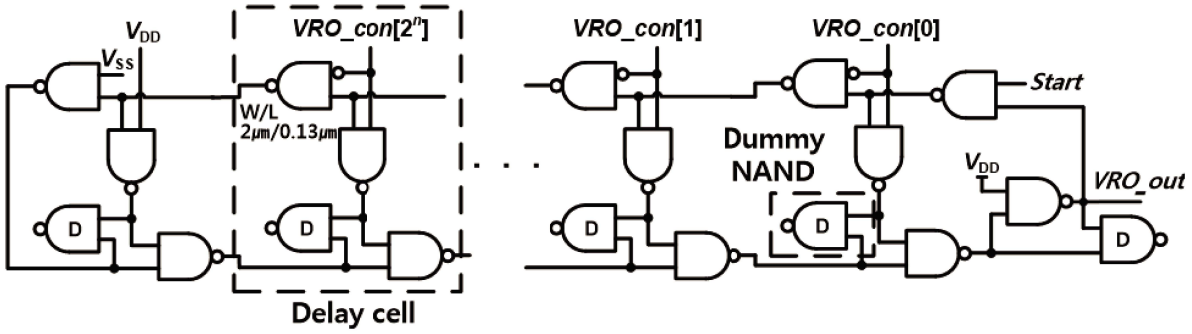

Fig. 3. The structure of the VRO.

deactivated (activated) and the shortest (longest) $PW_{\mathrm{VRO\_out}}$ is generated. The width of 2μm and the length of 0.13μm are used for the PMOS and NMOS in the NAND gates used in VRO. As mentioned above, the large N_{C} and N_{O} is preferred to achieve a high sensing accuracy. In addition, from (3) and (4), smaller delay of the NAND gates enlarges N_{C} and N_{O} and thus can help to improve the sensing accuracy. However, the delay of the NAND gates cannot be reduced much by increasing the size of NAND gates. The delay of the NAND gates rather depends on the process technology. Therefore, the size of the NAND gates is determined as the maximally possible width within the cell-pitch. The additional finger is not used to increase the size of NAND gates because it does not improve the gate delay much but causes area overhead and large power consumption.

The ripple carry counter is used to convert $PW_{\mathrm{VRO\_out}}$ into *Temp_code*[k-1:0]. The conversion is performed according to the counter clock (CLK_{CNT}), which is the external clock signal, when $PW_{\mathrm{VRO\_out}}$ is high. *Temp_code*[k-1:0] is stored in the T-register at the falling edge of $PW_{\mathrm{VRO\_out}}$. When the delayed $PW_{\mathrm{VRO\_out}}$ becomes low, the counter resets all bits of *Temp_code*[k-1:0] to zero in preparation for the next temperature sensing.

The T- and R-registers, which consist of k-bit D-flip-flops, store *Temp_code*[k-1:0] and *Ref_code*[k-1:0], respectively. The stored k-bits are transmitted to the comparator when the delayed $PW_{\mathrm{VRO\_out}}$ toggles the T-register. The N-register consists of n-bit D-flip-flops and stores *Bin_code*[n-1:0] in order to calculate the temperature.

The comparator compares *Temp_code*[k-1:0] with *Ref_code*[k-1:0]. Because the comparator simply determines whether *Temp_code*[k-1:0] and *Ref_code*[k-1:0] are all of the same value, the comparison is performed as soon as the delayed $PW_{\mathrm{VRO\_out}}$ arrives at the comparator. The comparison result (*Comp_out*) controls the BTC. If *Temp_code*[k-1:0] is not the same as *Ref_code*[k-1:0], the comparator generates a high-pulse *Comp_out* to activate the BTC with the DN-counter. Otherwise, the comparator generates a low-pulse *Comp_out* to deactivate the BTC with the DN-counter.

The BTC converts *Bin_code*[n-1:0] of the binary code to *VRO_con*[2^n-1:0] of the thermometer code to adjust the number of activated delay cells in the VRO [27]. For example, if *Bin_code*[2:0] is "011," the BTC converts it to a *VRO_con*[7:0] of "0000 0111." Initially, *Bin_code*[n-1:0] is set all-high at the DN counter. When *Comp_out* is high, the DN counter decreases *Bin_code*[n-1:0]. After the DN counter stops decreasing when *Comp_out* is low, *Bin_code*[n-1:0] is stored in the N-register and the BTC converts it to *VRO_con*[2^n-1:0].

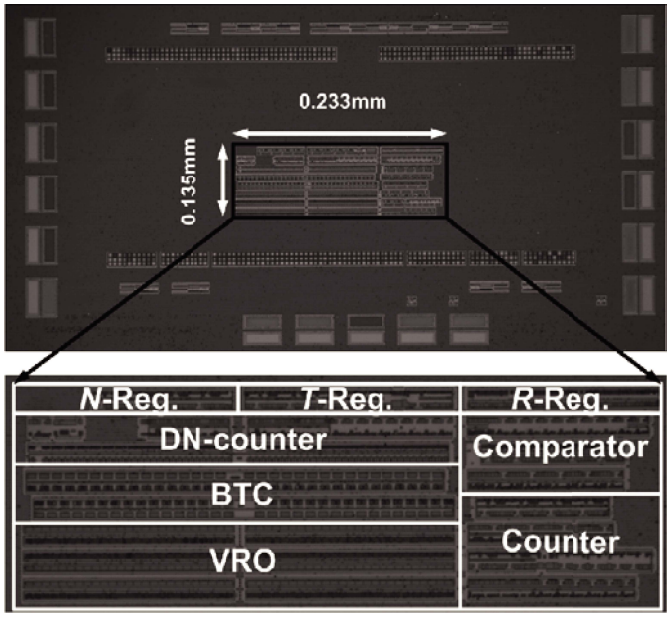

Fig. 4. Microphotography of the proposed temperature chip.

IV. Measurement Results and Comparisons

The proposed temperature sensor was fabricated using the 0.13-μm CMOS process technology. The microphotography of the chip is shown in Fig. 4. The proposed temperature sensor occupies an active area of 0.031 mm^2. All measurements were performed at 20 to 120 °C, with 1.2 V supply voltage. The temperature environment for the measurement was provided by a forced convection drying oven, JISICO J-300M.

The resolution was measured to be 0.595 °C/bit. Fig. 5 shows that the sensing error ranged from -0.63 to $+1.04$ °C, with a second-order master curve fitting for curvature correction. The measured energy per conversion was 0.67 nJ/conversion. The conversion rate of 430 kHz is closely related to the frequency of *VRO_out*.

The Time-domain based temperature sensors are weak for power supply variation because the delay of the delay cell is

TABLE I
PERFORMANCE COMPARISON OF RECENT TIME-DOMAIN TEMPERATURE SENSORS WITH ONE-POINT CALIBRATION

Paper	Temp. Range (°C)	Sensing Error (°C)	Conversion Rate (Hz)	Resolution (°C/bit)	Area (mm^2)	Technology (μm)	Energy (nJ/conversion)	Res. FoM* (nJ°C^2)	Acc. FoM* (nJ%^{2})
[20]	0~100	-4.0~4.0	5k	0.78	0.12	0.13	240	146.02	15360
[21]	0~60	-5.1~3.4	10k	0.139	0.01	0.065	15	0.29	3010.42
[22]	-40~100	-2.7~2.9	366k	0.043	0.0066	0.065	1.09	0.002	17.44
[23]	0~100	-0.7~0.6	4.4k	0.133	FPGA	FPGA	175	3.10	295.75
This work	20~120	-0.63~1.04	430k	0.595	0.031	0.13	0.67	0.24	1.87

*Res.FoM and Acc. FoM is an abbreviation for 'Resolution Figure of Merit' and 'Accuracy Figure of Merit'
Res.FoM = Energy×(Resolution)^2, Acc.FoM = Energy×(Relative error)^2
Relative error(%) = Maximum sensing error/Temp. Range

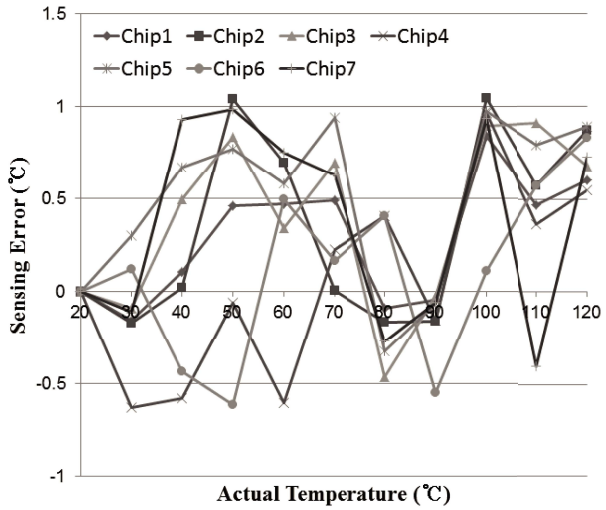

Fig. 5. Sensing error of seven chips.

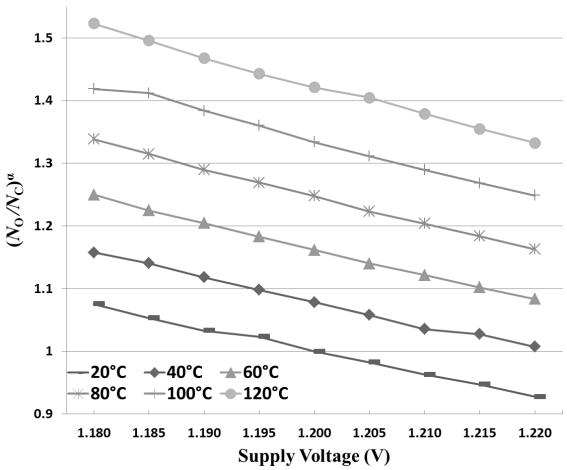

Fig. 6. Simulation result of the ratio of NO and NC with supply voltage variation from 1.18 V to 1.22 V after calibration operation.

largely affected by supply voltage variation [21]. The proposed temperature sensor also has the same problem. To check the supply sensitivity of the proposed temperature sensor, the ratio of N_C and N_O in (5) is simulated for various temperature and supply voltage. Because the acceptable supply voltage variation of the state-of-art microprocessor is ±19 mV [28], [29], the supply sensitivity within VDD ± 20 mV is simulated. The supply sensitivity of the proposed structure based on the simulation result in Fig. 6 is 0.43 °C/mV. The supply sensitivity is quite large when compared to that of the voltage-domain temperature sensors [15]. But the sensing error due to the supply voltage variation can be suppressed by adopting voltage regulator to the supply voltage of VRO [21].

Table I compares the performance of the proposed temperature sensor with recently published temperature sensors that have adopted one-point calibration. The measurement results show that the proposed temperature sensor achieves a low sensing error, small area, low energy per conversion, and high-speed conversion rate as compared with previous sensors. In particular, it significantly reduces the sensing error, area, and energy consumption by eliminating the reference generator and the code matching procedure using the comparator and the counter. Furthermore, for proper comparison, the resolution FoM and the accuracy FoM in [30] are calculated. The proposed temperature sensor achieves a resolution FoM of 0.24 nJ°C^2 and an accuracy FoM of 1.87 nJ%^{2}. Because the proposed temperature sensor has a lower resolution of 0.595 °C/bit than the compared temperature sensors, the proposed structure does not have the best resolution FoM. Nevertheless the achieved resolution FoM of the proposed temperature sensor is close to that of the state-of-art temperature sensors [30] because of the largely enhanced energy efficiency. In addition, the best accuracy FoM is achieved by the virtue of the small sensing error and energy efficiency.

V. CONCLUSION

This paper proposed a time-domain temperature sensor for low-power on-chip thermal management. To achieve highly efficient energy consumption per conversion, the proposed temperature sensor uses the binary code difference between the measured code and an externally applied code, rather than a reference generator. The code matching procedure acts to cancel the effect of process variation, and the comparison operation provides a high conversion rate. In addition, to reduce the cost of mass production by reducing the calibration effort, our system utilizes one-point calibration. The proposed

temperature sensor was fabricated using the 0.13-μm CMOS technology and achieves the low sensing error of -0.63 to $+1.04$ °C using one-point calibration with second-order master curve fitting over the temperature range of 20 to 120 °C. It has a small area of 0.031 mm^2, a low energy consumption of 0.67 nJ/conversion, and a high conversation rate of 430 kHz. Therefore, the proposed temperature sensor represents an advance in on-chip thermal management.

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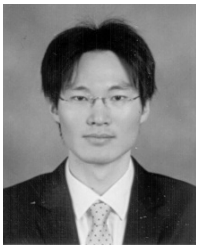

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