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Numerical study on thermal impacts of different void patterns on performance of chip-scale packaged power device

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ABSTRACT

Chip scale package (CSP) technology offers promising solutions to package power device due to its relatively good thermal performance among other factors. Solder thermal interface materials (STIMs) are often employed at the die bond layer of a chip-scale packaged power device to enhance heat transfer from the chip to the heat spreader. Nonetheless, the presence of voids in the solder die-attach layer impedes heat flow and could lead to an increase in the peak temperature of the chip. Such voids which form easily in the solder joint during reflow soldering process at manufacturing stage are primarily occasioned by out-gassing phenomenon and defective metallisation. Apparently, the thermal consequences of voids have been extensively studied, but not much information exist on precise effects of different patterns of solder die-attach voids on the thermal performance of chip-level packaged power device. In this study, three-dimensional finite element analysis (FEA) is employed to investigate such effects. Numerical studies were carried out to characterise the thermal impacts of various voids configurations, voids depth and voids location on package thermal resistance and chip junction temperature. The results show that for equivalent voiding percentage, thermal resistance increases more for large coalesced void type in comparison to the small distributed voids configuration. In addition, the study suggests that void extending through the entire thickness of solder layer and voids formed very close to the heat generating area of the chip can significantly increase package thermal resistance and chip junction temperature. The findings of this study indicate that void configurations, void depth and void location are vital parameters in evaluating the thermal effects of voids.

1. Introduction

The continuing trends on miniaturization of microelectronic packages coupled with the need to maximise their thermal performance require innovative package designs for power devices and modules. State-of-the-art integrated circuit (IC) packaging techniques such as chip scale packaging (CSP) technology [1–5] offer promising solution for packaging power electronics. This is as a result of the technology's inherent size advantage and relatively improved thermal and electrical performance [1]. Indeed, there has been continuous progress in applying CSP to power electronics in recent years; among them are the MOSFET (metal oxide semiconductor field effect transistor) BGA packages from Fairchild Semiconductor [6,7], FlipFET package from International Rectifier [8] and flip chip packages for power chips used in the IPEMs from centre for power electronics systems (CPES) [1].

In flip-chip CSP technology (Fig. 1), whilst the active side of the silicon device is mounted onto a substrate, which can be attached to a printed circuit board (PCB) via ball grid array (BGA) solder interconnections, heat removal from the device is primarily through the backside of the silicon die (chip). Heat dissipating units such as the heat spreader and/or heat sink are usually attached to the backside of heat generating silicon die in an effort to improve the surface area available for heat dissipation. The bonding of the heat spreader/sink to the heat generating silicon die is often done using thermal interface materials (TIMs) in order to improve contact between the mating surfaces and thermal transfer across the interface by suppressing interstitial air-filled gaps [9]. Therefore, the efficiency of heat transfer through TIMs is critical in flip-chip CSP technology. Solder thermal interface materials (STIMs) are preferred to their polymer-based counterparts because they offer higher thermal conductivities [10–13].

Nevertheless, voiding remains one of the major reliability concerns in the use of solder as TIMs [14]. The use of lead(Pb)-free solders has even escalated concerns emanating from solder voids due to its comparatively poor solderability [15] as studies have reported the occurrence of voids in excess of 50% of solder joint volume in some Pb-free solders [16,17]. Voids reduce the effective solder cross-section area available for heat transfer [18] and subsequently result in an increase in thermal resistance and chip peak temperature which can lead to temperature activated failure

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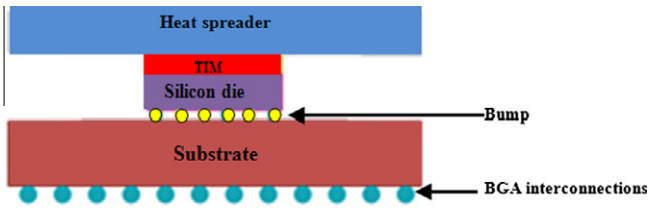

Fig. 1. Schematic of flip-chip CSP configuration.

mechanisms. Unfortunately, voids formation are almost inevitable in solder joints during manufacturing mainly due to the following circumstances which are too complicated to control [19,20]:

- The entrapment of gas bubbles formed by reactions among materials and fluxes during the reflow soldering process.
- Poor wetting of solder due to defective or contaminated backside metallisation of the silicon die or heat spreader/sink.

Voids can also occur or degrade during device operation as a result of solder-alloy fatigue due to cyclic thermo-mechanical stresses [15,16]. Owing to the different aspects of solder voids, they can be classified into groups or types. For example [21],

- From the solder wetting point of view, there could be shallow voids (partially wetted) and deep voids (completely non-wetted voids).
- Based on void configuration, the formation of distributed small voids and large single coalesced voids is feasible.
- As regards void location, voids can form at the corner/edge or centre of the STIM layer.

These various void types could have different level of impact on the thermal performance of an electronic package and thus, the evaluation of the precise thermal effects of these different void patterns is essential. It should be noted that numerous studies on the impacts of voids on thermal performance of various electronic packages have been carried out by other researchers. For instance, Chang et al. [15] investigated the effect of solder void size and location on thermal resistance of power devices using three dimensional (3-D) finite element modeling. Their result suggested an increase in chip temperature and thermal resistance with the increase in void percentages. Thermal resistance increased to 6.53% and 27.18% when the void percentages were 20% and 79%, respectively. Fleischer et al. [22] used experimental and numerical methods to predict the relationship between void geometry and package thermal resistance. Package thermal resistance was observed to increase as void percentage rises. Thermal resistance increased to 30% with 73% voiding for random voids. This was in contrast with contiguous voids, with package thermal resistance increase of up to 200% for 73% voiding. Biswal et al. [23] employed finite element analysis (FEA) to assess the impact of solder voids on the overall heat conduction of a high power module. It was found that solder voids of relatively large radii impede heat conduction process to a great extent than distributed voids. Zhu [21] used FEA to study thermal impact of voids on a power device. The results showed that large, coalesced and/or edge voids have greater impact on the thermal resistance of the device than small, distributed voids. It was also suggested that the temperature in the chip is much more sensitive to a void extending across the chip width than a void along the chip length.

Although the aforementioned studies provide vital information on the relationship between package thermal performances and voids in the STIM layer, more studies are needed for an in-depth understanding of the precise contribution of different patterns of lead-free solder voids to package thermal behaviour. The purpose of the present study is to apply FEA to a systematic investigation of the effects of different numerically controlled Pb-free solder void patterns on the thermal performance of chip-level packaged power device. The solder void patterns under investigation include distributed small voids and large single coalesced voids; shallow voids and deep voids; corner/edge voids and centre voids. Thermal characterisation of the impacts of these voids is crucial in assessing the role of different void patterns in package thermal performance and improving the overall reliability of semiconductor power devices.

2. Thermal implications of voids

The heat generated by the power dissipated above the void has to flow laterally around the void and hence obstruct thermal flow as shown in Fig. 2. This impediment in heat flow could result in overheating or other temperature activated failure mechanisms. A practical example of voids induced failure case is shown in Fig. 3; the occurrence of voids in the STIM have resulted in high thermal resistance and subsequent melting of gold (Au) bonding wires found in another piece of our experimental works.

The rate of conductive heat transfer through a solder joint based on Fourier's law is given as:

$$Q = -kA\frac{dT}{dx} = kA\frac{T_1 - T_2}{L} \tag{1}$$

where Q is the heat transferred; k is the thermal conductivity; A is the cross sectional area of the solder joint; dT/dx is the temperature gradient; L is the thickness of the solder; and $T_1 - T_2$ is the temperature difference. It can be inferred from Eq. (1) that the heat transferred is directly proportional to the cross sectional area of the solder layer. Defining resistance as the ratio of a driving potential to the corresponding transfer rate, it follows from Eq. (1) that the heat spreading resistance for conduction in the solder joint can be expressed as:

$$\theta = \frac{T_1 - T_2}{Q} = \frac{L}{kA} \tag{2}$$

As a result of voids detrimental impact on heat conduction, process conditions are usually controlled carefully during manufacturing stage in order to keep void percentage at an acceptable level. This acceptable level is defined by the impact of voids on critical thermal parameters of an electronic package. A convenient parameter used in characterising and comparing the thermal effects of different cases of solder voids investigated in this paper is referred to as $\theta - JC$ (thermal resistance), defined as the ratio of the device temperature increase over ambient to the average power dissipated in the device [24] (which is a measure of the ability of a package to dissipate heat via conduction from the surface of the die to the heat spreader surface) [25,26]. This is expressed as:

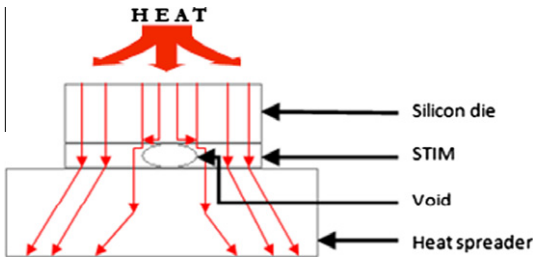

Fig. 2. Schematic of heat flow with void present in the die attach.

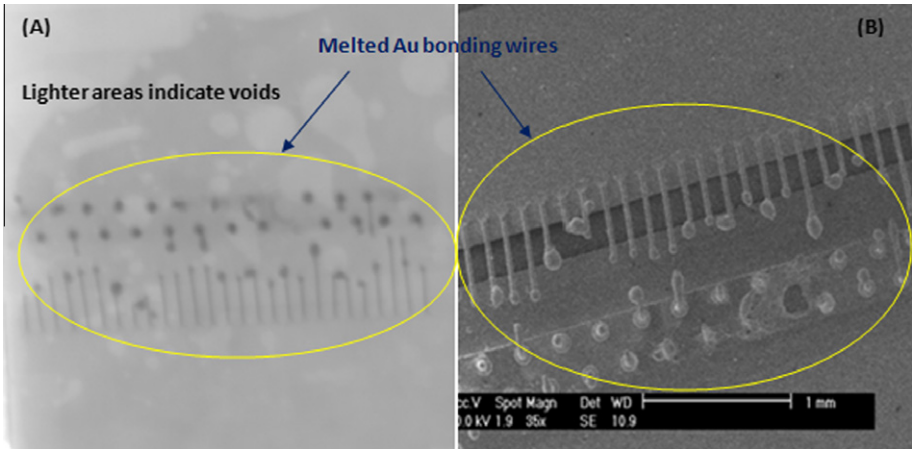

Fig. 3. Images of melted Au bonding wires due to overheating caused by voids in the STIM layer (A) X-ray image (B) SEM image.

$$\theta - JC = \frac{T_{max} - T_{min}}{P} \quad (3)$$

where T_{max} is the maximum temperature at the chip junction; T_{min} is the minimum temperature at the top surface of the heat spreader; P is the power dissipation of the silicon chip. θ – JC is an important thermal design parameter which can be used to determine the maximum allowable power or the chip peak temperature under a given power for infinite heat sink [27].

3. Finite element modeling of the thermal effects of voids

3.1. Thermal model

The thermal models (shown in Fig. 4A and B for packages with and without heat spreader respectively) were created in ANSYS 13.0. Table 1 specifies the properties and dimensions of the different components of the models. The heat (1 W) generating area (active area) is applied as a heat flux on the top surface of the silicon chip. The mesh consists of 1287,365 nodes and 438,204 elements. Temperature distributions around the package with and without heat spreader in natural convection (stagnant air) are shown in Fig. 5A and B, respectively. The maximum temperature was attained at the centre of the chip where the heat source is located. The thermal resistance and chip junction temperature were found to be about three times higher in the package without a heat spreader compared to the package with heat spreader. It is apparent that improved thermal performance could be achieved through coupling a heat spreader to the backside of the die using a TIM [28]. This is because of the relatively lower thermal conductivity through the front-side intermediate layers of the package particularly the organic substrate and also limited number of solder bumps that make only a small fraction of contact area. A more detailed work on the contribution of the solder balls under the chip (chip front-side) to heat dissipation has been reported in Ref. [3]. Hence, the present work considers only the backside of the package with heat spreader (shown in Fig. 6) as the representative improved heat removal path under investigation. The focus is on effects of die attach voids on thermal performance of the package.

3.1.1. Local modeling of voided solder die attach

The local (simplified) model consists of a silicon die of the packaged semiconductor power device mounted upon a stack of

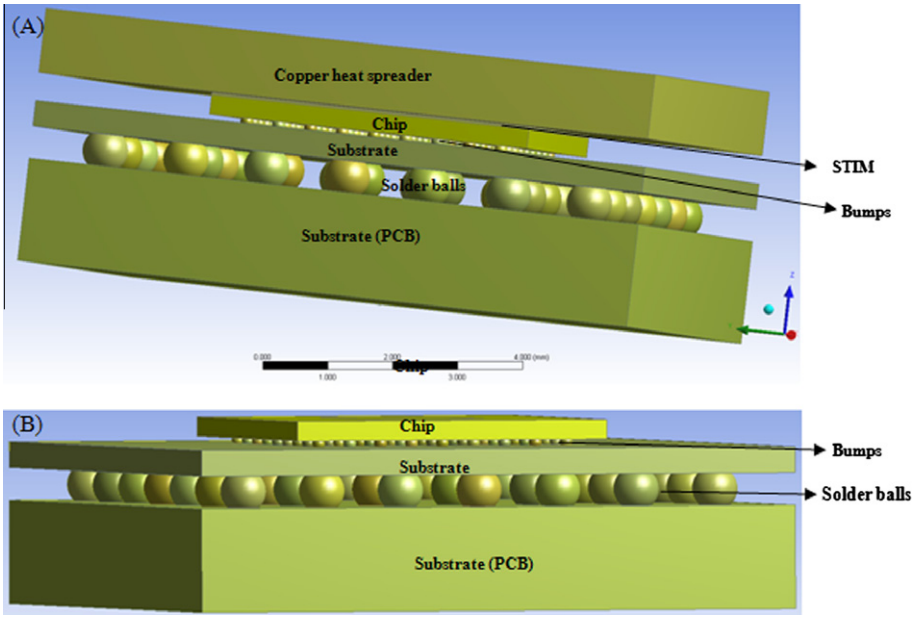

Fig. 4. Model structure for package (A) with heat spreader (B) without heat spreader.

Table 1
Dimensions and properties of models in Fig. 4.

Parameter	Chip	Solder (Sn3.0Ag0.5Cu)	Copper heat spreader	Bumps	Substrate	Solder balls	PCB
Length (mm)	5	5	9.59	–	9.59	–	9.59
Width (mm)	5	5	9.59	–	9.59	–	9.59
Thickness (mm)	0.3	0.04	1	–	0.4	–	1.6
Radius (mm)	–	–	–	0.05	–	0.33	–
Pitch (mm)	–	–	–	0.5	–	1.27	–
Standoff (mm)	–	–	–	0.1	–		–
Conductivity (W/mK)	120	50[a]	386	50[a]	0.3	50[a]	0.3

[a] Ref. [15].

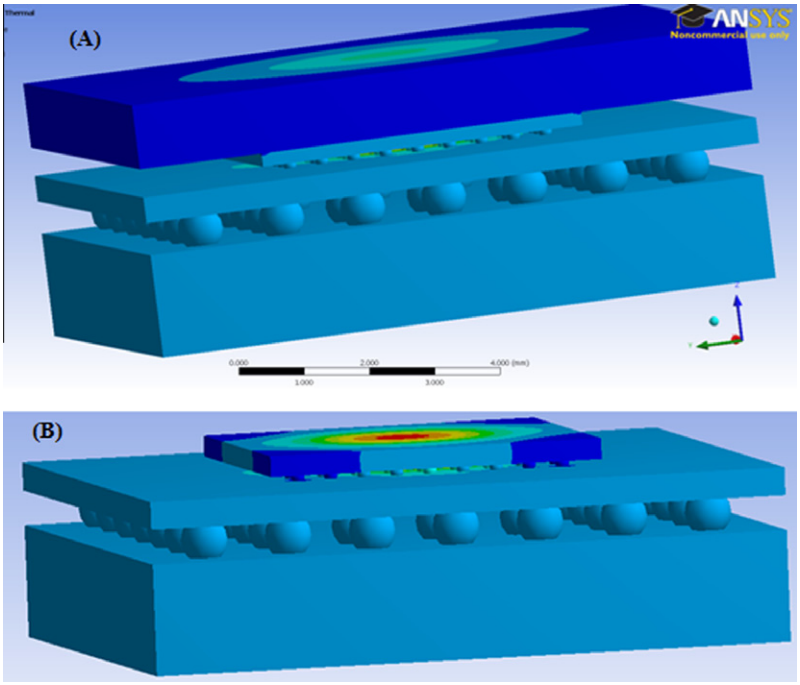

Fig. 5. Temperature distribution for package (A) with heat spreader (B) without heat spreader.

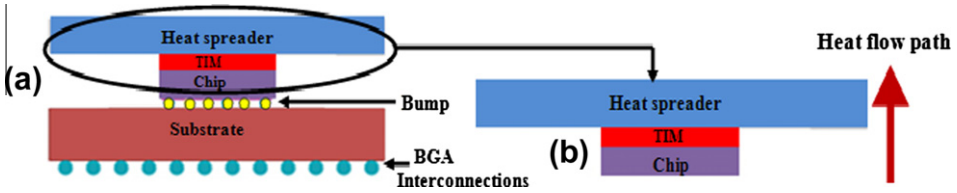

Fig. 6. Schematic of (a) full flip-chip CSP configuration (b) representative heat dissipation path (considered in the simulation).

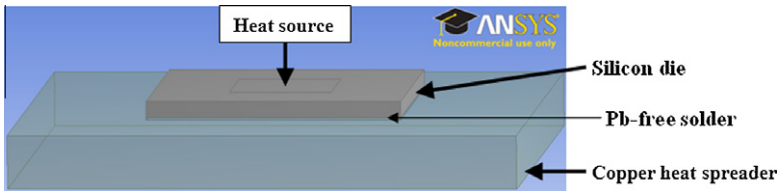

Fig. 7. Simplified model structure.

supporting layers of STIM and copper heat spreader (IHS) as depicted in Fig. 7. The properties and dimensions of the different components of the simplified model are listed in Table 2.

A geometric model without solder void, serving as control, was first developed and then modified by introducing large coalesced void and small distributed voids accordingly. Large coalesced void

Table 2
Properties and dimensions of package assembly constituents.

Parameter	Silicon die	Solder (Sn3.0Ag0.5Cu)	Copper heat spreader	Void
Length (mm)	5	5	10	–
Width (mm)	5	5	10	–
Thickness (mm)	0.3	0.04	1	–
Radius (mm)	–	–	–	Varies as in Table 2.
Conductivity (W/mK)	120	50[a]	386	0.0261

[a] Ref. [15].

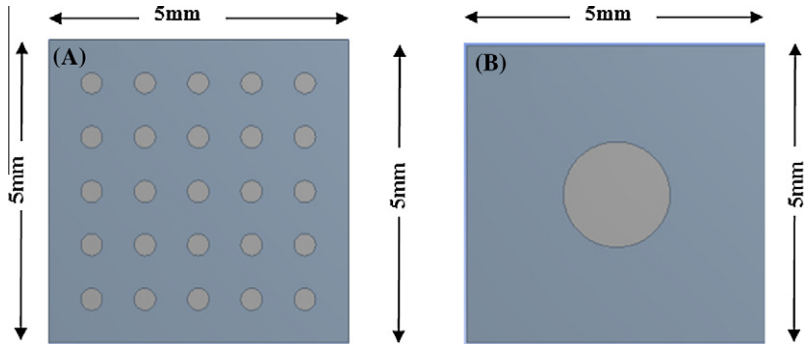

Fig. 8. Examples of void configuration for 10% void area concentration with (A) showing evenly distributed small voids and (B) showing large single void.

takes the form of a single, large centrally located, circular void while small distributed voids are modeled as evenly spaced circular voids with equivalent total void area as the large coalesced void. The voiding area was calculated in such a way that one single coalesced circular void would be equivalent to 25 small evenly distributed circular voids as delineated in Fig. 8 for 10% void area concentration. The complete void configurations are shown in Table 3.

Considering that the MIL-STD-883D, method 2030 [29], for the ultrasonic inspection of die attach requires that the overall solder void area should not exceed 50% of the total joint area, the void area percentages (total area of voids/foot print of solder) 5%, 10%, 20%, 30%, 40%, 50% are chosen as levels of interests, and a 75% void selected as a worst case reference for this study.

3.1.2. Boundary conditions

Overall boundary conditions for the simplified model like the global model include a uniform heat flux Q (W/mm^2) at the top centre surface of the die. The heat (1 W) generating area (active area) is applied as a heat flux on the top surface of the silicon chip. A fixed temperature (25 °C) is applied at the backside of the copper heat spreader, representing an infinite heat sink. The other surfaces are assumed to be adiabatic, i.e. no heat transfer by convection or radiation is considered. The heat is dissipated from the chip primarily by conduction through the supporting layers. Thus, only conduction mode of heat transfer is considered for all the void cases (models) investigated in this paper.

The FEA program (ANSYS) subdivides the assembly into finite elements (mesh) as shown in Fig. 9. The mesh consists of 606,219 nodes and 120,564 elements, the results are checked for mesh independence by comparison to models with 355,971 nodes and 2909,666 nodes. Only ½ geometric symmetry of the assembly is used in the analysis to reduce computational time and storage space.

4. Results and discussions

The voids are firstly modeled as vacuum with no material property and then with the material property of air (0.0261 W/mK thermal conductivity). There was no significant variation noticed in the results obtained from the two different approaches. Thus, in order to reduce computational time, all cases of void models considered in this study are modeled as vacuum unless otherwise stated. It is important to know that even though the values obtained through the approach employed in this study can be used to predict and compare thermal response of a package due to the effects of different solder die-attach void patterns; they may not represent real quantitative values of thermal resistances due to the limitations of the approach. Factors, such as defects of materials, thermal contact/interfacial resistances and non-linearity in the materials including solder voids are not considered in the modeling. These factors are traded off for an in-depth comprehension of the impacts of different numerically controlled solder die-attach void patterns on package thermal performance. In line with the method the simulations were carried out, this section will be presented in four parts:

4.1. Effect of heat generating source area on thermal resistance values

Considering that the active (heat source) area in a chip is often smaller than the total chip area, the influence of the heat (1 W) generating area on thermal resistance is examined by varying the active area in the chip from 10% to 100% for the two different void configurations (10% large and distributed voids area). The results are shown in Fig. 10. It is clear from the results that $\theta - JC$ decrease as the heat generating area increases. At each heat generating area, $\theta - JC$ is higher for large coalesced void configuration than distributed voids. As the heat generating area increases from 10% to 100%, $\theta - JC$ variation for the distributed voids configuration is 338% which is higher than the 284% observed for large coalesced void configuration. Thus, this study suggests that $\theta - JC$ values may strongly depend on the heat (power) generating area of the chip. It is of immense consequence to thermal engineers creating accurate thermal models to understand that the effect of the chip power on thermal resistance depends on the area of the chip generating the power. Considering that the heat generating area of the chip is much smaller than the total chip area in reality, a fixed heat generating area of 2 mm × 2 mm (40%) at the top centre surface of the chip as shown in Fig. 7 is employed as a level of interest for

Table 3
Large and distributed void configurations.

Model	Configuration type	Void radius[a] (mm)	Number of voids	Void area[b] (mm^2)	Percentage of void area (V%)
	No void	0	0	0	0
	Large	0.631	1	1.25	5
	Distributed	0.126	25	1.25	5
	Large	0.892	1	2.49	10
	Distributed	0.178	25	2.49	10
	Large	1.261	1	4.99	20
	Distributed	0.252	25	4.99	20
	Large	1.544	1	7.49	30
	Distributed	0.309	25	7.49	30
	Large	1.784	1	10.00	40
	Distributed	0.357	25	10.00	40
	Large	1.995	1	12.50	50
	Distributed	0.399	25	12.50	50
	Large	2.442	1	18.74	75
	Distributed	0.488	25	18.74	75

[a] Approximated to three decimal places, the voids radii were calculated using formula: $r^2 = \left(\frac{R}{5}\right)^2$, where r is the radius of each of the small distributed voids; R is the radius of large single coalesced void.
[b] Approximated to two decimal places, voids areas were calculated using formula: $25(\pi r^2) = \pi R^2$.

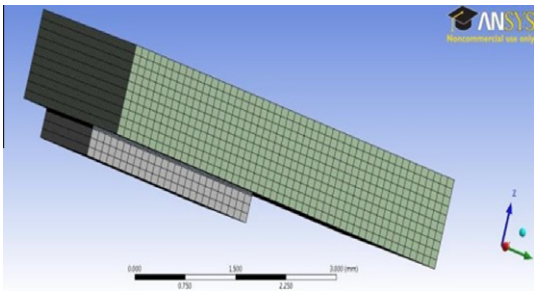

Fig. 9. An example of a meshed model.

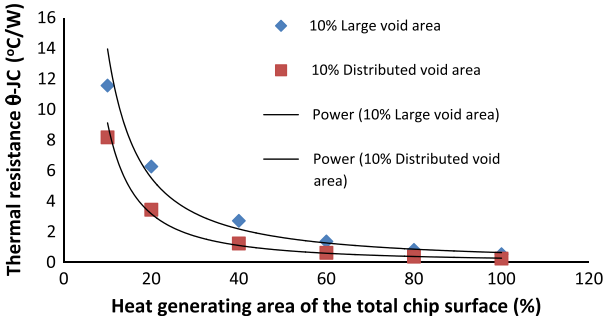

Fig. 10. Effect of heat generating area on $\theta - JC$.

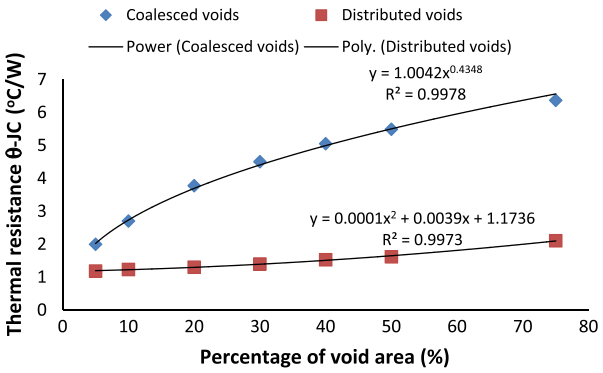

Fig. 11. Variation of $\theta - JC$ with different void configurations.

subsequent studies on effect of different void patterns on package thermal resistance.

4.2. Effect of void configurations – large vs. distributed

The voids are 0.04 mm deep in a 0.04 mm thick solder layer. The results as presented in Fig. 11 show that for both void configurations, $\theta - JC$ rises as void percentage increases. Furthermore, as illustrated in Figs. 12 and 13, the chip junction temperature also rises as $\theta - JC$ increase. The increase in chip junction temperature due to 75% large coalesced void configuration is 451.7%, which is more than the 74.6% observed for equivalent percentage (75%) of small distributed voids.

There is a distinct difference in the thermal impact of large and distributed voids as void percentage increases. The thermal resistance due to distributed void configurations ($\theta - JC_D$) increases to a maximum of 2.105 °C/W with 75% voids, and is well correlated with a polynomial fit: $\theta - JC_D = 0.0001V^2 + 0.0039\,V + 1.1736$. As regards large void pattern, equivalent void percentage to that of distributed voids results in a much higher increase in thermal resistance ($\theta - JC_L$) of 6.367 °C/W for 75% voiding. This is well correlated with a power fit: $\theta - JC_L = 1.0042V^{0.4348}$. The results suggest that:

- $\theta - JC$ increases as void percentage increases.
- Void configuration has a significant impact on the thermal performance of a package.
- Large single void can greatly increase the thermal resistance of a package compared to distributed voids of equivalent void percentage.

More attention should therefore be given to large coalesced voids when setting criteria for solder die-attach inspection. The difference in the thermal spreading resistance behaviour of large coalesced and small distributed void configurations can be qualitatively explained through the effects of heat flow. Three-dimensional heat spreading comprises of both vertical flow and lateral flow [30]. Therefore, there could be vertical heat flow resistance from the heat generating source above the void, and a lateral heat flow resistance from the region above the void to the surrounding non-voided areas [22]. Void in solder die attach area results in a thermal spreading resistance as heat is forced to flow laterally around the void region. Additionally, heat flow in the vertical direction is restricted by the high thermal resistance through the void itself. For the same void percentage, lateral heat flow resistance is higher for large coalesced void configurations since heat flows laterally for a much shorter distance for the small distributed voids. Thus, large coalesced voids result in a much more increase in the overall thermal resistance.

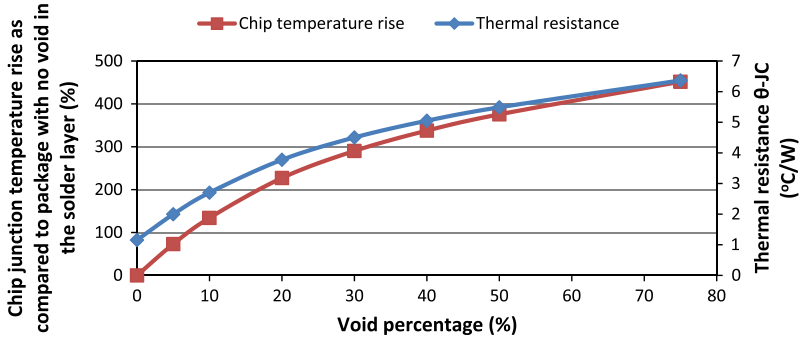

Fig. 12. Thermal performance due to large voids.

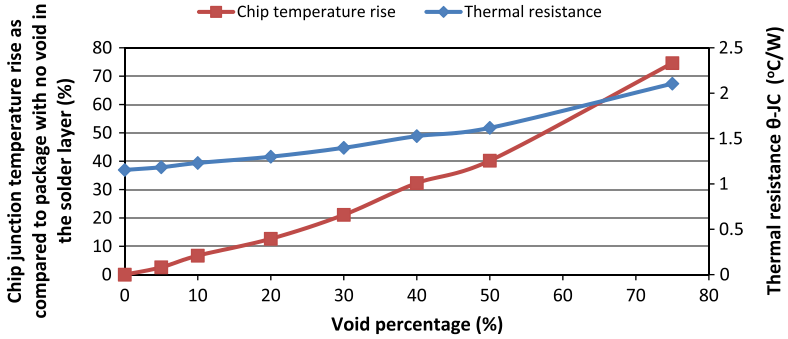

Fig. 13. Thermal behaviour due to distributed voids.

4.2.1. Comparison with available experimental data

Experimental work on void configuration is scarcely available in literature; this could be as a result of the complexities and interactions associated with the many factors that affect void formation during manufacturing and operating stages [31]. Hence, practically controlling exact void configurations in a solder layer of about 0.04 mm thickness would be too complicated. No wonder, finite element thermal analysis is often employed to isolate and characterise the precise effects of the different void configurations as even a mixture of these voids can form in one given solder joint in reality. To the authors' knowledge, the only previous experimental work which allows the exact control of void configuration is that of Fleischer et al. [22]. They studied the effect of large void and distributed void experimentally by precisely etching square void patterns directly onto the backside of the chip. They also carried out a numerical study to show that the thermal effect of voids located in the chip backside is equivalent to voids located in the die bond layer. Their results as depicted in Fig. 14 showed that large contiguous void results in a much higher thermal resistance compared to small distributed voids of equivalent voiding percentage. This validates the finding of this study which suggests that small distributed voids account for less thermal resistance compared to large coalesced void of the same voiding percentage. Nonetheless, considering that in reality, solder voids do not follow a regular square-like shape but appear to progress roundly/chaotically, this study employ a circular void approach precisely embedded in the solder die-attach layer. This approach is different from the square void patterns precisely etched onto the backside of the chip in Ref. [22]. The strong qualitative agreement in the results from the two different approaches suggests that void geometry may not have an effect on thermal resistance. The quantitative discrepancies between the simulation results reported in this paper and the experimental results in Ref. [22] are expected because the experimental parameters including the material properties of lead-based solder attach layer studied by Fleischer et al. were different from the parameters used in the present numerical study.

4.3. Effect of voids depth (shallow vs. deep voids)

Previous analysis suggests that large coalesced voids have more adverse impact on the thermal resistance of package than distributed voids for equivalent voiding percentage. Hence, large coalesced void was chosen for this study.

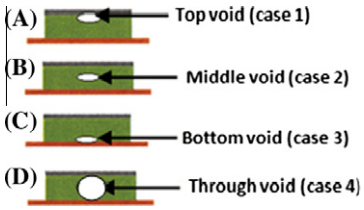

Fig. 15. Schematic showing (A–C) shallow void cases and (D) through void (not drawn to scale).

Shallow voids can be formed at different vertical positions in the solder layer. This is because voids can be encapsulated in the middle of solder layer due to entrapment of gas bubbles formed by flux and other reactants during reflow soldering process. Furthermore, there is a potential for voids to occur at the surface between the solder layer and metallised silicon die or heat spreader as a result of poor solder wetting due to defective backside metallisation or backside contamination during manufacturing. Hence, representative shallow voids are situated at different vertical positions in the solder layer as shown in Fig. 15A–C. Through void (Fig. 15D) can occur as a result of degradation of shallow voids during device service and also due to completely non-wetting of solder during manufacturing.

Four cases of voids depth were simulated; the cases are referred to as top voids (case 1), middle voids (case 2), bottom voids (case 3) and through voids (case 4). Top voids are 0.02 mm deep located centrally in the upper part of the solder layer (0.04 mm thick) next to the silicon die as illustrated in Fig. 15A. Middle voids are 0.02 mm deep located centrally in the middle of 0.04 mm thick solder layer as shown in Fig. 15B, leaving 0.01 mm thick of solder layer on top and below the voids. Bottom voids are 0.02 mm deep located centrally in the lower part of the solder layer (0.04 mm thick) next to the copper heat spreader as delineated in Fig 15C. Through voids are 0.04 mm deep in a solder layer of 0.04 mm thickness, creating a through solder void as shown in Fig. 15D. The solder void models used for this study are modeled by filling the void depths with material that has the thermal conductivity of air (0.0261 W/mK). Other dimensions including the void area percentages are as earlier listed in the thermal model section for large coalesced voids.

Fig. 16 shows $\theta - JC$ rises as the void percentage increases for the different void cases. The thermal performance predictions for

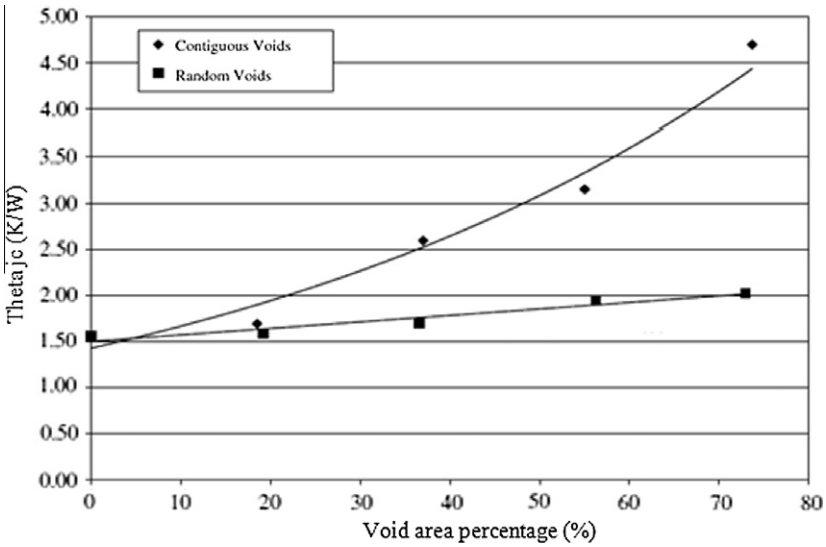

Fig. 14. Variation of thermal resistance with contiguous and distributed void percentage [22].

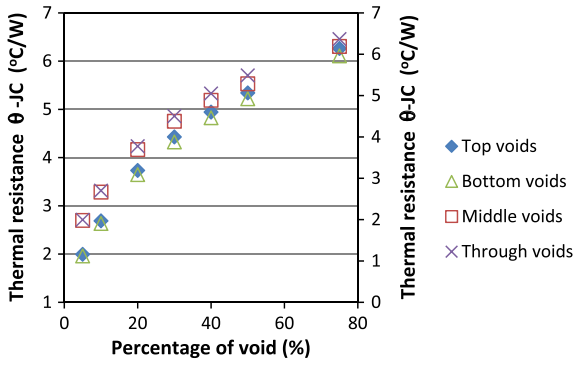

Fig. 16. $\theta - JC$ performance for the different void cases.

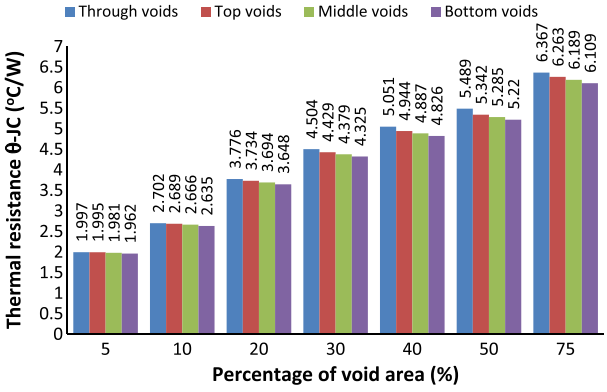

Fig. 17. Variations of $\theta - JC$ due to the different void cases.

the different void cases are observed to be similar as the result data for each case is correlated with a power fit. Fig. 17 depicts the comparison of thermal resistance due to the different void cases. Among the shallow void cases, top voids (closest to the heat source) relatively lead to the highest increase in $\theta - JC$. Furthermore, bottom voids (next to the heat spreader) which occur in solder layer surface further from the heat generating chip result in less values of $\theta - JC$ compared to the middle voids. The variations in $\theta - JC$ due to the different shallow void cases with the same thickness result from the vertical proximity of the voids to the heat generating source. With regards to the four void cases, as expected, thermal resistance is highest for through voids. A through void in the solder layer replaces a relatively much higher thermal conductivity solder region with an extremely low thermal conductivity void. Overall, there is no significant variation in $\theta - JC$ as a result of the four different void cases as $\theta - JC$ only varies between 1% and 5% as the voids percentages increase from 5% to 75%. Similar result trend as regards the void cases was reported by Chen et al. [27]. However, the work of Chen was limited to 10% void area. In this study, the influence of void depth/position on thermal resistance can be observed in detail from 5% to 75% void area, greatly extending the current state of knowledge. This detailed information particularly may be of assistance to thermal engineers especially with works [16,17] reporting the occurrence of voids in excess of 50% of solder joint volume in some Pb-free solders.

4.4. Effect of void location (corner voids vs. centre void)

MIL-STD-883D, method 2030 [28], for the ultrasonic inspection of die attach requires that a corner void should not be bigger than 10% of the total void area. Hence, 10% large coalesced void area was chosen for this study as a level of interest. Furthermore, through

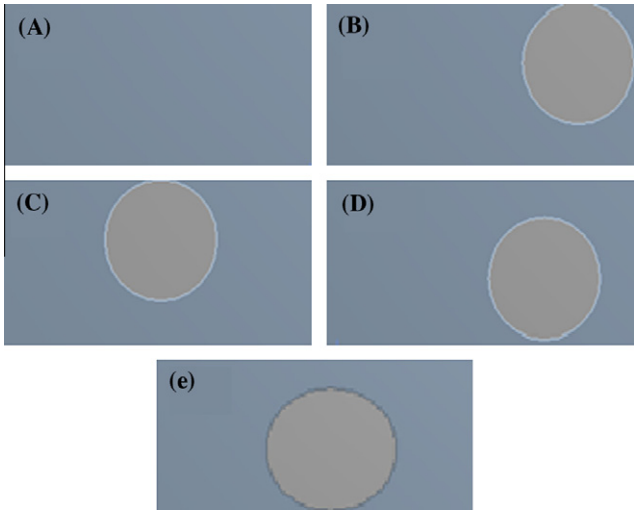

Fig. 18. (A) shows solder layer without void (B) shows void location A (C) shows void location B (D) shows void location C. (E) shows void location D (not drawn to scale).

voids were used for this investigation because they account for more profound effect on $\theta - JC$ compared to shallow voids as evident from the previous finding.

While the heat source is kept constant as shown in Fig. 7, 10% void was arbitrary located at different proximities (void location A–C) to the heat generating source as depicted in Fig. 18B–D representing corner voids. Additionally, 10% void area was positioned near the centre of the heat generating chip (Fig. 18E) representing centre void (void location D). A depiction of solder layer without void is presented in Fig. 18A to serve as a reference. The solder voids are 0.04 mm deep in a solder layer of 0.04 mm thickness. Other dimensions and properties remained as previously listed in the thermal model section. While the heat distribution effects of the four different void locations are as shown in Fig. 19B–E, Fig. 19A delineates the temperature contour at the back surface of the chip when there is no void in the solder layer as a reference.

Visual inspection of the temperature contour at the back surface of the silicon die reveals that voids significantly impede thermal path as delineated in Fig. 19B–E with reference to Fig. 19A. A strong upshot of void location on die back surface temperature is evident. One can easily differentiate the void location as it is qualitatively reproduced on the back surface temperature contour of the chip.

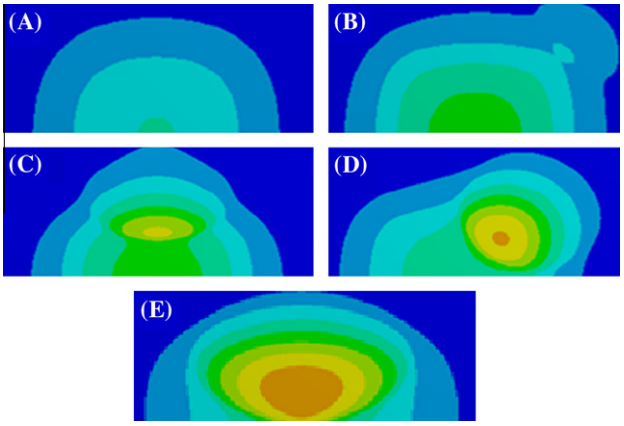

Fig. 19. Heat distribution effects on the back surface of the silicon chip (A) when there is no void (B) as a result of void location A (C) shows hot spot as a result of void location B (D) shows hot spot as a result of void location C (E) shows hot spot as a result of void location D (not drawn to scale).

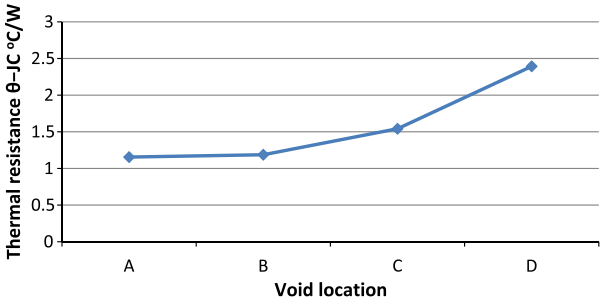

Fig. 20. Thermal effects of the four different void locations.

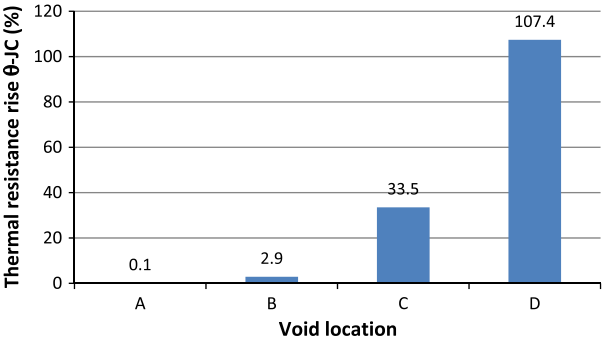

Fig. 21. Comparison of $\theta - JC$ rise due to the different void locations.

At different locations, the void location results in a progression of high temperature points around the void. The result data as presented in Fig. 20 shows that the closer the void is to the heat source, the higher the $\theta - JC$. This is comparable to the result in Ref. [14] where corner-void was accountable for a peak temperature less than that of centred void effect. $\theta - JC$ rise (Fig. 21) as compared to assembly with no void in the solder die attach layer is 0.1% when the void is furthest from the heat source (void location A), 2.9% when further (void location B) and 33.5% when the void is closer to the heat source (void location C). $\theta - JC$ significantly rises to 107.4% for centre void (void location D) positioned near the centre of the heat generating chip. The findings from the present study actually suggest that a void located at the edge of a solder layer may not result in hot spot (representing the hottest spot at the chip surface as suggested by the work of Fleischer et al. [22] and Biswal et al. [23]); this is because the active area in a real chip is smaller than the total chip area, and hence the void percentage under the un-active area does result in a relatively lower thermal resistance as evident from the less significant rise (0.1%) in $\theta - JC$ due to void location (A) (Fig. 19B).

5. Summary and findings

In this study, thermal simulations have been performed to characterise the thermal effects of different numerically controlled solder die attach void patterns on the performance of chip-level packaged power device. An analytical approach referred to as $\theta - JC$ (thermal resistance) was employed to understand and explain the findings. The following are findings of this study:

- $\theta - JC$ values are dependent on the heat generating area of the chip.
- Large single void has a more detrimental impact on $\theta - JC$ compared to small distributed voids of equivalent void percentage.
- Shallow voids formed in the solder die attach layer next to the surface of the heat generating chip result in a relatively higher $\theta - JC$ than equivalent shallow voids present at other vertical positions further from the heat generating chip. Nonetheless, through-thickness void (voids extending through the whole solder layer) in the same lateral position as the shallow voids is accountable for the highest $\theta - JC$ values.
- $\theta - JC$ is highest for voids present near the center of the heat source. A void at the edge (very far from the heat source) of the solder die attach layer may not result in hot spot (representing the hottest spot at the chip back surface).

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