Hybrid Temperature Sensor Network for Area-Efficient On-Chip Thermal Map Sensing

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***Abstract*—Spatial thermal distribution of a chip is an essential information for dynamic thermal management. To get a rich thermal map, the sensor area is required to be reduced radically. However, squeezing the sensor size is about to face its physical limitation. In this background, we propose an area-efficient thermal sensing technique: hybrid temperature sensor network. The proposed sensor architecture fully exploits the spatial low-pass filtering effect of thermal systems, which implies that most of the thermal information resides in very low spatial frequency region. Our on-chip sensor network consists of a small number of accurate thermal sensors and a large number of tiny relative thermal sensors, responsible for low and high spatial frequency thermal information respectively. By combining these sensor readouts, a thermal map upsampler synthesizes a higher spatial resolution thermal map with a proposed guided upsampling algorithm.**

***Index Terms*—Temperature sensors, microprocessors, area-efficient, collaborative sensing, spatial low-pass filtering effect.**

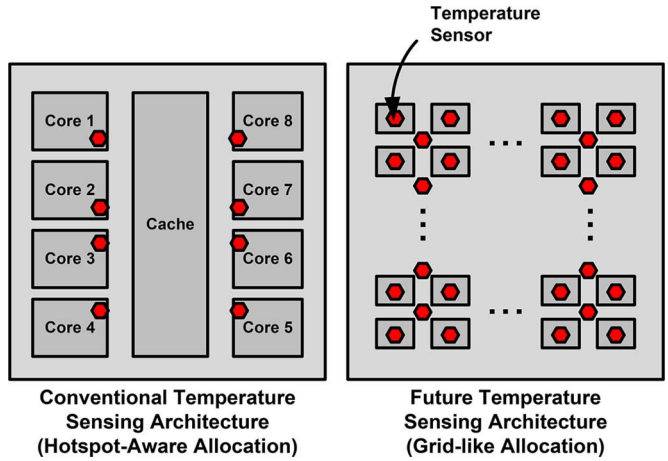

Fig. 1. Technical direction of on-chip temperature sensing architecture. The uncertainty of potential hotspot location requires more sensors with regular placement.

I. Introduction

THE exponential growth of transistor density has resulted in tremendous computing power. However, this evolution was slowed down since the processors have started to hit a 'thermal wall'. This trend is mainly caused by ever increasing power density and poor cooling environment. Compared to processors in the 1980s, the power density has dramatically increased by more than a factor of 32 and still counting [1]. Increasing power density leads to a thermal hazard which is further exacerbated due to the lack of sufficient heat dissipation path in mobile devices and die-stacking packages [2]. Therefore, the importance of dynamic thermal management (DTM) [3] cannot be overestimated.

Since a processor's maximum performance is limited to the hottest spot in die area, also known as the 'hotspot', DTM spreads the heat out over the entire die as much as possible. In legacy processors with small number of cores, DTM was relatively an easy task since the hotspot location could be estimated by off-line thermal analysis. However, the trend in many-core architectures [4] makes DTM much harder than before since the potential hotspot locations may not be predicted during the design phase [5].

Many efforts to deal with this problem give rise to the following technology directions: 1) increasing the number of sensing points and 2) placing them regularly, not on the potential hotspots only, as shown in Fig. 1. The statistics in the number of temperature sensors on high-performance processors shows evidence of this observation; it has been ever increasing but limited up to 44 sensors [6]. An intuitive way to achieve these goals is to reduce the size of each sensor. Most of the previous works tried to solve this problem by shrinking the circuit area of sensors and have brought significant improvements [5]. However, the sensor area is hard to shrink since large delay lines [7], [8] or bipolar junction transistor (BJT) with large ADC and digital circuits [9] are required to generate a proportional-to-absolute-temperature (PTAT) signal. Thus, it is impractical to use conventional sensors when a large number of sensing points are needed.

For these reasons, we devised a *complementary* sensing method for dense thermal map acquisition. The proposed method fully exploits the spatial low-pass filtering effect of thermal systems [10], which implies that most of the thermal

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information resides in a very low spatial frequency area. Inspired by this observation, a two-stage sensing strategy is proposed: to acquire low frequency information from conventional sensors (more area and accuracy) and reconstruct more dense thermal map by using high frequency information from auxiliary sensors (less area and accuracy).

Based on the idea above, we propose a hybrid temperature sensor network (HTSN). In contrast to the previous approaches, HTSN measures the dense temperature distribution in a logical manner rather than using the sensor outputs directly. It combines two types of thermal information from absolute temperature sensors (ATS) and relative temperature sensors (RTS). ATS is a conventional temperature sensor which provides PTAT information to construct a seed thermal map with low spatial resolution. RTS is a simple sensor that measures the thermal relativity between two sensing points. A thermal map upsampler (TMU) receives all the sensor outputs and doubles the spatial resolution of the seed thermal map (L1 upsampling) by a proposed guided upsampling algorithm (GU). This procedure works well even though the RTS provide limited information—higher, lower, or similar temperature since the local thermal gradient is not significant due to the smoothness property of thermal distribution. The area of RTS is extremely small and it greatly reduces the circuit area per each sensing point in an entire chip. In addition, HTSN with GU algorithm is highly scalable and the thermal map can be further upsampled to 4x higher resolution (L2 upsampling) with small area overhead. Moreover, HTSN is designed in an all-digital manner to reduce circuit complexity and design efforts in an advanced CMOS process.

This paper is organized as follows. Section II presents a brief analysis of chip's thermal characteristics as a preliminary study to this work. Section III describes the overall architecture of HTSN and detailed design of the sensor circuits. Section IV describes how a dense thermal map is reconstructed by using these sensors. Section V presents the measurement results. Finally, Section VI concludes this paper.

II. Spatial Low-Pass Filtering Effect

In order to acquire rich information of temperature distribution with minimum sensor circuitry, it is required to understand the physical nature of a chip's thermal system. As described in [10], a chip's temperature distribution is smooth over the die area, also known as the *spatial low-pass filtering effect*.

For a better understaning of thermal behavior, we used thermal node representation and electrical-thermal duality, as depicted in Fig. 2. In this representation, the entire die area is divided into a number of smaller die segments. Using electrical-thermal duality, spatial thermal resistance and heat capacity of each die segment are modeled with the electrical counterparts such as R_S and C_S respectively. Thus, the entire die can be represented as a RC mesh network which operates as a spatial low-pass filter. Note that this thermal node representation describes a *spatial* behavior, not a temporal one (more detailed explanation can be found in [10]).

To visualize this property, a proof-of-concept experiment was conducted. We used Hotspot thermal simulator [11] to obtain a

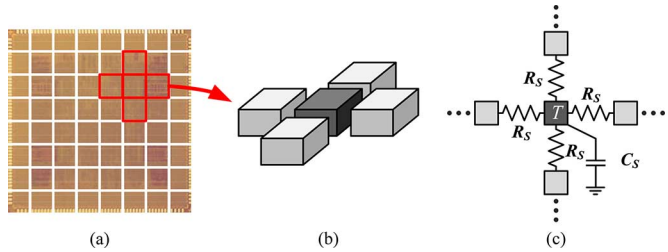

Fig. 2. Thermal node representation. (a) Entire die. (b) Die segments. (c) Equivalent spatial thermal schematic.

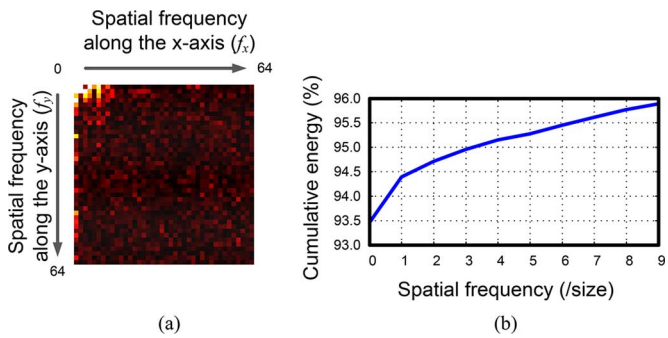

Fig. 3. Spatial frequency analysis of the thermal map from Hotspot [11]simulation of the test chip. (a) A 2-D frequency map. (b) A cumulative energy along the x-axis. 'Size' in the unit of spatial frequency means the die size (width or height).

thermal map of our test chip. Then the thermal map is transformed into a spatial frequency domain. In this experiment, we observed that the temperature information is highly concentrated within very low frequency area, as depicted in Fig. 3(a). More quantitative visualization (Fig. 3(b)) shows that 93.5% of the entire information resides in DC region. This is strong evidence of the spatial low-pass filtering effect. As a result, we realized that an area-efficient sensing architecture can be designed by combining two sensor circuits dedicated to low (0–1/size) and high (2∼/size) spatial frequency bands.

III. Hybrid Temperature Sensor Network

Fig. 4 describes the hierarchical sensing architecture of HTSN. The proposed scheme is designed based on the spatial low-pass filtering effect which implies that the majority of the temperature information can be captured by a small number of ATS. The number of ATS is determined in design time through a spatial frequency domain analysis. The role of ATS layer is to generate a seed thermal map which will be elaborated (upsampled) by TMU. In upsampling phases, the second type of sensor (RTS) is used to capture only a local thermal relativeness of two sensing points. Exploiting this local gradient information from RTS network, TMU doubles the resolution of seed thermal map.

A. Absolute and Relative Temperature Sensors

In a trade-off between accuracy and circuit area, ATS design has to focus on its accuracy since the final thermal map is highly sensitive to the seed thermal map. Thus, any type of

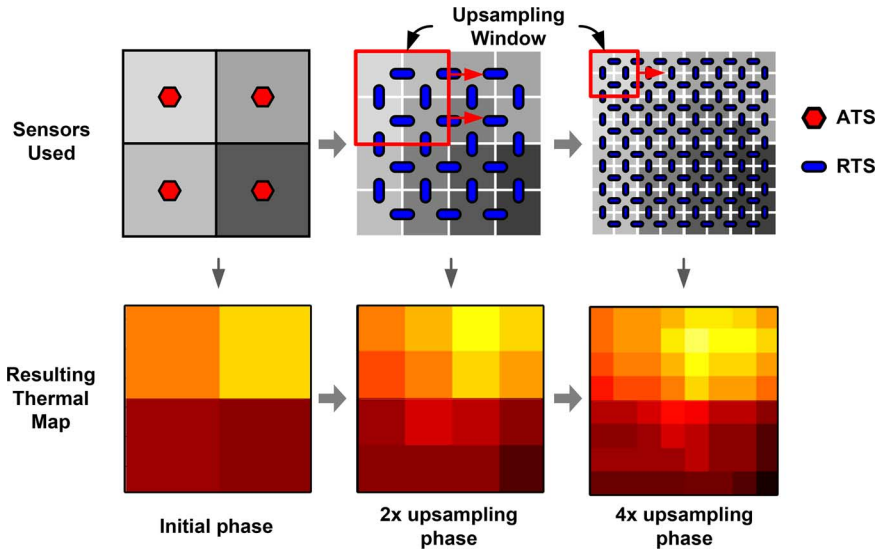

Fig. 4. Hierarchical sensing architecture of HTSN.

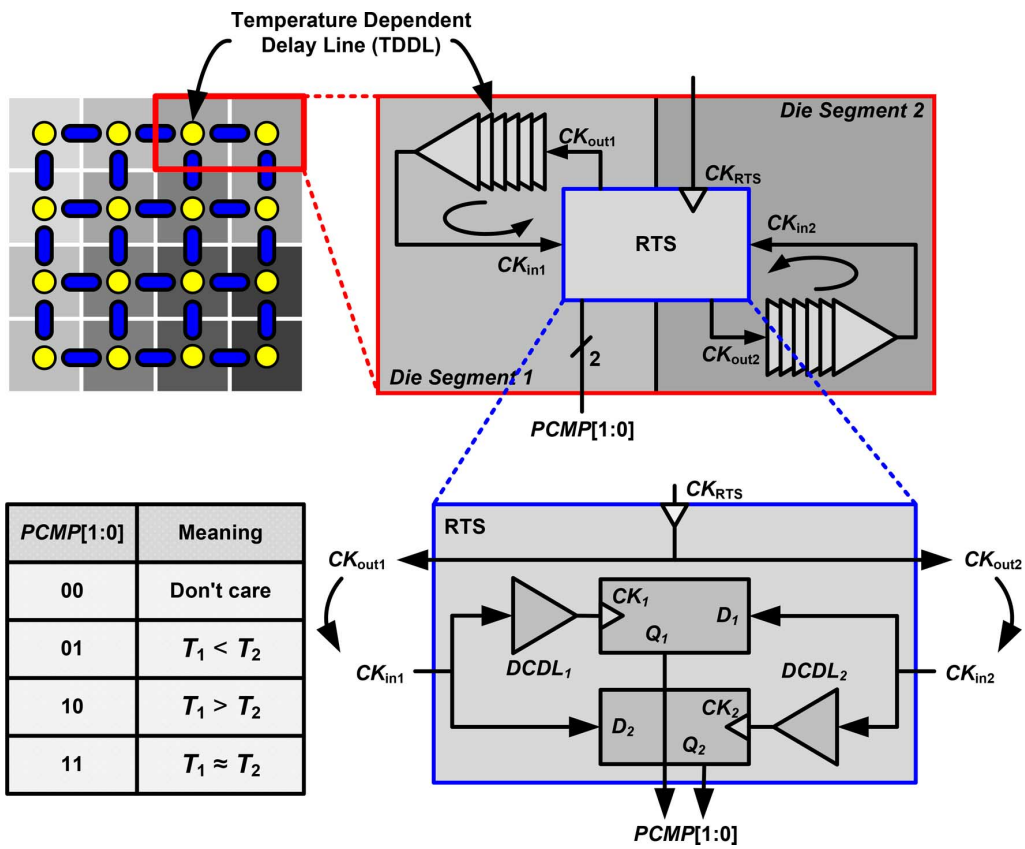

Fig. 5. A schematic and a sensing mechanism of a time-domain RTS.

conventional temperature sensors can be used to play a role of ATS as long as it shows enough accuracy. In this work, we used a dual-DLL-based temperature sensor [8] for a construction of seed thermal map.

RTS provides a limited thermal gradient information required for GU algorithm. In this work, the RTS is designed as a time-domain sensor using bang-bang phase detector as illustrated in Fig. 5. It consists of two D flip-flops (DFF) and digitally controlled delay lines (DCDL) for threshold temperature control. Given a clock signal $\mathrm{CK_{RTS}}$, RTS re-transmits the clock signals $(\mathrm{CK_{out}})$ to two sensing points simultaneously. Then it determines whether the temperature of a point is higher or lower than the other by comparing the phases of the returning clock signals $(\mathrm{CK_{in}})$. On each of the sensing points, there is a temperature-dependent delay line (TDDL) to generate a temperature-dependent phase change. Finally, the bang-bang phase

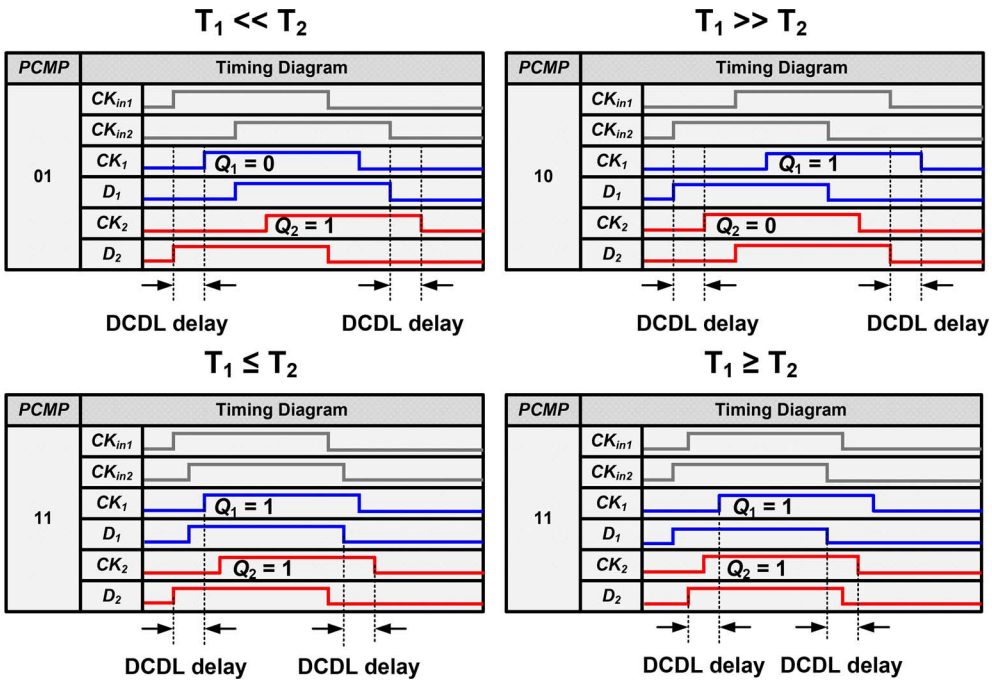

Fig. 6. A detailed waveform of four possible sensing scenarios of RTS.

detector generates a thermal gradient signal, also called physical comparison (PCMP) in the GU algorithm. In our implementation, the delay difference between TDDLs (typically less than 1 ns) is much smaller than RTS clock period (10 ns) since every phase comparison is made only between the neighboring TDDLs. In order to handle longer delay difference, designers can increase the RTS clock period without loss of accuracy and dynamic range.

Fig. 6 describes four possible temperature comparison results. PCMP is designed to describe one of the following conditions: $T_1 > T_2$, $T_1 < T_2$, and $T_1 \approx T_2$. For instance, if T_1 is higher than T_2, the PCMP output is '01' since the returning clock $\mathrm{CK_{in2}}$ lags behind $\mathrm{CK_{in1}}$. The PCMP value becomes '11' when the phase difference between $\mathrm{CK_{in1}}$ and $\mathrm{CK_{in2}}$ is smaller than the threshold which is determined by DCDL delay and the DFF's setup-time. TMU collects 100 PCMP samples and chooses the most frequent one to mitigate the effect of noise in $\mathrm{CK_{in1}}$ and $\mathrm{CK_{in2}}$.

B. Discussion About Thermal Inversion

The basic assumption of the RTS in this work is that the propagation delay of TDDL is positively correlated with temperature. However, especially with a deep sub-micron process, it is not always true, i.e., there can be a negative dependence between the propagation delay and temperature [12]. This phenomena is known as *thermal inversion*. In this case, designers cannot adopt time-domain-based sensors. One possible solution is to use voltage-based sensors. For an ATS, a BJT-based sensor [5], [9] is an appropriate choice to be robust to thermal inversion.

RTS also can be designed in voltage domain by comparing two voltage outputs from temperature-to-voltage circuits and generates PCMP signal by comparing these signals.

Since the voltage-based design is also vulnerable to power supply noise, enough number of sample for averaging is required to ensure correct comparison result. In addition, we can expect further area reduction since the temp-to-voltage sensor does not have delay-lines which occupy relatively large area in our delay-based design.

IV. Upsampling Thermal Map

Given the sensor readouts, the next step is to combine these to form richer thermal map. We propose a simple algorithm for this task, called guided upsampling. The term "guided" stands for the role of RTS which guides the upsampling algorithm to carve the seed thermal map correctly.

A. Guided Upsampling Algorithm

The upsampling process is performed in a window-by-window manner, as shown in Fig. 4. In a sliding window, four temperature values (T_1–T_4) and four PCMP signals are provided.

The rule of LCMP computation is similar to that of PCMP. A threshold value T_{th} is used to determine the case of similar temperature. The value of T_{th} is also determined by pre-silicon simulation of RTS. Given T_a and T_b, the LCMP corresponding to the cases of $T_a - T_b > T_{\mathrm{th}}$, $-T_{\mathrm{th}} < T_a - T_b < T_{\mathrm{th}}$ and $T_a - T_b < -T_{\mathrm{th}}$ are 2'b10, 2'b11, and 2'b01, respectively.

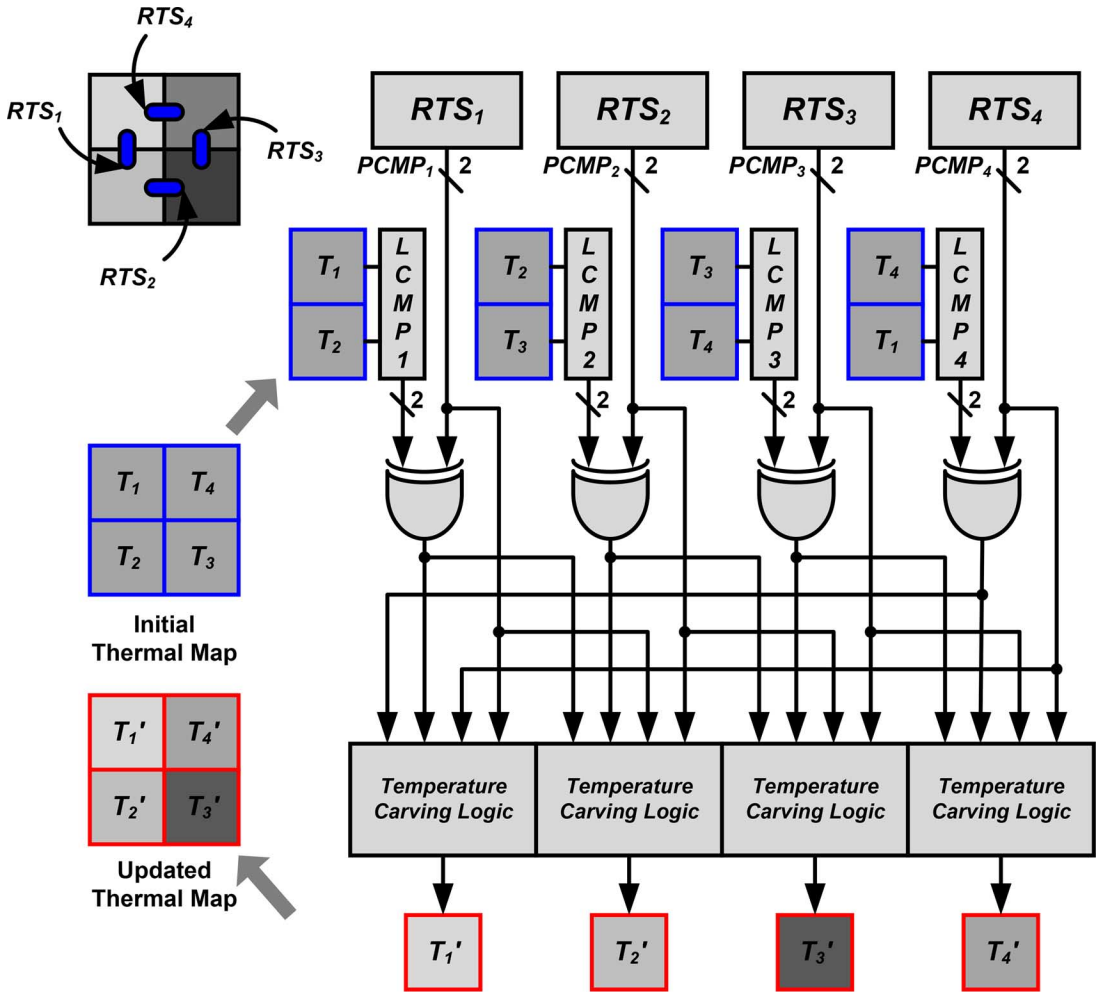

Fig. 7. Detailed schematic of TMU.

Algorithm 1. Guided upsampling algorithm for computing T_1'

$\Delta T_1 = 0$
if $PCMP1$ xor $LCMP1! = 0$ **then**
  if $PCMP1 ==$ 2'b10 $(T_1 > T_2)$ **then**
    $\Delta T_1 = \Delta T_1 + T_c$
  else if $PCMP1 ==$ 2'b01 $(T_1 < T_2)$ **then**
    $\Delta T_1 = \Delta T_1 - T_c$
  end if
end if
if $PCMP4$ xor $LCMP4! = 0$ **then**
  if $PCMP4 ==$ 2'b10 $(T_4 < T_1)$ **then**
    $\Delta T_1 = \Delta T_1 - T_c$
  else if $PCMP4 ==$ 2'b01 $(T_4 > T_1)$ **then**
    $\Delta T_1 = \Delta T_1 + T_c$
  end if
end if
$T_1' = T_1 + \Delta T_1$

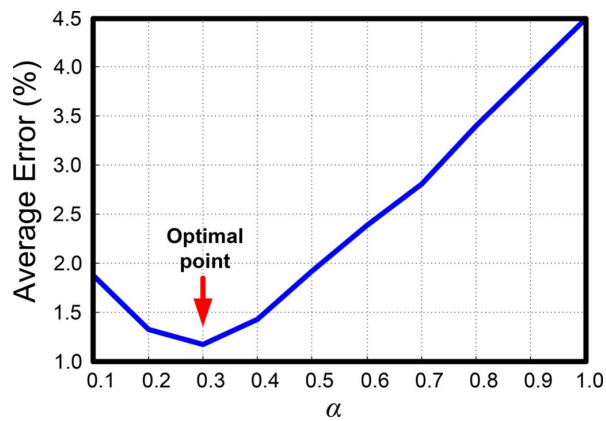

Fig. 8. Error analysis using pre-silicon simulation of GU algorithm. In our implementation, $\alpha = 0.3$ was the best configuration.

Initially, the temperature values are set to the same value from the corresponding lower-level upsampling window. Then the algorithm examines whether LCMP agrees with PCMP from RTS. Fig. 7 and Algorithm 1 describe the schematic of TMU and a detailed procedure when TMU updates T_1. Since T_1 faces two neighboring nodes, T_2 and T_4, the actual update takes place two times. If the actual thermal gradient is not reflected to the thermal map i.e., LCMP and PCMP do not agree with each

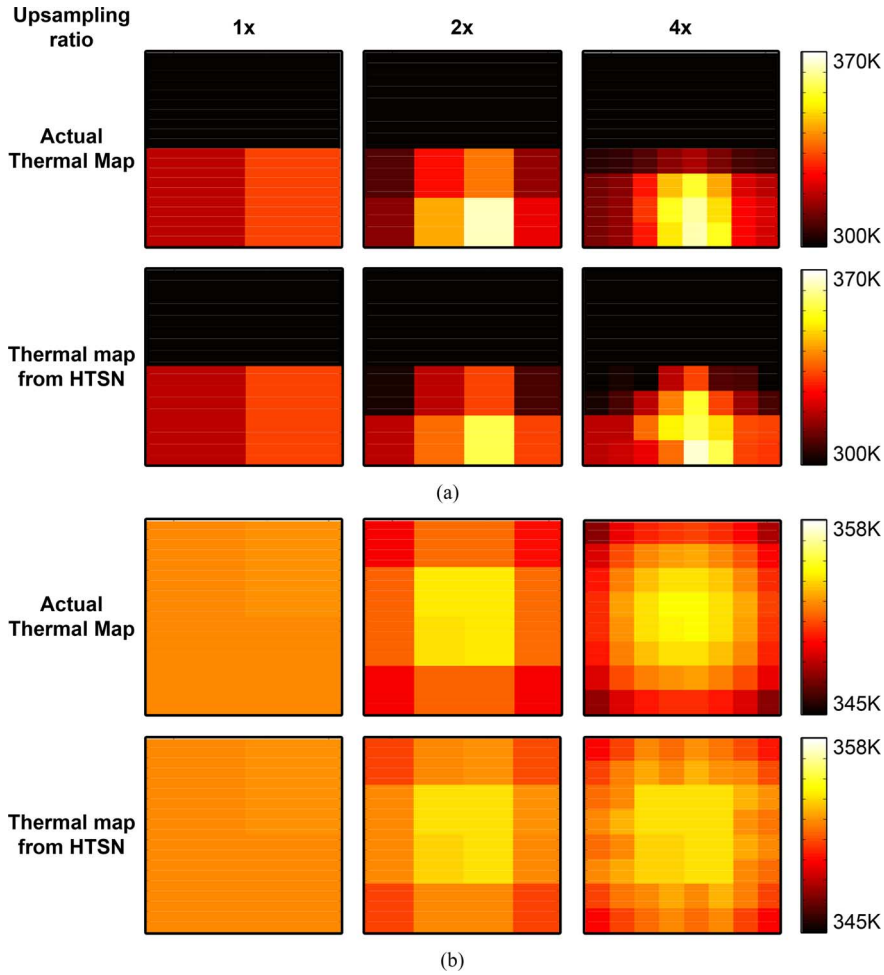

Fig. 9. Simulation results of GU algorithm. (a) High thermal gradient. (b) Low thermal gradient.

other, the temperature carving logic (TCL) is activated to reflect the PCMP values in the updated temperature value. TCL simply adds or subtracts a pre-determined temperature carving interval T_c to the original temperature value based on the activation and PCMP signals. To maintain the stability, T_c should be less than the half of the maximum possible temperature difference within the upsampling window, as described in the following equation:

$$T_c = \alpha \cdot \max(|T_1^* - T_2^*|, |T_2^* - T_3^*|, |T_3^* - T_4^*|, |T_4^* - T_1^*|) \quad (1)$$

where α is an empirically deteremined parameter and T_k^* is the kth element of the lower-level thermal map.

In our case, $\alpha = 0.3$ was the best parameter which was determined by pre-silicon simulation of GU algorithm (Fig. 8). The upsampling window scans the entire die area in forward and backward direction to remove directional bias. Fig. 9 shows the simulation results of GU algorithm. We investigated two extreme cases with high and low thermal gradient and successfully identified the hotspot locations.

B. HTSN System Design

Fig. 10 shows the sensor architecture of our implementation. HTSN provides 64 bit ATS (16 bit for each ATS), and 136 bit PCMP signals from RTS networks. Using these information, TMU runs GU algorithm and writes the resulting thermal map to the thermal map register file. The parameters for GU algorithm and the thermal maps are transferred via host interface.

For time-division multiplexing, a 4-to-1 MUX and 1-to-4 DEMUX are placed at the input and output of TDDLs respectively. The phased control signals are provided by TMU.

V. Measurement Result

We verified the proposed sensing architecture by designing a quad-core processor with HTSN in 0.13 μm CMOS as shown in Fig. 12 and Table I. Each core has its own clock domain, enabling a per-core frequency scaling to induce a temperature gradient. The target measurement area of HTSN is 1.8 mm $\times$ 1.8 mm. Fig. 13 shows the measurement setup. The ARM-based host system assigns workload/frequency pair to each core and retrieves upsampled thermal map data, which is visualized using MATLAB.

We performed a TDDL calibration before the actual measurement. In uniform temperature state, we checked whether the RTS outputs generated ‘similar temperature’ (2'b11) signals. In our measurement, no calibration on TDDL is required since the

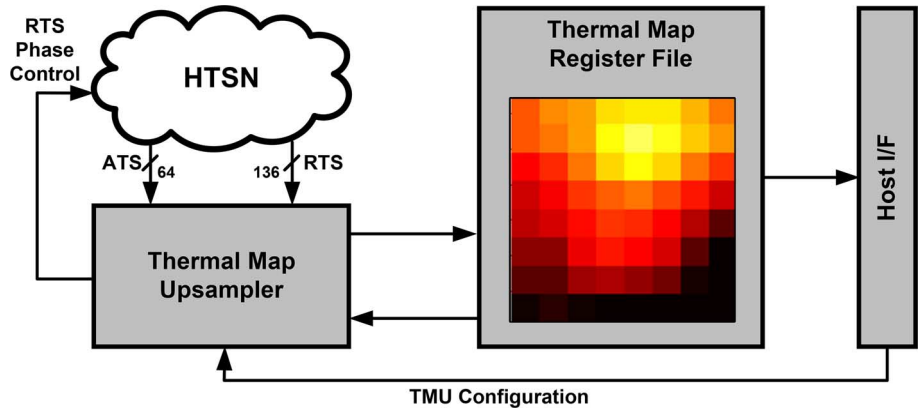

Fig. 10. HTSN control system.

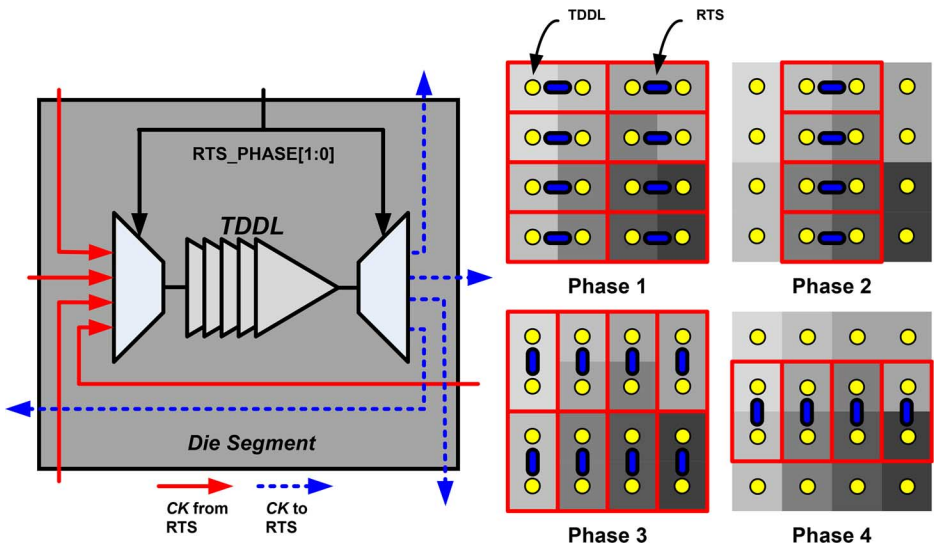

Fig. 11. 4-phase sensing scheme.

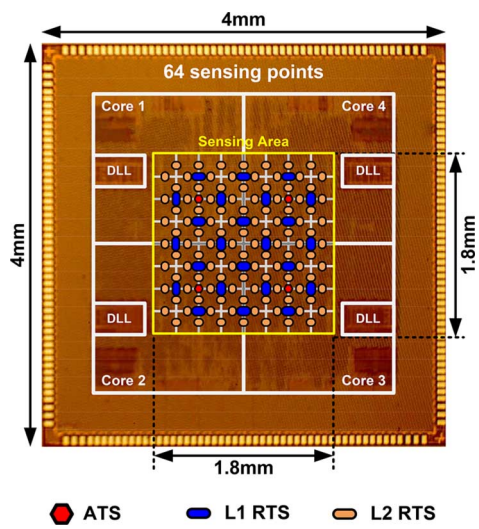

Fig. 12. Die micrograph.

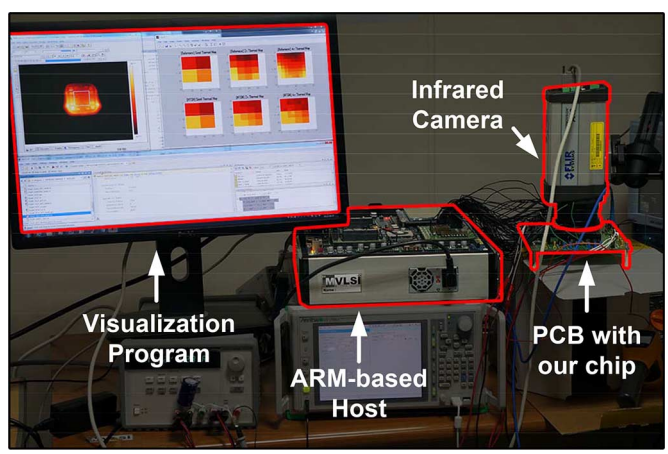

Fig. 13. The measurement setup. An infrared camera is used to capture the actual thermal map.

die area was relatively small and RTS compares only the neighboring TDDL delays. However, if HTSN is applied to large commercial processor, the TDDL calibration feature should be carefully designed.

We used an infrared (IR) camera to obtain the reference thermal map (Fig. 14). The accuracy of our IR camera was $\pm 2\%$ which is not negligible in our experiment. To overcome this accuracy problem, we used two measurement strategies. First, we calibrated ATS to the IR camera readouts. This is reasonable since this work focuses on RTS performance, rather than ATS. By doing this, we could eliminate the DC bias of seed thermal

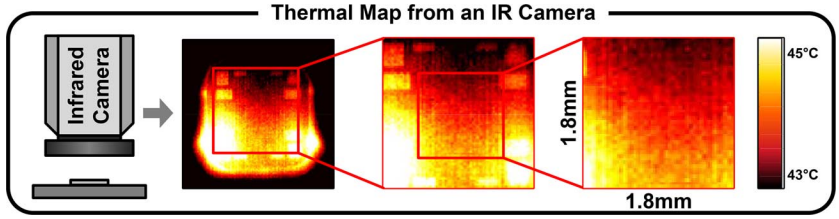

Fig. 14. Thermal map acquisition process.

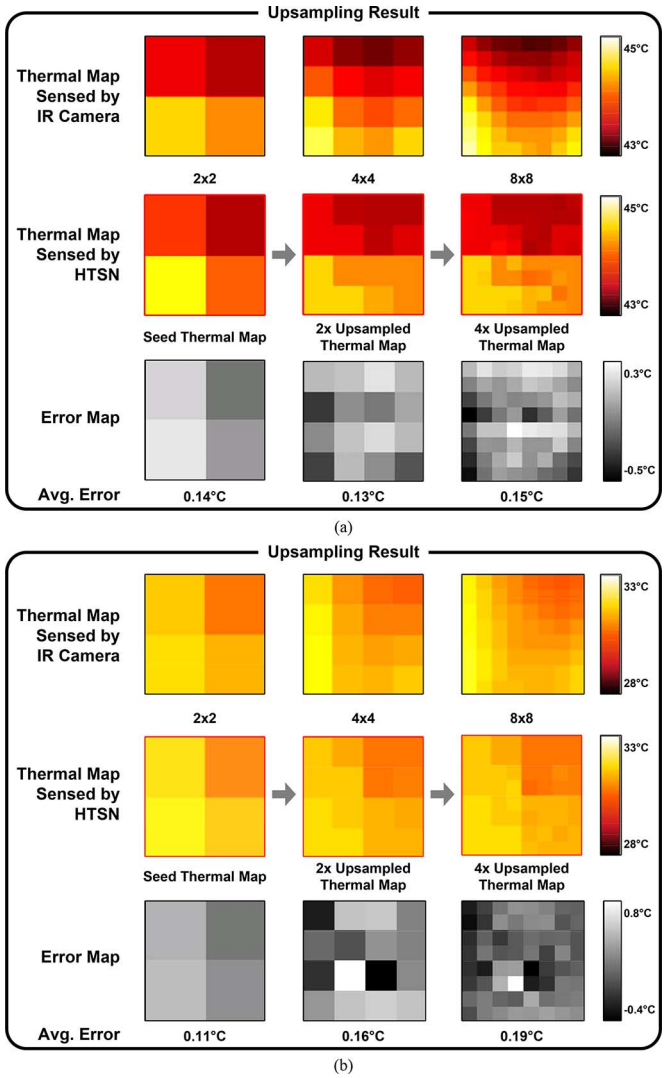

Fig. 15. Measurement results with temperature range of (a) 43°C–45°C; (b) 28°C–33°C.

maps. Secondly, IR camera signals are averaged over time since the actual thermal map does not change during measurement. For each analysis, we averaged 100 thermal images.

Fig. 15 shows the measurement results. The error maps have spatially uncorrelated distribution which implies that the upsampling process does not induce any spatial bias.

Table II shows the area breakdown of HTSN. Maintaining acceptable accuracy, the required circuit area per sensing point is reduced drastically. Even though many RTS and TDDL blocks are used, the effective area of a sensing point is rather small due to the extremely simple design of RTS.

TABLE I
IMPLEMENTATION DETAIL

Technology	0.13μm CMOS (1P6M)
Power Supply	1.2V (Core) / 3.3V (IO)
Chip Size	4mm x 4mm
Sensing Area	1.8mm x 1.8mm
Operating Frequency	100MHz (HTSN) / 400MHz (TMU)
HTSN Sensing Rate	L1: 3.4MS/s L2: 1.8MS/s for a single GU iteration

TABLE II
AREA BREAKDOWN OF HTSN

Module	Number	Area (μm^2)
ATS	4	19,916
TDDL	80	92,400
RTS	136	28,560
TMU	1	27,071
Total area (64 sensing points)		167,947
Area per sensing point		2,624

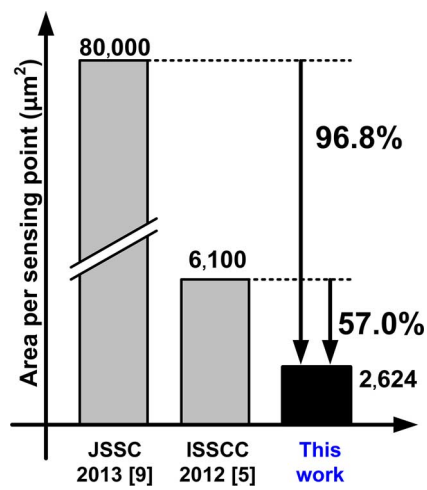

Fig. 16. Area efficiency compared to the previous works.

Fig. 16 shows the area efficiency of the proposed architecture. Compared to the conventional design, our architecture achieves 57% reduction of the area per sensing point over the most area-efficient previous art [5].

VI. Conclusion

In this paper, we have proposed a hybrid temperature sensor network for area-efficient thermal map sensing. The on-chip sensor network consists of a small number of accurate thermal sensors and a large number of tiny relative thermal sensors. By combining these sensor readouts, a thermal map upsampler synthesizes a higher spatial resolution thermal map with a proposed guided upsampling algorithm.

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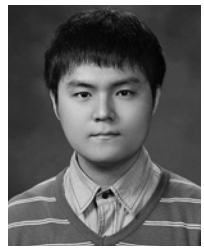

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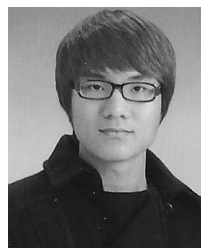

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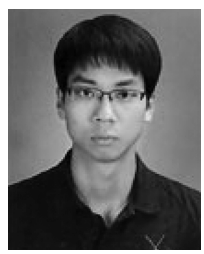

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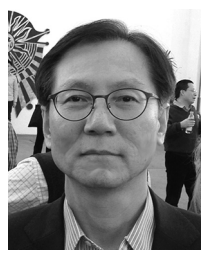

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