

Thermal Management of On-Chip Hot Spot

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The rapid emergence of nanoelectronics, with the consequent rise in transistor density and switching speed, has led to a steep increase in microprocessor chip heat flux and growing concern over the emergence of on-chip hot spots. The application of on-chip high flux cooling techniques is today a primary driver for innovation in the electronics industry. In this paper, the physical phenomena underpinning the most promising on-chip thermal management approaches for hot spot remediation, along with basic modeling equations and typical results are described. Attention is devoted to thermoelectric microcoolers and two-phase microgap coolers. The advantages and disadvantages of these on-chip cooling solutions for high heat flux hot spots are evaluated and compared.

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1 Introduction

Microelectronics has become the heart of any modern electronic product from home/office PC systems, to advanced transportation, navigation, and energy management electronic systems. However, because all the microelectronic devices require power for their use, the conversion of electrical energy to thermal energy is an unavoidable by-product of the normal operation of any electronic devices and leads to higher microprocessor temperature that, if not properly managed, will significantly affect the performance, leakage power, and reliability of a micro-electronic chip, assembly, and product. Moreover, recent advances in device miniaturization and design complexity are causing highly nonuniform power distribution on the microprocessors, producing "high-flux hot spots." These specific regions on the chip can have a heat flux several times higher than the chip average, of the order of 1 kW/cm^2 , thus resulting in exceedingly high local temperatures that can dramatically degrade microprocessor performance and system reliability [1]. On the other hand, if effective localized cooling of performance-critical macrocells can be achieved, the resulting "cold spots" can produce speed gains as large as 200% in some complementary metal oxide semiconductor (CMOS) microprocessors [2]. For this reason, mitigating the chip-level hot spot effects through localized cooling has become one of the most significant factors in the design of high-performance electronic products and has evolved into a primary driver for innovation in electronics cooling technology.

Beyond the challenge of continuously enhancing available thermal management techniques for high heat flux chips, the need to develop cooling approaches that can specifically handle such microscale high flux hot spots has become a primary roadblock to the commercialization of next-generation microelectronic devices and systems. The application of conventional thermal packaging technology and uses of traditional thermal management hardware such as heat sinks and heat pipes, developed to provide uniform chip cooling, to such nanoelectronic chip designs, result in lower allowable chip power dissipation or unnecessary overcooling of large areas of the chip. Consequently, new and novel cooling techniques, with the ability to selectively cool submillimeter hot spots, are in urgent demand. Advanced liquid cooling techniques, such as microchannel cold plates, liquid immersion cooling, and jet/spray cooling, provide very high heat transfer coefficients and could be

used to meet these requirements [3]. However, the reliability, complexity, volume, weight, and cost are the major barriers to successful commercial implementation of these approaches. In this paper, we discuss and compare the novel hot spot remediation techniques using thermoelectric microcoolers and two-phase microgap coolers. The advantages and disadvantages of these on-chip cooling solutions for high flux hot spots are evaluated.

2 Prediction of Hot Spot Temperature

Hot spots are localized regions on microprocessors with very high heat flux, resulting in exceedingly high local temperature. Due to the hot spots, the temperature differential across a microprocessor can vary from 5°C to 30°C and the reliability of the circuit is thus mainly determined by the hot spot temperatures. To accurately predict hot spot temperature on a microprocessor, it is required to derive an exact analytical solution of three-dimensional Laplace's equation for the temperature distribution in a volume subjected to a small, uniform heat flux source (hot spot) on a thin silicon slab [4]. For simplicity, the classical result for a specified hot spot with a uniform heat flux on a semi-infinite slab, given by Eq. (1), can provide a baseline calculation of the local temperature rise

$$\Delta T_{\text{semi-inf}} = \frac{q''_{\text{hotspot}} w_{\text{hotspot}}}{\pi^{0.5} k_{\text{Si}}} \quad (1)$$

where q''_{hotspot} is the heat flux of the hot spot on the semi-infinite slab, w_{hotspot} is the hot spot size, and k_{Si} is the thermal conductivity of silicon substrate. To account for heat spreading effect for a silicon chip with a thickness of t_{Si} , a simplified closed-form equation to estimate hot spot temperature rise is derived as follows [8]:

$$\Delta T_{\text{hotspot}} = \frac{q''_{\text{hotspot}}}{k_{\text{Si}}} \left(0.237 \frac{w_{\text{hotspot}}^2}{t_{\text{Si}}} - 209.4 w_{\text{hotspot}}^2 + 0.56 w_{\text{hotspot}} \right), \\ r^2 = 0.99 \quad (2)$$

Figure 1 compares the hot spot temperature rise, predicted using Fourier-series exact solution [4], with the values obtained from the simplified solution, using Eq. (2). In this comparison, the silicon chip thickness ranges from $100 \mu\text{m}$ to $500 \mu\text{m}$, and hot spot size varies from $20 \mu\text{m} \times 20 \mu\text{m}$ to $300 \mu\text{m} \times 300 \mu\text{m}$, while its heat flux is fixed at 1000 W/cm^2 as an example. Figure 1 reveals that for progressively smaller hot spots and thicker silicon chips, the present closed-form equation asymptotically approaches

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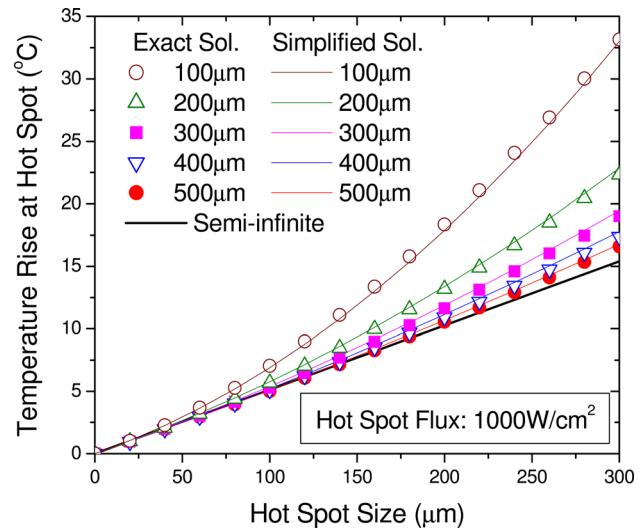


Fig. 1 Hot spot temperature rise as a function of hot spot size for various silicon chip thickness [8]

the classical semi-infinite values. For larger hot spots and/or thinner chips, the temperature rise is substantially higher than the semi-infinite values but Eq. (2) yields values that are less than 2% different from the exact solution. We also obtain similar results with various hot spot heat fluxes indicating that Eq. (2) is a very convenient way to accurately predict hot spot temperature rise.

3 On-Chip Hot Spot Cooling Using Thermoelectric Cooler

Thermoelectric coolers for hot spot thermal management have received considerable attention because these solid state devices can offer high reliability, can be locally and selectively applied for spot cooling, can provide high cooling heat flux, and can be integrated with integrated circuit (IC) processing [4–16]. In this section, the underlying physics of recently developed thermoelectric coolers (TECs), including minicontact enhanced Bi_2Te_3 TECs, in-plane Si μ TEC's, superlattice SiGe TEC's, and superlattice Bi_2Te_3 TEC's are described and their ability to suppress on-chip hot spots is modeled and evaluated.

3.1 Mini-Contact Enhanced TEC. Conventional thermoelectric coolers can only provide a cooling heat flux about $10 \text{ W}/\text{cm}^2$, severely limiting the direct application of these devices to high heat flux hot spot remediation [1]. Recently, the novel use of

a minicontact pad, connecting the TEC and the silicon chip, thus concentrating the thermoelectric cooling power on a small area on the top of the silicon chip, as shown in Fig. 2, was proposed and investigated [5,6].

A 3D finite element method (FEM) thermal model was developed and used to determine the efficacy of applying such a minicontact enhanced TEC to a typical chip package with the geometry and material properties listed in Table 1. The effective cooling power, which is the combination of the thermoelectric cooling power, $ST_c I$, and Joule heating from the electric contact resistance at the interface between the thermoelectric element and the metallization layer, $I^2 R_{\text{ec}}$, is imposed as a surface boundary condition on the cold side of the TE element in this simulation, yielding a corresponding cooling heat flux of

$$q''_{\text{TE,c}} = \frac{-S_{\text{Bi}_2\text{Te}_3} T_c I + I^2 R_{\text{ec}}}{A_{\text{TE Element}}} \quad (3)$$

Similarly, the effective heating power is imposed as a surface boundary condition on the hot side of the TE element with a corresponding heating heat flux of

$$q''_{\text{TE,h}} = \frac{S_{\text{Bi}_2\text{Te}_3} T_h I + I^2 R_{\text{ec}}}{A_{\text{TE Element}}} \quad (4)$$

where S is the Seebeck coefficient of thermoelectric material, T_c and T_h are the average temperatures of the cold side and the hot side of the TE element, respectively, R_{ec} is the electric contact resistance, and $A_{\text{TE Element}}$ is the base area of TE element. The Joule heating inside the thermoelectric elements is input as volumetric heat generation in the numerical simulation.

Figure 3 shows the temperature profiles that could be achieved along a line bisecting the bottom of the silicon chip cooled by a TEC with $20 \mu\text{m}$ -thick Bi_2Te_3 elements. When such an advanced miniaturized TEC is activated with 10 W and enhanced with a $1250 \mu\text{m} \times 1250 \mu\text{m}$ copper minicontact pad, a 17°C hot spot temperature reduction can be obtained [5]. Due to the effect of the heat concentrating/spreading resistance inside the minicontact pad and the silicon chip, there is the “optimum” minicontact geometry for this application. If the minicontact size is extended to $2400 \mu\text{m} \times 2400 \mu\text{m}$ or reduced to $600 \mu\text{m} \times 600 \mu\text{m}$, the hot spot cooling is decreased to 12°C and 9°C , respectively.

Thermoelectric element thickness is a key parameter for improving the hot spot cooling performance as the maximum achievable cooling heat flux of a TEC is inversely proportional to the element thickness. Figure 4 illustrates the variation of hot spot cooling with the minicontact size for three different thermoelectric element thicknesses under optimized input power on the TEC. As is expected, thinner thermoelectric elements allow the TEC to

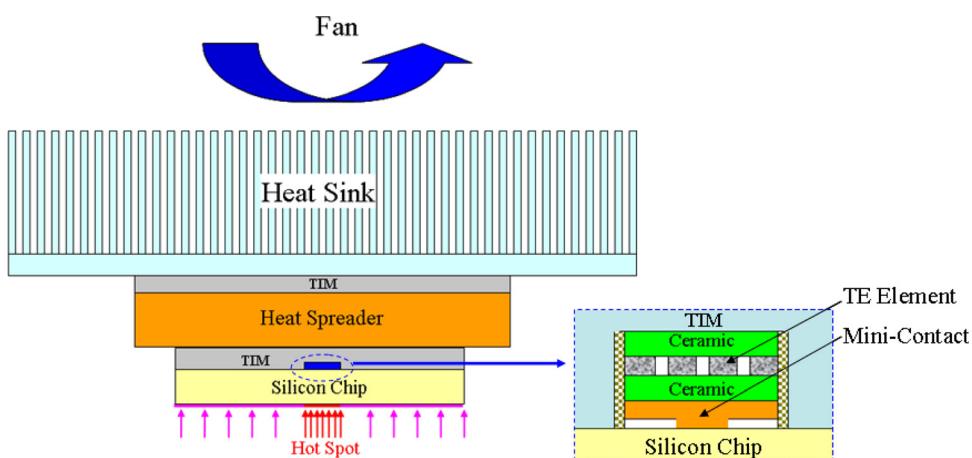


Fig. 2 Schematic of minicontact enhanced TEC for hot spot remediation [5,6]

Table 1 Geometry and material properties used for package-level thermal model

	Geometry	Materials	$k(\text{W/m K})$
Heat sink base	50 mm × 50 mm × 5 mm	Al	180
Heat spreader	31 mm × 31 mm × 1.5 m	Cu	360
TIM3	31 mm × 31 mm × 175 μm	Solder	30
TIM2	31 mm × 31 mm × 30 μm	Solder	30
TIM1	11 mm × 13 mm × 300 μm	Solder	30
TE element	2.4 mm × 2.4 mm × 20 μm	Bi_2Te_3	1.4–1.5 ^a
Silicon die	11 mm × 13 mm × 500 μm	Silicon	90–150 ^a
Minicontact base	2.4 mm × 2.4 mm × 100 μm	Cu	360
Minicontact tip	Height = 50 μm ^b	Cu	360
Ceramic substrate	2.4 mm × 2.4 mm × 50 μm	AlN	180

^aTemperature dependent thermal conductivity is used.

^bThe cross-sectional area of the minicontact tip will change from 600 $\mu\text{m} \times 600 \mu\text{m}$ to 2400 $\mu\text{m} \times 2400 \mu\text{m}$.

achieve better hot spot temperature reductions, e.g., 6 °C to 11.2 °C and to 17.0 °C, as the thermoelectric element decreases from 100 μm to 50 μm and to 20 μm in thickness, using the optimum minicontact tip size. Even though the minicontact tip size is kept constant, thinner thermoelectric elements always yield better hot spot cooling than thick elements. However, it is interesting to find that the optimum minicontact tip size increases with decreasing element thickness, from 800 $\mu\text{m} \times 800 \mu\text{m}$ for a 100 μm thick element to 1000 $\mu\text{m} \times 1000 \mu\text{m}$ for a 50 μm thick element, and to 1250 $\mu\text{m} \times 1250 \mu\text{m}$ for a 20 μm thick element.

It is also found that achieving low thermal resistance interfaces is critical to the success of minicontact TEC cooling, since a high thermal resistance at the minicontact/chip interface will significantly reduce the effectiveness of the minicontact enhancement. Moreover, a poor thermal interface between the TEC and the thermal interface material (TIM) will impede the dissipation of Peltier heat and Joule heat into the heat spreader and then into the heat sink and the ambient, raising the temperature of the TEC. Figure 5 displays the interplay between the thermal contact resistance and the maximum achievable hot spot cooling, with the assumption of equal thermal contact resistance at the two interfaces (e.g., $R_{c1} = R_{c2} = R_c$), revealing that with increasing thermal contact resistance at both interfaces, the net cooling achievable on the hot spot diminishes. For the typical configuration studied, the minicont-

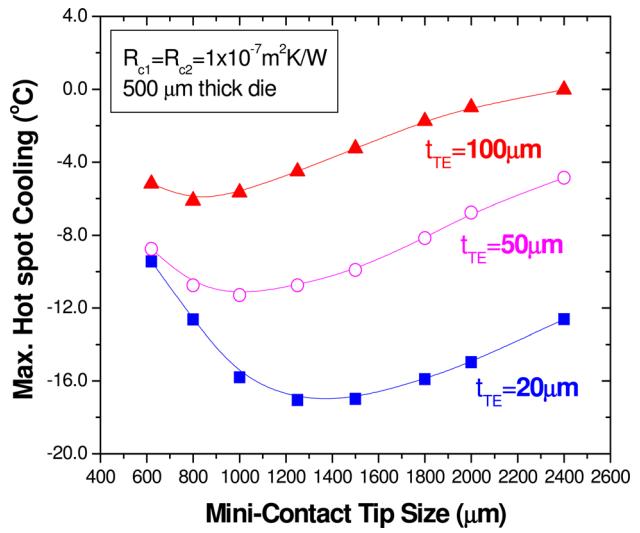


Fig. 4 Effect of thermoelectric element thickness on the hot spot cooling performance. Bismuth telluride element thickness t_{TE} is 20 μm , 50 μm , and 100 μm , respectively, silicon chip thickness is 500 μm , and the hot spot size is 400 $\mu\text{m} \times 400 \mu\text{m}$ with a heat flux of 1250 W/cm^2 , the electrical contact resistivity is $1 \times 10^{-7} \Omega \text{ cm}^2$, and the thermal contact resistance is $1 \times 10^{-7} \text{ K cm}^2/\text{W}$ [5].

tact is seen to provide excellent cooling with interface resistances below $1 \times 10^{-6} \text{ m}^2 \text{ K/W}$ but to display diminishing returns as the contact resistances increase and to elevate the hot spot temperatures for thermal contact resistances equal to or above $1 \times 10^{-5} \text{ m}^2 \text{ K/W}$.

To demonstrate minicontact enhancement effect and hot spot cooling efficiency, the miniaturized TECs with 200 μm -thick thermoelectric elements from Thermion, Inc. (Mode number: 1MC04-018-02-2200D) [11] were tested. The experimentally observed effect of the minicontact tip size on the temperature reduction at the targeted spot of a uniformly heated chip is displayed in Fig. 6 for three different power dissipations on a 20 mm × 20 mm × 500 μm chip. For the case of no power dissipation on the silicon chip, if the minicontact is of the same size as the TEC base, the measured maximum spot cooling is about 3.3 °C. However, if a

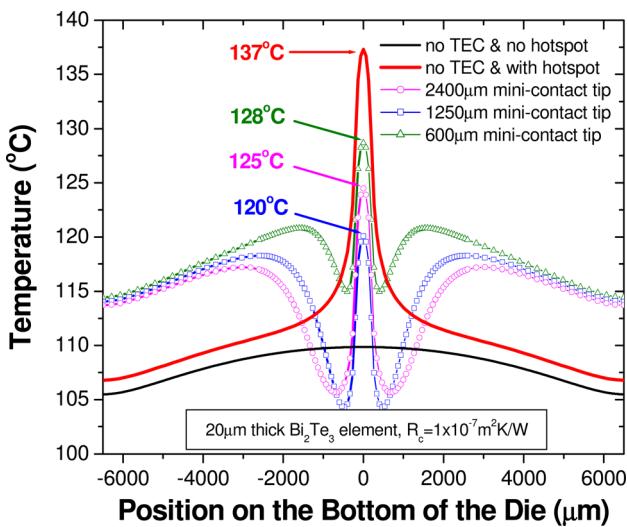


Fig. 3 Effect of minicontact size on TEC-induced temperature profile. Bismuth telluride element thickness is 20 μm , silicon chip thickness is 500 μm , the hot spot size is 400 $\mu\text{m} \times 400 \mu\text{m}$ with a heat flux of 1250 W/cm^2 , the electrical contact resistivity is $1 \times 10^{-7} \Omega \text{ cm}^2$, and the thermal contact resistance is $1 \times 10^{-7} \text{ K cm}^2/\text{W}$ [5].

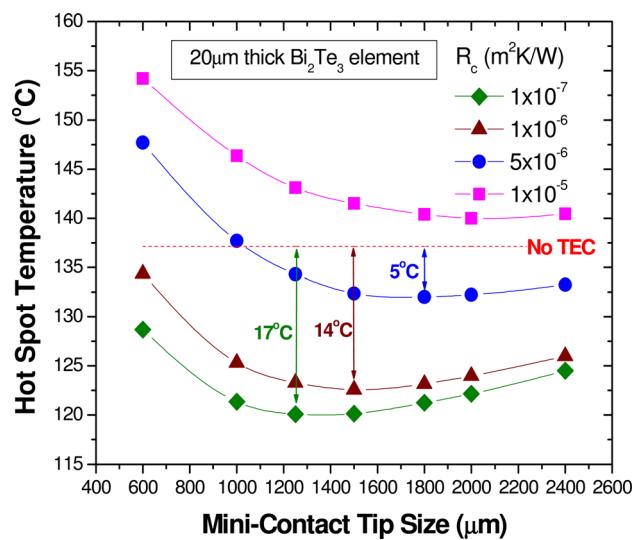


Fig. 5 Influence of thermal contact resistance on hot spot cooling. Bismuth telluride leg thickness is 20 μm , silicon chip thickness is 500 μm , and the hot spot size is 400 $\mu\text{m} \times 400 \mu\text{m}$ with a heat flux of 1250 W/cm^2 , the electrical contact resistivity is $1 \times 10^{-7} \Omega \text{ cm}^2$ [5].

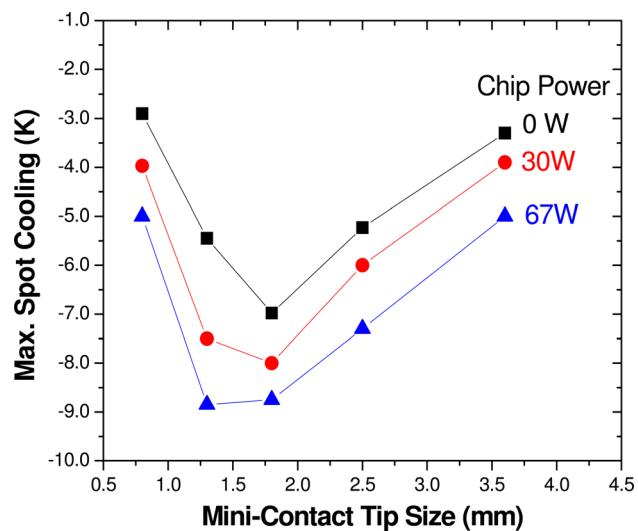


Fig. 6 Variation of measured maximum spot cooling with copper minicontact size. Thermion miniaturized TEC has 200 μm thick elements and silicon chip thickness is 500 μm [5].

1.8 mm \times 1.8 mm copper minicontact is integrated onto the TEC, 7.1°C maximum spot cooling can be obtained which results in 115% improvement on spot cooling performance. Similarly, by selecting the optimum minicontact size, spot cooling performance can be improved by 100% and 80%, when the power dissipation of the silicon chip is 30 W and 67 W, respectively.

3.2 In-Plane Silicon Microcooler. The concept of an in-plane silicon thermoelectric microcooler for on-chip hot spot cooling, fabricated on the back of the silicon chip, is illustrated in Fig. 7, which displays a single microcooler, activated by an electric current entering the silicon chip through the metal lead and the silicon cap, flowing laterally through the chip and exiting at the ground electrode located on the periphery of the chip [4]. The possible use of silicon microcoolers for the remediation of on-chip hot spots is facilitated by the use of well established metal-on-silicon fabrication techniques, yielding a very low thermal contact resistance between the metal and the chip. In addition, incorporation of the silicon chip into the thermoelectric circuit makes it possible to transfer the absorbed energy via the electric current to the edge of the chip, far from the location of the hot spot, thus substantially reducing the detrimental effect of thermoelectric heating on the temperature of the active circuitry.

The effective cooling flux applied on the silicon microcooler [4] surface can be expressed as

$$q''_{\text{TE,c}} = \frac{-S_{\text{Si}} T_c I + I^2 R_{\text{ec}} + \eta I^2 R_{\text{lead}}}{A_{\text{TEC}}} \quad (5)$$

where S_{Si} is the Seebeck coefficient of silicon, α is the allocation factor showing how much silicon Joule heating flows into the microcooler, R_{Si} is the electric resistance of the microcooler [4], R_{ec} is the electric contact resistance, R_{lead} is the electric resistance of metal lead, η is the percentage of lead Joule heat entering into the microcooler, and A_{TEC} is the surface area of silicon microcooler. Nonuniform Joule heat inside the silicon substrate was calculated by thermal-electric coupling in our numerical simulation.

Doping concentration in silicon can have a profound influence on silicon microcooler performance, strongly affecting the Seebeck coefficient and the electrical resistivity, but only modestly affecting the thermal conductivity if the operating temperature is at room temperature or above. The thermoelectric properties of silicon material are strongly dependent on doping concentration but only modestly on the doping materials [13]. The variation of maximum hot spot cooling with doping concentration is presented in Fig. 8 for 100 μm thick chip and the electrical contact resistivity ρ_{c} ranging from $1 \times 10^{-7} \Omega \text{ cm}^2$ to $1 \times 10^{-4} \Omega \text{ cm}^2$, revealing that across the range of microcooler sizes studied, with increasing doping concentration the hot spot cooling increases until reaching a maximum value at a doping concentration of approximately 2×10^{19} and then decreases with further increase in the doping concentration. Increasing doping concentration results in lower electrical resistivity and, as a consequence, less Joule heating in the silicon microcooler. Unfortunately, the Seebeck coefficient of silicon also decreases with increasing doping concentration, which leads to less Peltier cooling. The competition between these two factors results in an optimum doping concentration at which the maximum cooling performance could be obtained.

The effect of microcooler size on cooling performance involves the interplay of thermoelectric cooling by the microcooler and thermal diffusion from the hot spot to the microcooler. Figure 9 displays this behavior and shows the temperature reductions at the hot spot for a wide range of microcooler sizes and silicon chips operating under the background and hot spot heat fluxes of 70 W/cm² and 680 W/cm², respectively. It is seen that the temperature reduction at the hot spot first increases with microcooler size and, after reaching the maximum value of 3.0°C for 600 $\mu\text{m} \times 600 \mu\text{m}$ microcooler (for 100 μm thick silicon), decreases with a further increase in the microcooler size. In the application of silicon microcoolers to hot spot remediation, the silicon chip plays multiple roles, functioning as a thermoelectric material, to provide on-chip cooling and, at the same time, as an electrical conductor to transfer electrons from the ground electrode to the microcooler, and as a thermal conductor to provide a diffusion path for the heat generated in the chip to the ambient. Therefore, the chip thickness influences

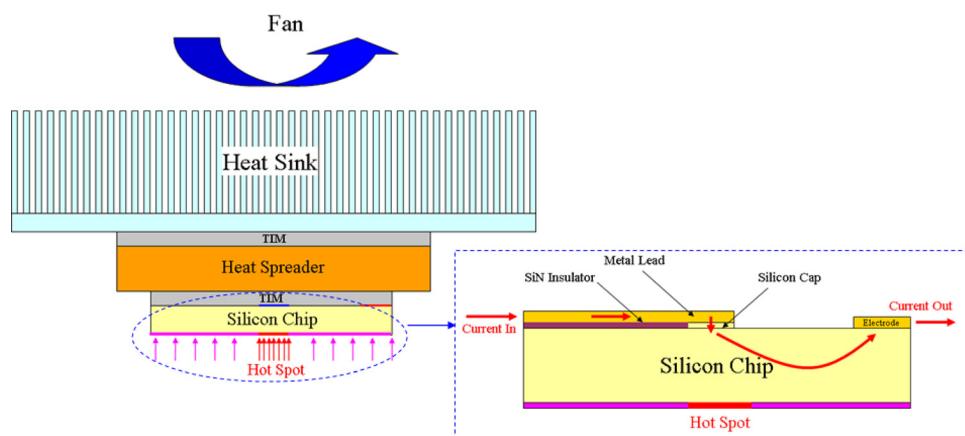


Fig. 7 Schematic of silicon thermoelectric microcooler. The arrows indicate the direction for electric current [4].

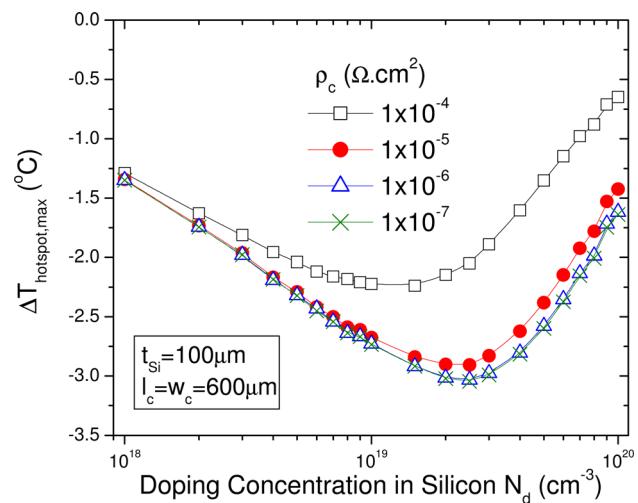


Fig. 8 Hot spot cooling as a function of boron doping concentration for various electrical contact resistivity. Microcooler size is $600 \mu\text{m} \times 600 \mu\text{m}$, silicon chip thickness is $100 \mu\text{m}$, and the hot spot size is $70 \mu\text{m} \times 70 \mu\text{m}$ with a heat flux of 680 W/cm^2 [4].

Joule heating distribution inside the chip, heat spreading from the hot spot, heat diffusion from the hot spot to the microcooler, and heat diffusion from the ground electrode, where Peltier heating occurs, to the hot spot. As the chip becomes thinner, the thermal resistance between the microcooler and the hot spot decreases, allowing the microcooler to achieve greater hot spot temperature reductions, e.g., 2.05°C to 3.03°C as the chip thickness decreases from $500 \mu\text{m}$ to $100 \mu\text{m}$, for the conditions of Fig. 9. It was found that hot spot size and heat flux also have some effect on cooling performance. For example, the maximum temperature reduction at the hot spot increases from 3.03°C for $70 \mu\text{m} \times 70 \mu\text{m}$ hot spot with 680 W/cm^2 heat flux to 3.90°C for $400 \mu\text{m} \times 400 \mu\text{m}$ hotspot with 1000 W/cm^2 heat flux, primarily because of the effect of the higher chip temperature (150°C versus 105°C) on Peltier cooling power.

3.3 Si/SiGe Superlattice Microcooler. SiGe/Si superlattices have been investigated extensively for more than 15 years due to their unique nanostructure, with very low thermal conductivity and thus high thermoelectric figure of merit (ZT) value. However, there are few reports of the on-chip hot spot cooling potential of SiGe/Si microcoolers when integrated into electronic packaging [14,15]. Bar-Cohen, Shakouri, and co-workers pioneered this

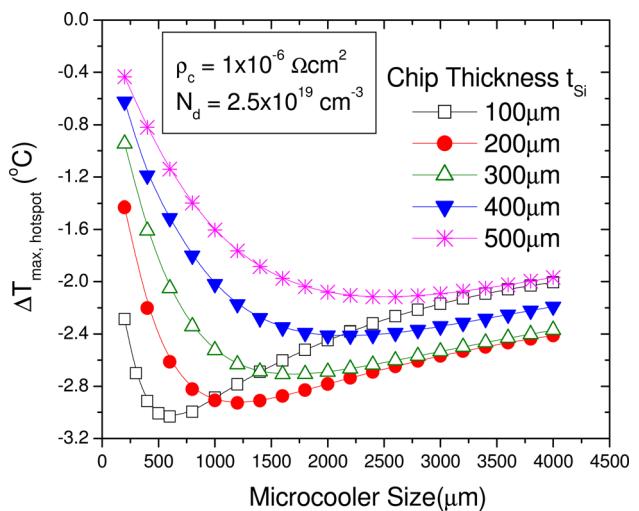


Fig. 9 In-plane silicon thermoelectric hot spot cooling as a function of microcooler size and chip thicknesses. Silicon chip thickness is $100 \mu\text{m}$, and the hot spot size is $70 \mu\text{m} \times 70 \mu\text{m}$ with a heat flux of 680 W/cm^2 [4].

study using the configuration shown in Fig. 10. The corresponding temperature profile along the bottom (active surface) of the silicon chip ($11 \text{ mm} \times 13 \text{ mm} \times 50 \mu\text{m}$) is illustrated in Fig. 11 [15].

The net cooling effect can then be expressed as an internal heat flux boundary condition on the surface of the microcooler given by

$$q''_{TE,c} = \frac{-S_{SiGe}T_{c,1}I + (S_{SiGe} - S_{Si})T_{c,2}I + I^2R_{ec} + \eta I^2R_{lead}}{A_{TEC}} \quad (6)$$

where S_{Si} and S_{SiGe} are the Seebeck coefficients of silicon and SiGe superlattice, respectively. $T_{c,1}$ and $T_{c,2}$ are the temperatures at SiGe/metal and SiGe/silicon interface, respectively. R_{ec} is the electric contact resistance, R_{lead} is the electric resistance of metal lead, η is the percentage of lead Joule heat entering into the microcooler, and A_{TEC} is the surface area of SiGe/Si microcooler. In the numerical simulation, Joule heat from SiGe and Silicon was calculated by thermal-electric coupling.

It is observed from Fig. 11 that when a $3 \mu\text{m}$ thick Si/SiGe superlattice cooler is integrated onto the top of the silicon chip with an optimized applied current of 0.6 A , the hot spot temperature is reduced by 1.8°C , corresponding to an 80% reduction of the local temperature rise produced by the 680 W/cm^2 , $70 \mu\text{m} \times 70 \mu\text{m}$ hot spot. Figure 12 shows the heat flux profile around the

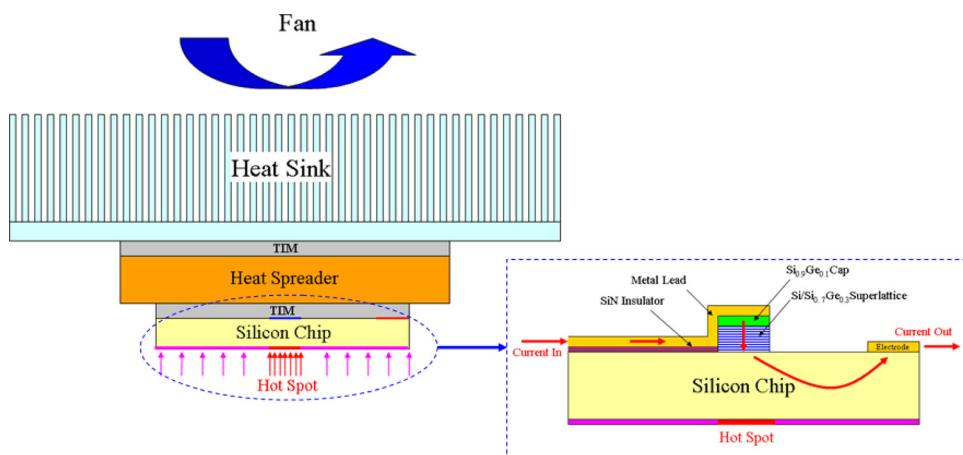


Fig. 10 Schematic of Si/SiGe superlattice microcooler integrated on the backside silicon chip for hot spot cooling (The arrows indicate the direction for electric current) [15]

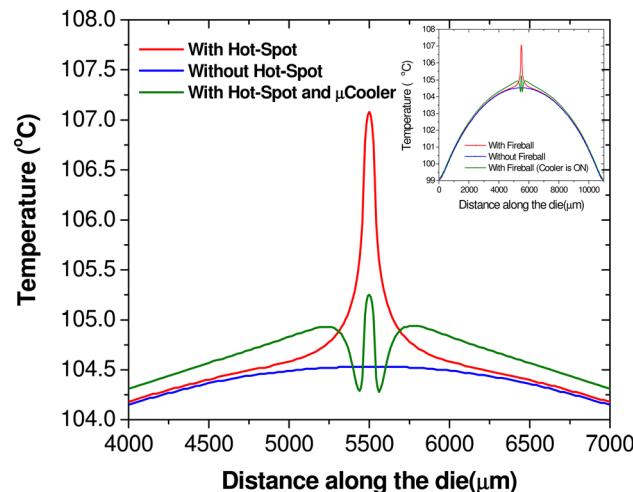


Fig. 11 Temperature profile on the bottom of silicon chip. The hot spot size is $70 \mu\text{m} \times 70 \mu\text{m}$ with a heat flux of 680 W/cm^2 , the chip thickness is $50 \mu\text{m}$, and SiGe/Si microcooler size is $150 \mu\text{m} \times 150 \mu\text{m}$ [15].

hot spot and the Si/SiGe microcooler. It can be seen that when the microcooler is not powered, heat spreading from the hot spot dominates while when the microcooler is operating, the heat flux leaving the hot spot is redirected toward the microcooler. Their studies revealed that for best effect, the TEC microcooler should substantially exceed the hot spot size, thus, serving to not only directly cool the hot spot but also indirectly reduce the temperature of the surrounding silicon. Recently, Litvinovitch and Bar-Cohen made comparisons of SiGe/Si TEC and in-plane silicon TEC using finite element simulation [16]. In their research, the effect of superlattice thickness, silicon substrate thickness,

microcooler size, hot spot size, and hot spot heat flux were systematically investigated. It was found that while the top surface of the superlattice always achieves the lower local temperatures, hot spot cooling does not benefit from the use of a silicon microcooler with an integrated SiGe/Si superlattice.

3.4 Bi₂Te₃ Superlattice Microcooler. Recently Chowdhury et al. [7] at Intel integrated a $100 \mu\text{m}$ -thick Bi₂Te₃-based superlattice microcooler into an electronic package to investigate its hot spot cooling capability and the test vehicle is illustrated in Fig. 13. The silicon chip size is $10.9 \text{ mm} \times 12.9 \text{ mm}$ with a background heat flux of 42.7 W/cm^2 and the hot spot size is $400 \mu\text{m} \times 400 \mu\text{m}$ with a heat flux of 1250 W/cm^2 , which corresponds to 60 W background heat and 2 W hot spot heat dissipation. The superlattice TEC consists of p-type Bi₂Te₃/Sb₂Te₃ and n-type Bi₂Te₃/Bi₂Te_{2.83}Se_{0.17} that were grown by metal–organic chemical vapor deposition on GaAs substrates with the Seebeck coefficient of $301 \mu\text{V/K}$, electrical resistivity of $1.08 \times 10^{-5} \Omega \text{ m}$, and thermal conductivity of 1.2 W/m K . These values give an intrinsic ZT value of ~ 2.1 at 27°C ambient temperature. The TEC, with a lateral dimension of $3.5 \text{ mm} \times 3.5 \text{ mm}$ and a total thickness of $100 \mu\text{m}$, was then mounted on a copper heat spreader and embedded into a layer of thermal interface material (a thermal grease with an effective thermal conductivity of 1.75 W/m K), when integrated into the electronic package.

Figure 14 shows the experimental data of hot spot temperatures when the TEC is integrated onto the backside of silicon chip. It is interesting to find that—for this particular packaging configuration—even when the TEC is not powered, there is a 7.6°C “passive cooling” of the hot spot. This is, as noted by the authors, because the thermoelectric cooler has a higher effective thermal conductance than the volume of thermal interface material that it replaces. The thermal conductivity of the Bi₂Te₃-based superlattice material, measured as $\sim 1.2 \text{ W/m K}$, is less than that of the thermal grease ($\sim 1.75 \text{ W/m K}$). However, due to the highly conductive metal

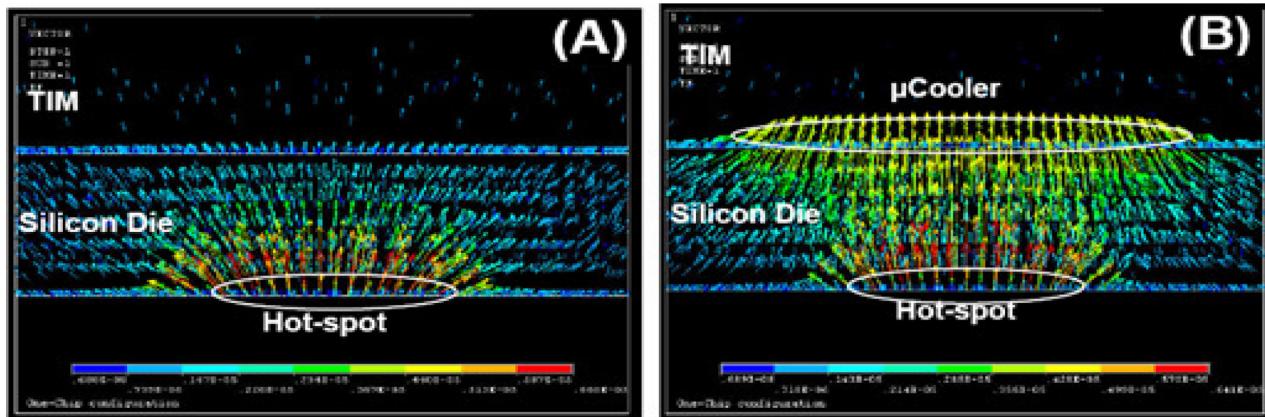


Fig. 12 Hot spot heat flux distribution (a) without microcooler and (b) with microcooler powered with 0.6 A . The hot size is $70 \mu\text{m} \times 70 \mu\text{m}$ with a heat flux of 680 W/cm^2 , silicon chip thickness is $50 \mu\text{m}$, and SiGe/Si microcooler size is $150 \mu\text{m} \times 150 \mu\text{m}$ [15].

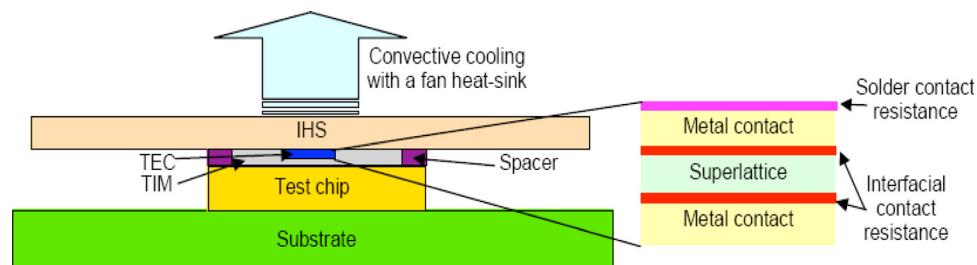


Fig. 13 Cross section of the electronic test package with a Bi₂Te₃-based superlattice TEC attached to the underside of the integrated heat spreader [7]

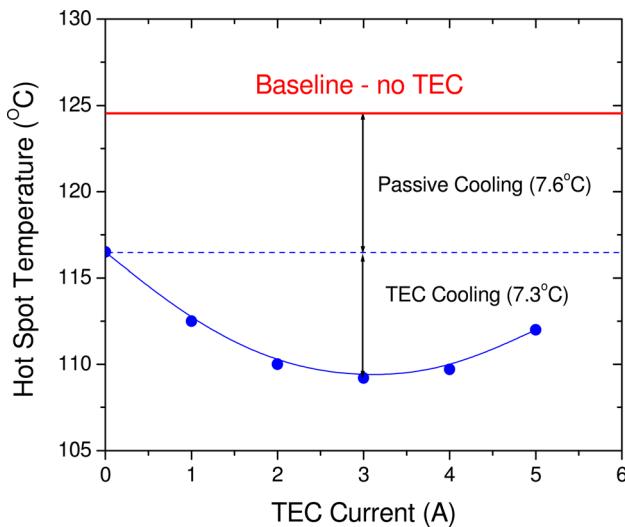


Fig. 14 Measured hot spot temperature on the chip as a function of current through the thermoelectric cooler (TEC). The hot spot size is $400 \mu\text{m} \times 400 \mu\text{m}$ with a heat flux of 1250 W/cm^2 [7].

contact pads, the effective thermal conductivity of the TEC device can reach around 17 W/m K , thus reducing the TEC conductance relative to the thermal grease TIM. More importantly, Fig. 14 reveals that when the TEC is activated, the measured hot spot temperature decreased further and reached a minimum, at an applied current of 3 A , with a TEC “active cooling” of 7.3°C . Thus, a total (passive and active) localized cooling of 14.9°C can be achieved with the use of the TEC. The authors noted the strong dependence of the cooling capability of such TECs on the interface of thermal resistance and electrical resistance. In addition, as the TEC is thermally attached to the chip with thermal grease, the thickness and thermal conductivity of the grease are the critical factors to the hot spot cooling performance.

4 On-Chip Hot Spot Cooling Using Microgap Cooler

Direct liquid cooling techniques, which allow for direct contact between an inert dielectric liquid and the surface of the chip and thus eliminate the TIM, hold great promise for hot spot driven thermal management of IC’s. Moreover, use of phase-change processes, including pool boiling, gas-assisted evaporative cooling, jet impingement, and spray cooling, exploit the latent heat of these liquids to reduce the required mass flow rates and can provide the added advantage of inherently high heat transfer coefficients

[17,18]. Recently, Bar-Cohen et al. [19] proposed the use of microgap coolers to achieve a volume-efficient application of direct liquid cooling, while providing high heat transfer coefficients—in the range needed to control the temperature of on-chip hot spots—on the back of the chip. In a microgap cooler, as shown in Fig. 15, a single microchannel is created above the silicon chip and the liquid is pumped through the channel, thus removing the heat dissipated from the hot spot as well as from the chip. Compared with a more conventional microchannel cooler, which needs to be attached with a TIM to the chip/substrate, microgap coolers require no attachment and no micromachining and thus could be a very attractive cooling approach for on-chip hot spot remediation.

The test results for the $210 \mu\text{m}$ gap cooler with FC72 as coolant are shown in Fig. 16. In these experiments, the mass flux was changed from $130 \text{ kg/m}^2 \text{ s}$ to $660 \text{ kg/m}^2 \text{ s}$ in steps of $130 \text{ kg/m}^2 \text{ s}$ and the corresponding inlet liquid velocity was $0.0794, 0.159, 0.238, 0.317$, and 0.397 m/s . The average heat transfer coefficient was found to generally display a parabolic variation with the heat flux, increasing toward a peak value of approximately $8 \text{ kW/m}^2 \text{ K}$ and then decreasing with further increases of heat flux, in general agreement with the observations for the larger $500 \mu\text{m}$ gap cooler. The lower mass flux data display no positive slope branch in its locus and the heat transfer coefficients for mass fluxes of $130 \text{ kg/m}^2 \text{ s}$ and $260 \text{ kg/m}^2 \text{ s}$ experience a continuous decline—with a short plateau—as the heat flux increases.

4.1 Two-Phase Flow Regimes. To determine the expected range of heat transfer coefficients and the most appropriate heat transfer correlation to be used, it is important to establish the two-phase flow regimes expected to prevail in the microgap cooler. Figure 17 displays a Taitel and Dukler flow regime map developed in this study for FC-72 flowing in a typical $110 \mu\text{m}$ gap cooler, identifying the superficial liquid and vapor velocities associated with each of the four primary flow regimes [20,21]. As displayed in Fig. 17, two-phase flow in the microgap cooler can be expected to fall primarily into the intermittent regime—at low qualities—and the annular flow regime—at higher qualities. In a recent study [19], Bar-Cohen and Rahim’s analysis of a large database of two-phase heat transfer coefficients in microgap channels have shown the Shah correlation [22] to best fit data in the intermittent flow regime, while the Chen correlation [23] to best fit annular flow data, with a standard deviation of 32% and 24%, respectively.

4.2 Characteristic Heat Transfer Coefficient Variation. The inherent complexity of two-phase transport in microgap coolers can be expected to lead to substantial variations in the heat transfer coefficient as the vapor quality increases from near-zero

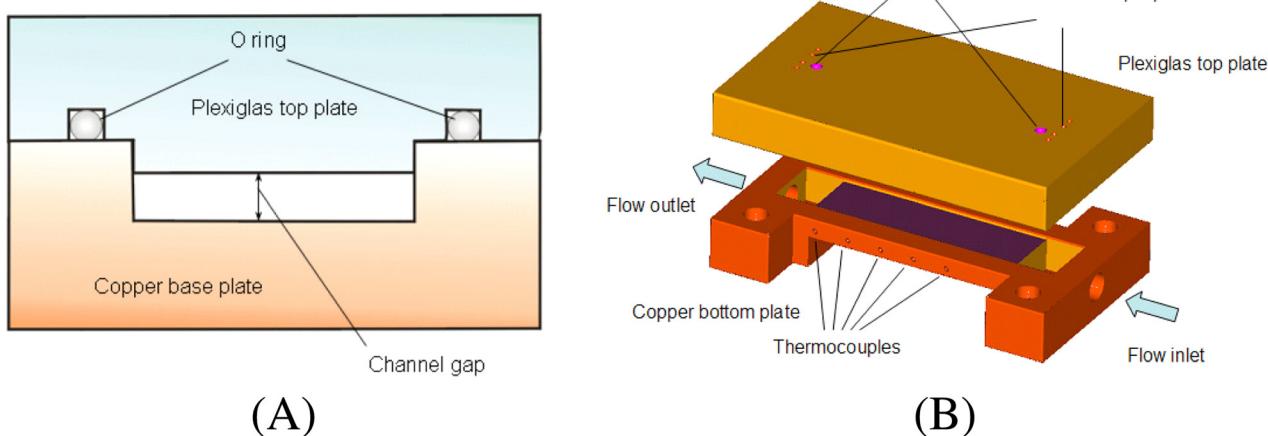


Fig. 15 Structure of microgap cooler for on-chip hot spot cooling [19]

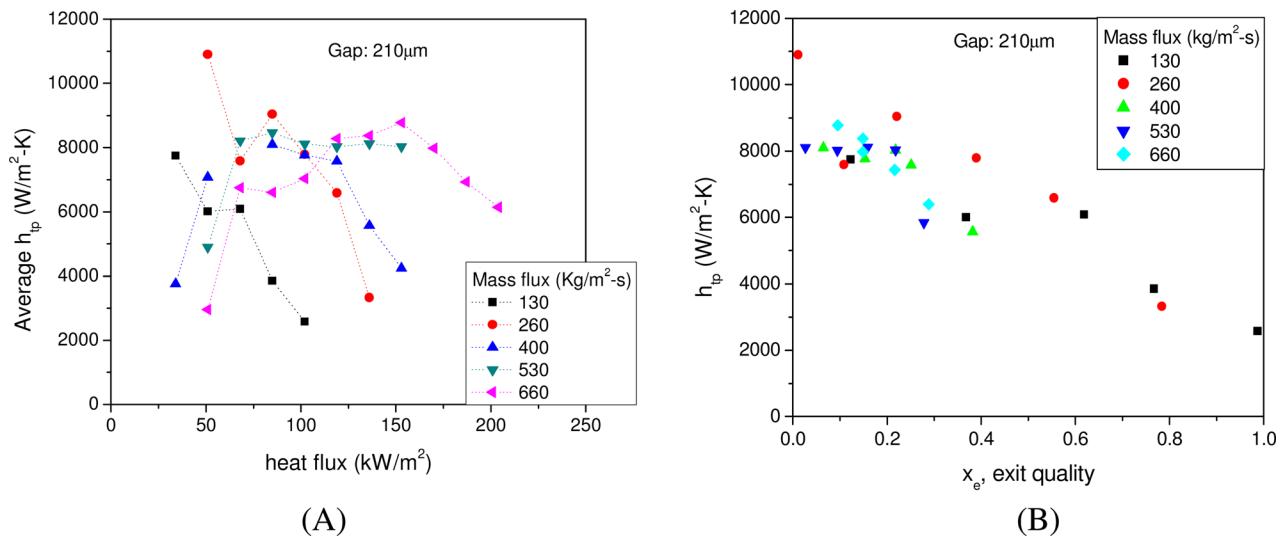


Fig. 16 Average heat transfer coefficient in 210 μm gap cooler: (a) variation with heat flux and (b) variation with exit quality [19]

(saturated liquid) to near-unity (saturated vapor) conditions. Referring to Fig. 18, the experimental two-phase heat transfer coefficients obtained in the studies by Yang and Fujita [24] and Cortina-Diaz and Schmidt [25], respectively, provide clear evidence of a possible M-shaped variation with thermodynamic quality. The empirical heat transfer coefficients are seen to rise steeply from the values attained for slightly subcooled conditions to a local maximum at a near-zero quality, after which the heat transfer coefficient values are seen to fall with higher quality toward a plateau-like region, only to reach another inflection point at moderate qualities (15–40%), where the curve once again attains a positive slope. Beyond this point, the heat transfer coefficient rises with increasing quality until it reaches a second local peak, at elevated quality values, of approximately 50% and 75%, respectively, for the two data sets. For even higher vapor qualities, the heat transfer coefficient deteriorates until reaching the minimum reported values, at qualities approaching unity, generally associated with observed dryout conditions. The behavior captured in the characteristics M-curve for the two-phase heat transfer coefficient can be understood to reflect the underlying

thermophysics of two-phase phenomena in these miniature channels [20].

Regrettably, it is rare to find in the literature data sets of the type shown in Fig. 18 that provide microchannel heat transfer coefficients over the full range of qualities. Rather, many of the examined data sets span only a modest range of qualities and, consequently, display only segments of the full M-shaped characteristic curve. This behavior is illustrated in Fig. 19 for our microgap cooler study. It can be easily seen that, at any fixed value of exit quality, the smallest gap, i.e., 110 μm , nearly always displayed the highest average heat transfer coefficients, relative to the 210 μm and 500 μm channels, ranging from 10 $\text{kW/m}^2 \cdot \text{K}$ for a mass flux of 1020 $\text{kg/m}^2 \cdot \text{s}$, at an exit quality of 10.5%, to 3.6 $\text{kW/m}^2 \cdot \text{K}$ for 260 $\text{kg/m}^2 \cdot \text{s}$ at an exit quality of nearly unity (99%). The thinner liquid films expected to develop in the narrower microgap channels, most notably in the dominant annular flow regime, are most likely responsible for this behavior. It may also be seen that for the narrower channels, at a fixed value of mass flux, the heat transfer coefficient decreases steeply at the lowest values of exit quality, then enters a plateau region, before again decreasing

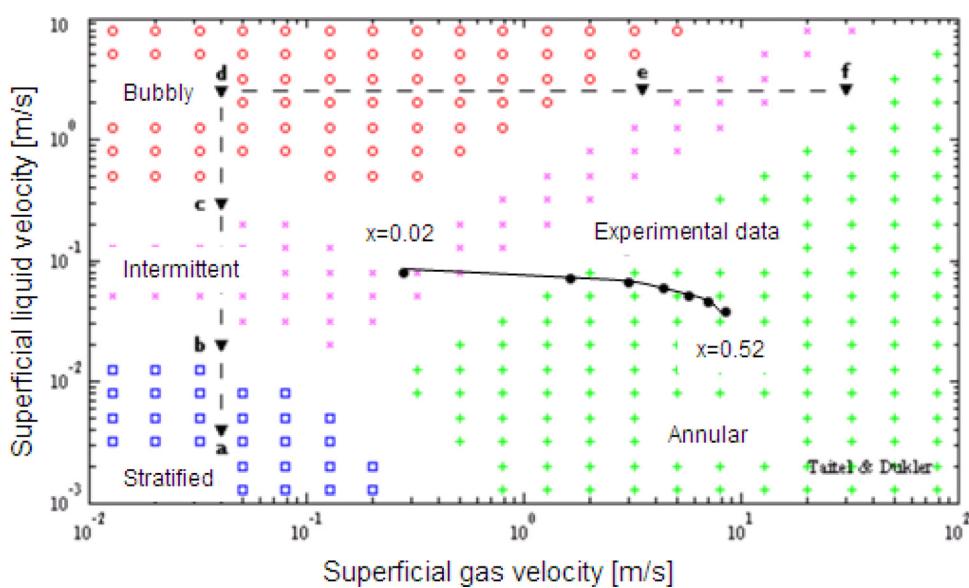


Fig. 17 Taitel and Dukler two-phase flow regime map for FC-72 flowing in a 110 μm microgap channel [$G = 133.3 \text{ kg/m}^2 \cdot \text{s}$, $D_h = 0.218 \text{ mm}$, $q'' = 16.8 \text{ kW/m}^2$] [19]

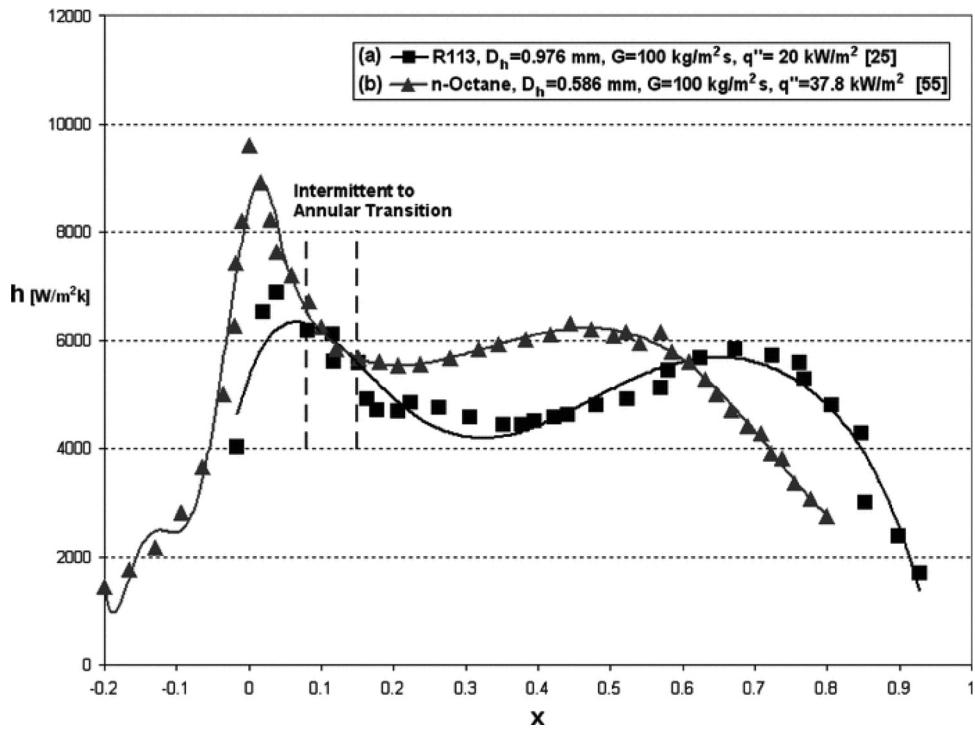


Fig. 18 Characteristic heat transfer coefficient curve in microgap channel [20]

steeply as the exit quality increases toward unity. This nonmonotonic heat transfer coefficient variation is reminiscent of the characteristic M-shaped locus shown in Fig. 18. But the absence—in the present study—of the local quality and heat transfer coefficients may mask the steep heat transfer coefficient increase in the channel segment just before local dryout begins.

4.3 Application of Liquid Cooling to Hot Spot Remediation. To assess the possibility and efficacy of microgap cooler for thermal management of hot spots, it is instructive to simulate the thermal performance of a microprocessor chip cooled by the microgap coolers. A 10 mm × 10 mm silicon chip, 500 μm thick, dissipating a uniform heat flux of 100 W/cm^2 across nearly all the active chip area, serves as the test vehicle for this simulation. The chip is assumed to possess a central, circular hot spot, varying from 100 μm to 400 μm in diameter and dissipating between 1000 W/cm^2 and 2000 W/cm^2 . It is further assumed that the thermal

conductivity of the silicon chip is invariant at 125 W/mK , that it is cooled from the back surface (opposite to that of the active circuitry) with heat transfer coefficients that vary from 5 $\text{kW/m}^2 \text{ K}$ to 20 $\text{kW/m}^2 \text{ K}$, reflective of the values that can be potentially achieved with microgap coolers [19]. For simplicity, the fluid is assumed to be at 0 $^\circ\text{C}$.

Figure 20 presents the three-dimensional temperature profile on the active face of the silicon chip for a baseline microgap-cooled chip configuration with a 400 μm hot spot, generating a 2 kW/cm^2 heat flux. As it can be seen, when this baseline chip, with a very severe hot spot, is cooled by a microgap cooler with an h equal to 10 $\text{kW/m}^2 \text{ K}$, it experiences an elevated average temperature of approximately 130 $^\circ\text{C}$ and a significant hot spot with a maximum temperature of 163 $^\circ\text{C}$, or some 33 $^\circ\text{C}$ above the average chip temperature. The average and peak temperatures for various other combinations of the specified parameters are shown in Tables 2 and 3.

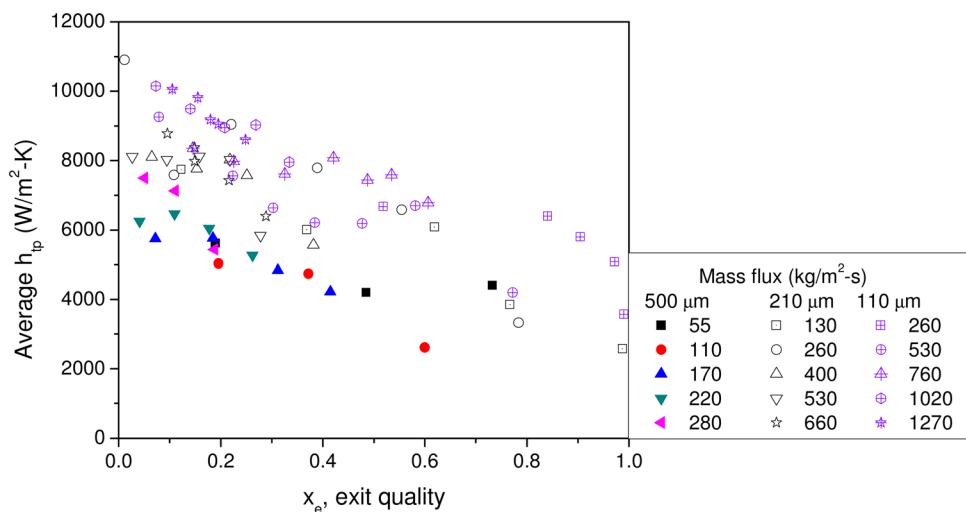


Fig. 19 Microgap size effect on the two-phase heat transfer coefficient [19]

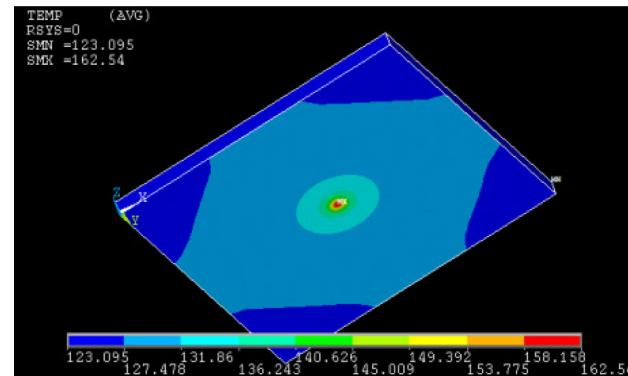


Fig. 20 Three-dimensional temperature profile for microgap cooling of $10\text{ mm} \times 10\text{ mm} \times 0.5\text{ mm}$ chip with a background heat flux of 100 W/cm^2 . The circular hot spot ($d_{\text{hotspot}} = 400\text{ }\mu\text{m}$) has a heat flux of 2 kW/cm^2 , the effective heat transfer coefficient applied on the chip surface is $10\text{ kW/m}^2\text{ K}$ [26].

Tables 2 and 3 present the results for a hot spot diameter of $100\text{ }\mu\text{m}$ and $400\text{ }\mu\text{m}$, respectively, with various hot spot heat fluxes and a range of heat transfer coefficients associated with the microgap coolers. In these tables, the first and second columns present the hot spot flux (q''_{hs}) and convective coefficients (h), respectively, while the next three columns provide the average temperature on the active side of the chip (T_{chip}), the average temperature on the convective cooled (back) side of the chip (T_{conv}), and the average hot spot temperatures ($T_{\text{hs,ave}}$). The last column in Tables 2 and 3 presents the maximum temperature on the active side of the silicon chip ($T_{\text{hs,max}}$). Not surprisingly, the average chip temperature (on both the active and wetted surfaces) is seen to vary directly with the heat transfer coefficient, while the on-chip hot spot temperature rise is conduction limited and—for the fixed chip geometry and thermal conductivity—is driven by the heat flux and size of the hot spot. Thus, as seen in Table 3, while raising the heat transfer coefficient to $20\text{ kW/m}^2\text{ K}$ lowers the chip average temperature to $77.5\text{ }^\circ\text{C}$, the on-chip temperature rises ($T_{\text{hs,max}} - T_{\text{chip}}$) for a 1 kW/cm^2 , $400\text{ }\mu\text{m}$ hot spot, remains at approximately $15\text{ }^\circ\text{C}$ across the range of heat transfer coefficients from 5 kW to $20\text{ kW/cm}^2\text{ K}$. However, since the peak chip temperature is established by the superposition of these two effects, any reduction in the average chip temperature has a salutary effect on the peak chip temperature.

Interestingly, the on-chip temperature rise—of the hot spot center relative to the chip average—can be seen to vary almost directly with the product of the heat flux and diameter, yielding a ninefold increase from $3.6\text{ }^\circ\text{C}$ for a $100\text{ }\mu\text{m}$, 1 kW/cm^2 hot spot to $32.4\text{ }^\circ\text{C}$ for a $400\text{ }\mu\text{m}$, 2 kW/cm^2 hot spot. Due to the superposition of the convective and conductive effects, it may also be noted that while a large change (approximately 50%) in the maximum excess temperature results from increasing the microgap heat transfer coefficient from $5\text{ kW/m}^2\text{ K}$ to $10\text{ kW/m}^2\text{ K}$, further increases to $20\text{ kW/m}^2\text{ K}$ only reduces the maximum temperature rise by approximately 30%.

Table 2 Temperatures for $100\text{ }\mu\text{m}$ hot spot diameter for various heat flux and cooling conditions [26]

$q''_{\text{hs}}(\text{W/cm}^2)$	$h(\text{W/m}^2\text{ K})$	$T_{\text{chip}}(^\circ\text{C})$	$T_{\text{conv}}(^\circ\text{C})$	$T_{\text{hs,ave}}(^\circ\text{C})$	$T_{\text{hs,max}}(^\circ\text{C})$
1000	20,000	76.2	74.2	78.9	79.7
1000	10,000	126.2	124.2	129.0	129.7
1000	5000	226.3	224.3	229.1	229.8
2000	20,000	76.4	74.4	82.2	83.8
2000	10,000	126.5	124.6	132.3	134.0
2000	5000	226.7	224.7	232.5	234.1

Table 3 Temperatures for $400\text{ }\mu\text{m}$ hot spot diameter for various heat flux and cooling conditions [26]

$q''_{\text{hs}}(\text{W/cm}^2)$	$h(\text{W/m}^2\text{ K})$	$T_{\text{chip}}(^\circ\text{C})$	$T_{\text{conv}}(^\circ\text{C})$	$T_{\text{hs,ave}}(^\circ\text{C})$	$T_{\text{hs,max}}(^\circ\text{C})$
1000	20,000	77.5	75.6	89.1	92.2
1000	10,000	128.2	126.4	140.2	143.3
1000	5000	229.4	227.6	241.6	244.7
2000	20,000	79.2	77.5	103.7	110.3
2000	10,000	130.7	129.0	155.9	162.5
2000	5000	233.2	231.6	259.0	265.6

5 Conclusions

This paper addresses on-chip hot spot cooling which has become one of the most active and challenging domains in the thermal management of nanoelectronic devices and packages. The physical phenomena underpinning the most promising on-chip thermal management approaches are described in this paper with an attention devoted to thermoelectric microcoolers and two-phase microgap coolers for hot spot remediation and thermal management. It was demonstrated that, with proper thermal, electrical, and geometric optimizations, minicontact enhanced thermoelectric coolers can yield hot spot temperature reductions in excess of $17\text{ }^\circ\text{C}$ at a $400\text{ }\mu\text{m} \times 400\text{ }\mu\text{m}$ 1250 W/cm^2 hot spot but are vulnerable to the deleterious effects of contact resistance. Microscaled thin film in-plane silicon microcoolers monolithically grown on the back of silicon chips, and nanostructured bismuth-telluride superlattice microcooler grown on a heat spreader and mounted on the back of the chip, are similarly found to provide effective thermal management for high heat flux spots, and to be capable of neutralizing the local temperature rise for a large variety of high flux hot spots. Experimental and modeling results for microgap coolers, relying on the boiling and evaporation of a dielectric liquid flowing in a miniature gap at the back of the chip, suggest that this cooling technique, which eliminates the solid–solid thermal interface resistance and provides direct contact between chemically inert, dielectric fluids and the back surface of an active electronic component, could provide local and global heat transfer coefficients comparable to single-phase water flow and thus meet many of the most demanding nanoelectronics thermal management challenges including severe on-chip hot spots.

References

- [1] Shakouri, A., and Zhang, Y., 2005, "On Chip Solid State Cooling for Integrated Circuits," *J. IEEE Trans. Compon. Packag. Technol.*, **28**(1), pp. 65–69.
- [2] Tritt, T. M., 2006, "Thermoelectric Materials, Phenomena, and Applications: A Bird's Eye View," *MRS Bull.*, **31**(3), pp. 188–194.
- [3] Bar-Cohen, A., and Watwe, A., 2001, "Fundamentals of Thermal Management," *Fundamentals of Microsystems of Package*, R. R. Tummala, ed., McGraw-Hill, New York.
- [4] Wang, P., and Bar-Cohen, A., 2007, "On-Chip Hot Spot Cooling Using Silicon-Based Thermoelectric Microcooler," *J. Appl. Phys.*, **102**(3), p. 034503.
- [5] Wang, P., Bar-Cohen, A., and Yang, B., 2009, "Mini-Contact Enhanced Thermoelectric Coolers for On-Chip Hot Spot Cooling," *Heat Transfer Eng.*, **30**(9), pp. 736–743.
- [6] Yang, B., Wang, P., and Bar-Cohen, A., 2007, "Mini-Contact Enhanced Thermoelectric Cooling of Hot Spot in High Power Devices," *IEEE Trans. Compon. Packag. Technol. Part A*, **30**, pp. 432–438.
- [7] Chowdhury, I., Prasher, R., Lofgreen, K., Chrysler, G., Narasimhan, S., Mahajan, R., Koester, D., Alley, R., and Venkatasubramanian, R., 2008, "On-Chip Cooling by Superlattice-Based Thin-film Thermoelectrics," *Nat. Nanotechnol.* **4**, pp. 235–238.
- [8] Wang, P., and Bar-Cohen, A., 2007, "Analysis and Simplified Thermal Model of Silicon Microcooler for On-Chip Hot Spot Thermal Management," Proceedings of Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition (InterPack'07), Vancouver, Canada, July 8–12, 2007. Paper No. IPACK2007-33940.
- [9] Wang, P., Bar-Cohen, A., and Yang, B., 2006, "Impact of Thermal Contact Resistance on Hot Spot Cooling Using Mini-Contact Enhanced Thermoelectric Coolers," Proceedings of IMAPS Thermal Management 2006, Palo Alto, CA, Sept. 10–13 (CDROM).
- [10] Wang, P., Bar-Cohen, A., and Yang, B., 2006, "Multiple Silicon-Based Thermoelectric Microcoolers for Hot Spot Thermal Management," Proceedings of the 13th International Heat Transfer Conference (IHTC-13), Sydney, Australia, Aug. 13–18, Paper No. CND-09.

- [11] www.thermion-company.com
- [12] Wang, P., Bar-Cohen, A., and Yang, B., 2006, "Analytical Modeling of Silicon Thermoelectric Microcooler," *J. Appl. Phys.*, **100**(1), p. 14501.
- [13] Herwaarden, A. W., and Sarro, P. M., 1986, "Thermal Sensors Based on the Seebeck Effect," *Sens. Actuators*, **10**, pp. 321–346.
- [14] Zhang, Y., Zeng, G., Shakouri, A., Wang, P., and Bar-Cohen, A., 2005, "Experimental Demonstration of Microrefrigerator Flip-chip Bonded With IC Chips for Hot Spot Thermal Management," Proceedings of the Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition (InterPack'05), San Francisco, CA, July 17–22, Paper No. IPACK2005-73466.
- [15] Wang, P., Bar-Cohen, A., Yang, B., Zhang Y., and Shakouri, A., 2005, "Thermoelectric Microcooler for Hot Spot Thermal Management," Proceedings of the Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition (InterPack'05), San Francisco, CA, July 17–22, Paper No. IPACK2005-73244.
- [16] Litvinovitch, V., Wang, P., and Bar-Cohen, A., 2008, "Impact of Integrated Superlattice μ -TEC Structure on Hot Spot Remediation," Proceedings of the 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic System, Orlando, FL (ITHERM'08), pp. 1231–1241.
- [17] Bergles, A. E., and Bar-Cohen, A., 1994, "Immersion Cooling of Digital Computers," *Cooling of Electronic Systems*, S. Kakac, H. Yuncu, and K. Hijikata, eds., Kluwer Academic Publishers, Boston, MA, pp. 539–621.
- [18] Bergles, A. E., and Bar-Cohen, A., 1990, "Direct Liquid Cooling of Microelectronic Components," *Advances in Thermal Modeling of Electronic Components and Systems*, A. Bar-Cohen and A. D. Kraus, eds., ASME, New York, pp. 241–250.
- [19] Kim, D., Rahim, E., Bar-Cohen, A., and Han, B., 2010, "Direct Submount Cooling of High-Power," *IEEE Trans. Compon. Packag. Technol. Part A* **33**, pp. 698–712.
- [20] Bar-Cohen A., and Rahim, E., 2009, "Modeling and Prediction of Two-Phase Micropip Channel Heat Transfer Characteristics," *Heat Transfer Eng.*, **30**, pp. 601–625.
- [21] Taitel, Y., and Dukler, A. E., 1976, "A Model for Prediction of Flow Regime Transitions in Horizontal and Near Horizontal Gas-liquid Flow," *AIChE J.*, **22**, pp. 47–55.
- [22] Shan, M. M., 1982, "Chart Correlation for Saturated Boiling Heat Transfer: Equations and Further Study," *ASHRAE Trans.*, **88**, pp. 185–196.
- [23] Chen, J. C., 1967, "Correlation for Boiling Heat Transfer to Saturated Fluids in Convective Flow," *Ind. Eng. Chem. Process Des. Develop.*, **5**(3), pp. 322–329.
- [24] Yang, Y., and Fujita, Y., 2004, "Flow Boiling Heat Transfer and Flow Pattern in Rectangular Channel of Mini-Gap," Proceedings of the 2nd International Conference on Microchannels and Minichannels, New York, Paper No. ICMM2004-2383.
- [25] Cortina-Diaz, M., and Schmidt, J., 2006, "Flow Boiling Heat Transfer of n-Hexane and n-Octane in a Minichannel," Proceedings of the 13th International Heat Transfer Conference, Sydney, Australia.
- [26] Bar-Cohen, A., Arik, M., and Ohadi M., 2009, "Direct Liquid Cooling of High Flux Micro and Nano Electronic Components," *Proc. IEEE*, **94**(8), pp. 1549–1570.