University of Windsor
Department of Electrical and Computer Engineering
ELEC-4430 Embedded System Design Lab Project 1
Winter 2022
Instructor: Dr. M. Khalid
Due: Monday February 28, 2022 (by 7 pm)

You will design, model and simulate a Fibonacci Number generator with VHDL and Intel Quartus Prime Lite CAD tool. You will implement it on the **Intel DE10-Lite FPGA Board** and its character display module. Following points describe the functionality of the number generator:

1. The Fibonacci Number generator generates N elements of the Fibonacci series entered by the user using the switches present on the DE10-Lite board (Signal N (4 downto 0)). Signal N is in the range 1-30.
2. The numbers are then displayed one after the other with some delay on the six 7-segment displays (output signal SEVEN_SEG_DISPLAY (41 downto 0)) of the DE10-Lite FPGA board when the display control input switch, DC_IN, is set to high.
3. When the display control input, DC_IN, is set to low, user can traverse the Fibonacci series using a switch and a pushbutton present on the board such that, when the switch(S) is high, one press of push button (signal PB) traverses one step in the Fibonacci series in the ascending order and when the switch(S) is low, one press of push button (signal PB) traverses one step in the Fibonacci series in the descending order.
4. Also, the Fibonacci number generator allows to start from the first element of the series using the START switch.

START	DC_IN	S	PB	SEVEN_SEG_DISPLAY
1	X	X	X	Displays the first element of the Fibonacci series
0	1	X	X	Traverses the Fibonacci series in ascending order starting from the first element with delay between each display: 1 => 1 => 2 => 3 => 5 ... =>Nth element
0	0	High	Low	Traverses one step in the Fibonacci series in ascending order from the currently displayed element 3 => 5
0	0	Low	Low	Traverses one step in the Fibonacci series in descending order from the currently displayed element. 5 => 3
0	0	X	High	No operation, Fibonacci count retains it's previous value.

Table 1: Functionality of the Fibonacci Generator.

Following table describes the Input and output signals for the Fibonacci number generator:

Signal	Number of bits	Direction
N	5 bits wide	Input
DC_IN	1 bit wide	Input
PB	1 bit wide	Input
S	1 bit wide	Input
START	1 bit wide	Input
SEVEN_SEG_DISPLAY	42 bits wide	Output

Table 2: Input/Output for the Fibonacci Number Generator

Report:

You will need to write a 3 to 6 page report for this project. Describe how you implemented the Fibonacci Number generator and what problems or difficulties you have encountered, and how you solved them. Make sure to include the Simulation Results showing an example of each operation listed in Table 1.

Useful Hints:

- You can simulate the operation of your VHDL code by using Quartus Simulator Tool. This tool is an excellent way to verify that your code is operating as you planned and according to the specs. You only need to show the GA, simulation of I/O signals of the Fibonacci number generator, not the display.
- Use the “ieee.std_logic_unsigned.all” and “ieee.numeric_std.all” library for easy implementation of arithmetic operations.
- You can save the current state (comprising of the current Fibonacci number being displayed, the previous Fibonacci number and the count (ranging from 1 to N) of the current Fibonacci number) of the Fibonacci series counter in a storage element by declaring a signal of custom type (Declared using the ‘type’ keyword).
- The DE10-Lite FPGA board manual is available on the course website. Please read it carefully. As senior engineering students, you are expected to be able to study and understand engineering data sheets effectively.
- It is highly recommended that each group writes the VHDL code BEFORE coming to the lab. This will save significant amount of their time.
- GA will check the results of simulation and functionality of the design on the DE10-Lite FPGA-boards. After that GA will ask oral questions related to the project to each team member. Please ensure that each member of the group have thorough understanding of the project. All group members should participate in developing the code and simulation.
- You will be marked on the functionality of implementation, simulation, oral questions and report.
- Each group MUST email their VHDL code to the instructor and GAs.
- Late submissions will not be accepted.
- Copied code will result in a grade of 0 and other penalties.