The University of Windsor

ELEC2250: Physical Electronics

Summer 2020

Lab Nine

Study of JFET I-V Characteristics

Friday, August 7, 2020

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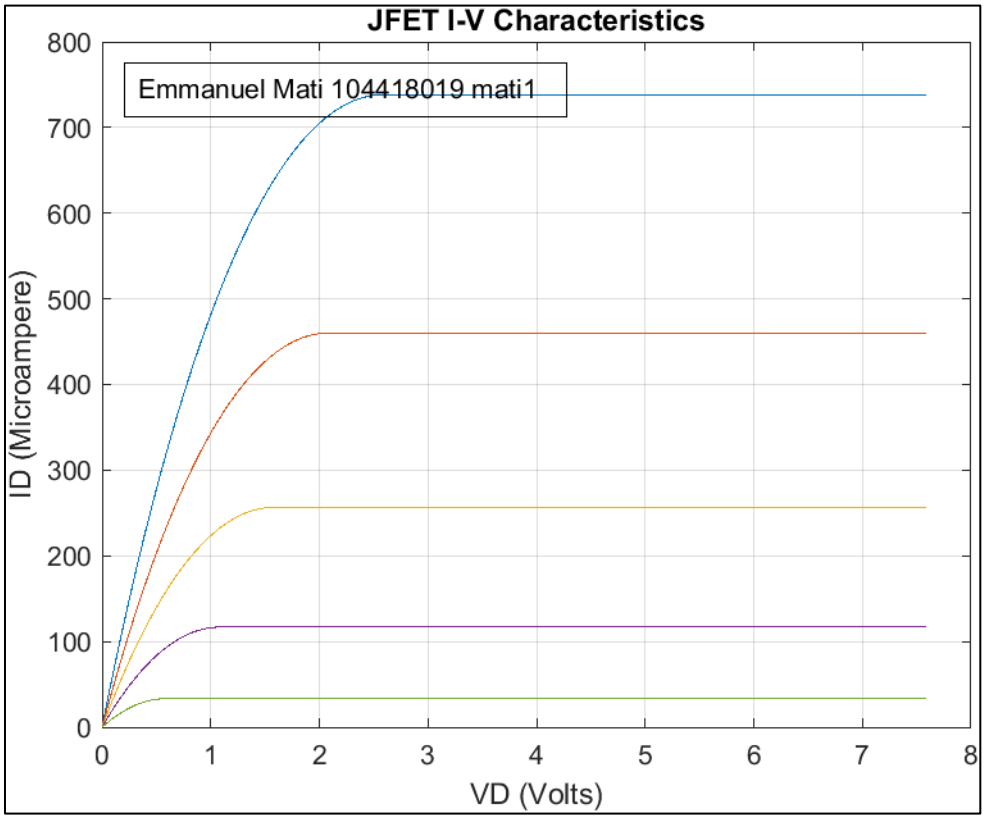
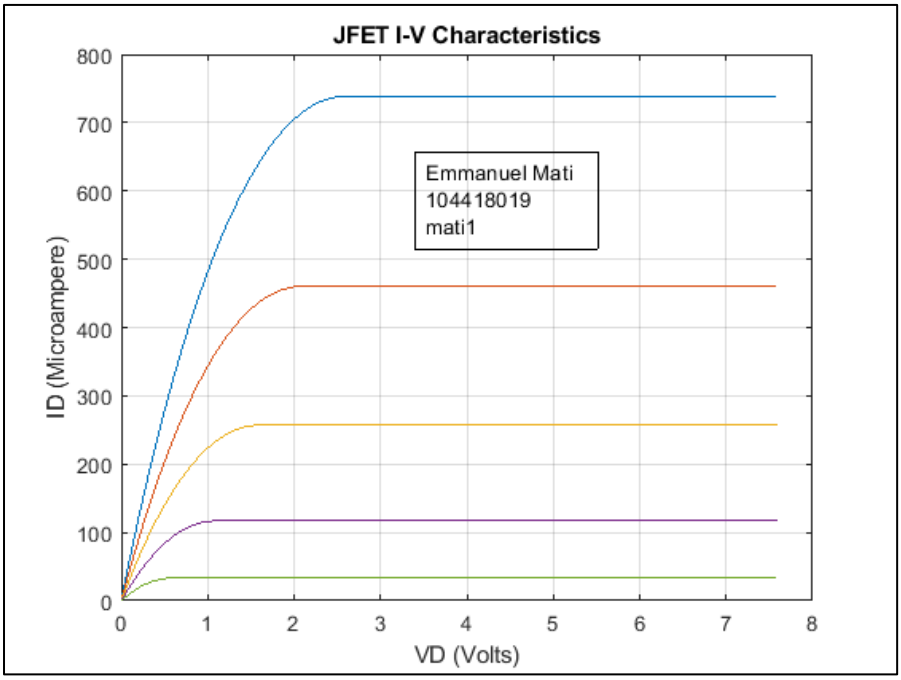
Graphs

**Refer to the MATLAB code attached to this submission*

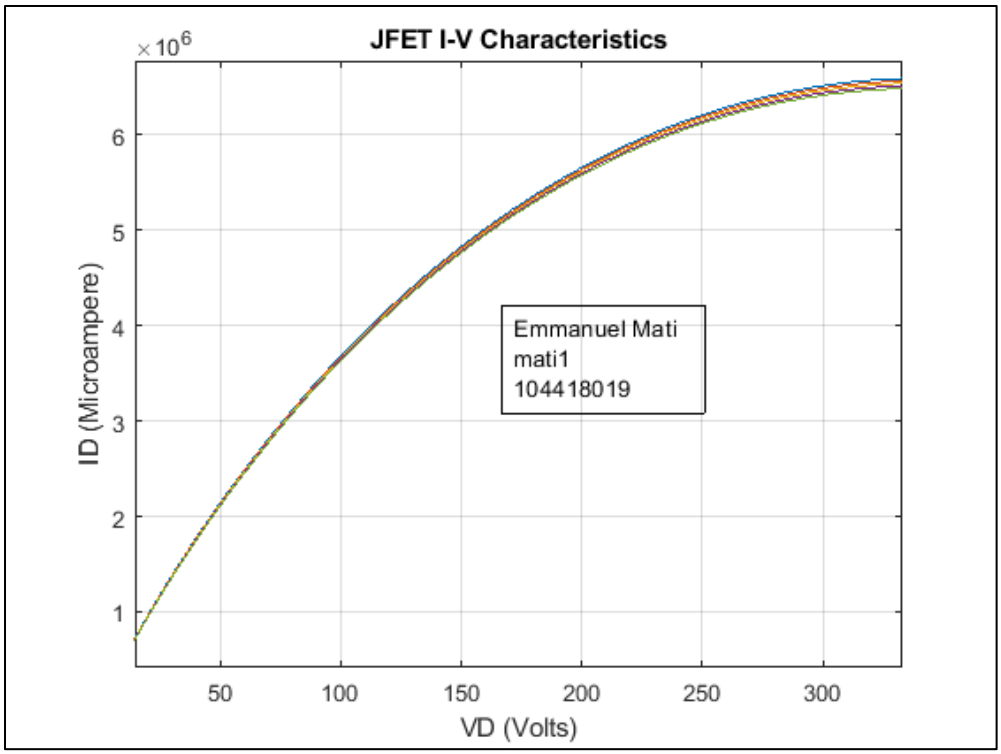
Default Output



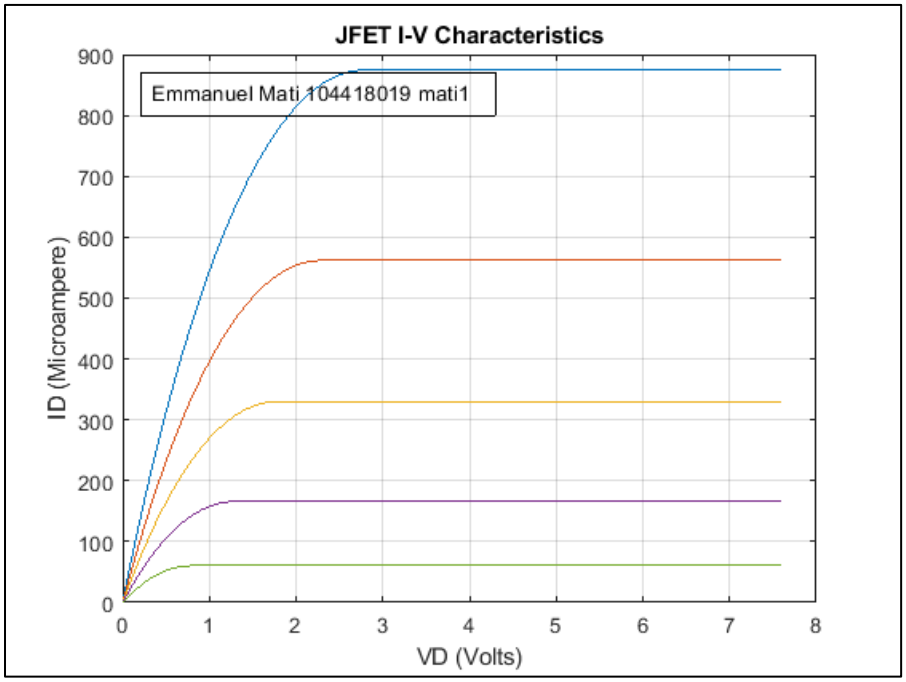
Part 1 ND = 2e15



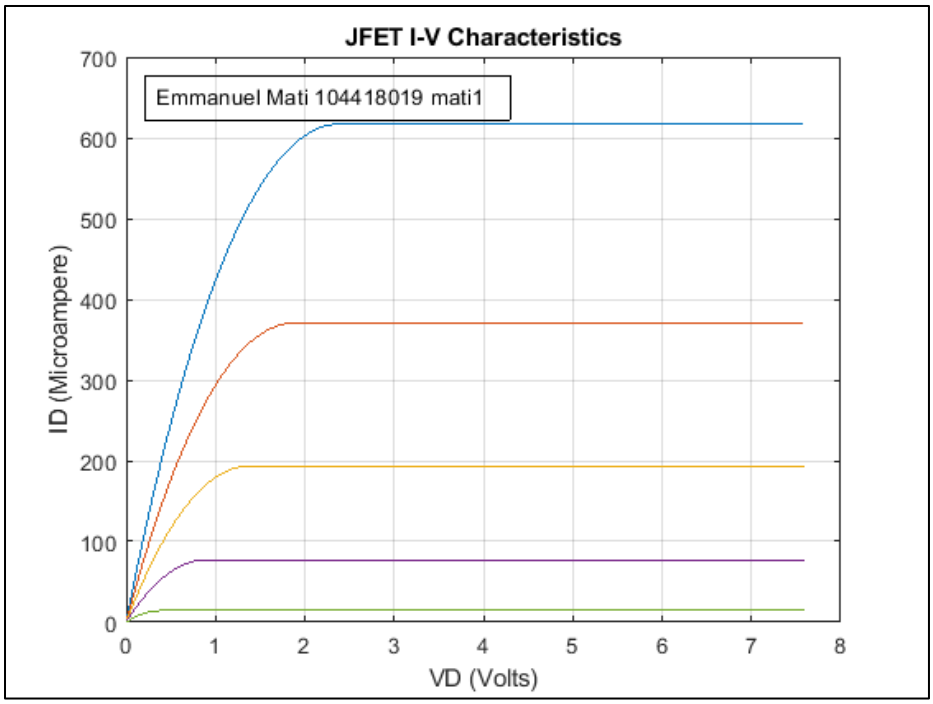
Part 1 ND = 2e17



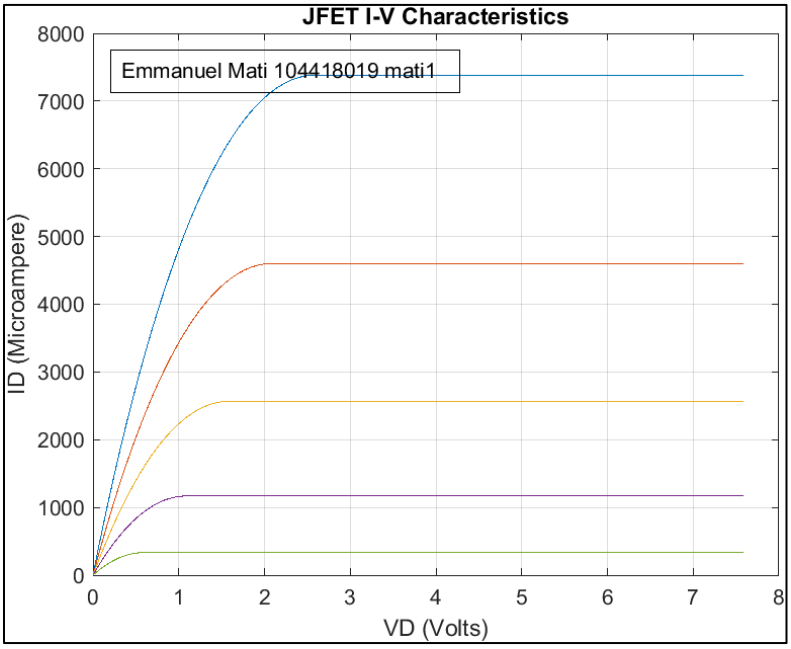
Part 2 VG= VG + 0.2



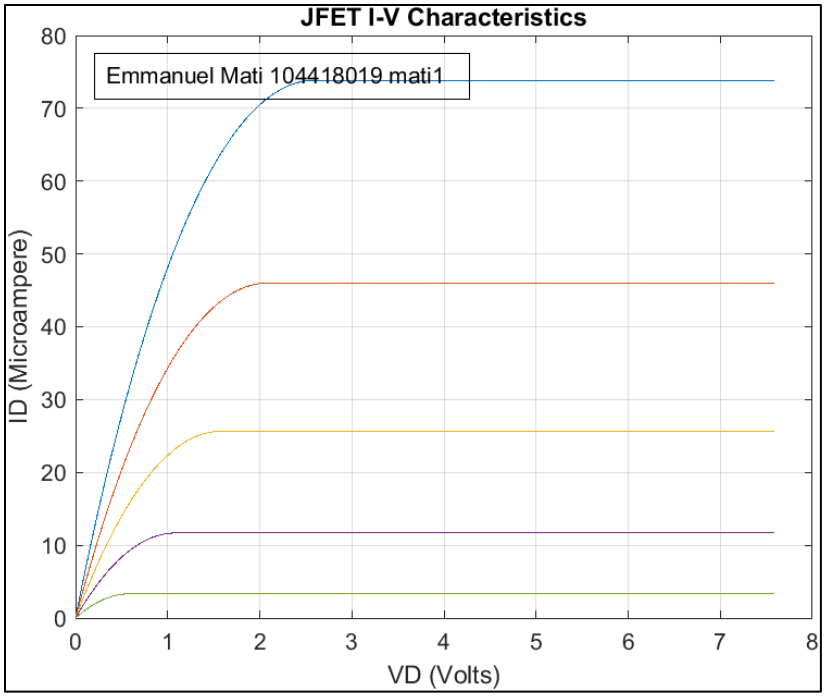
Part 2 VG= VG - 0.2



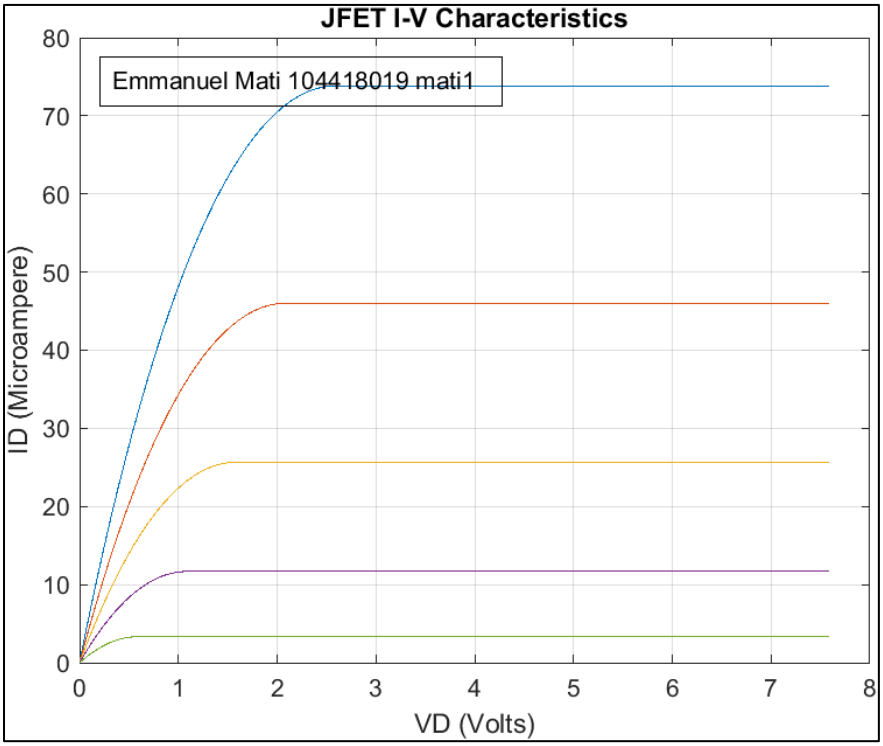
Part 3 Z= 50e-3



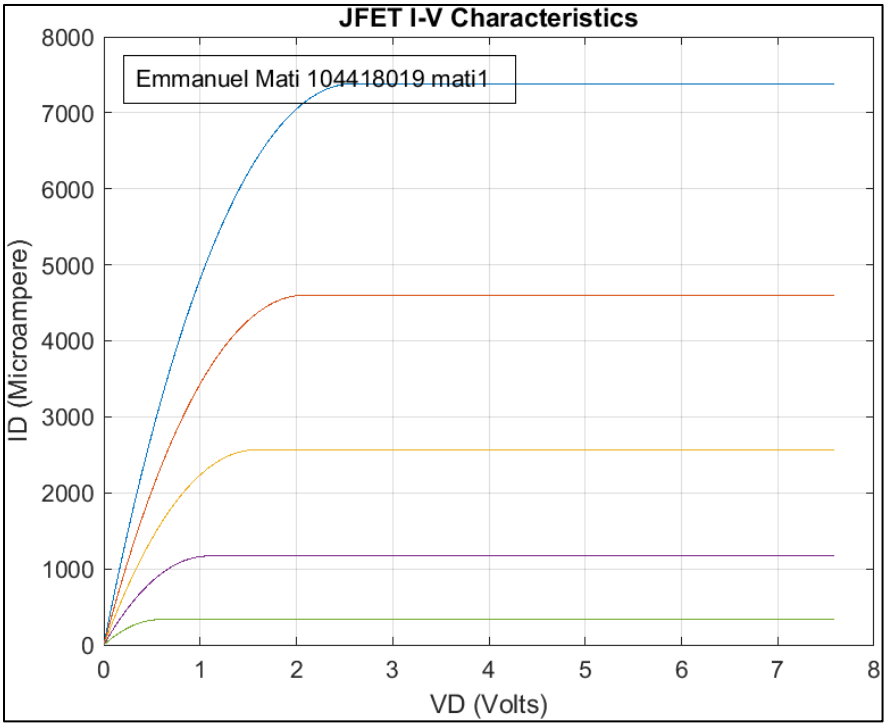
Part 3 Z= 50e-5



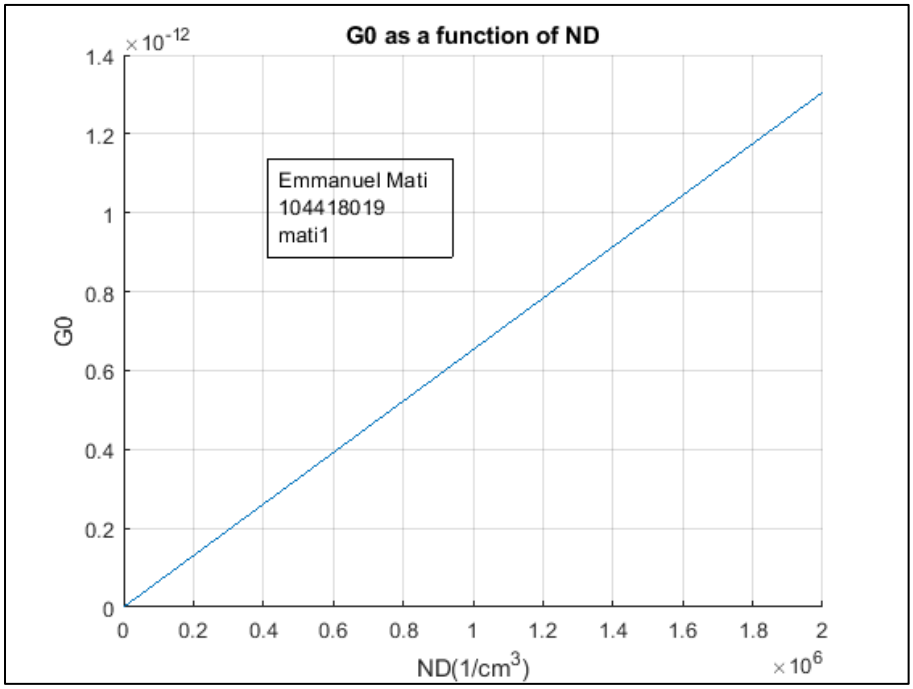
Part 4 L = 5e-3



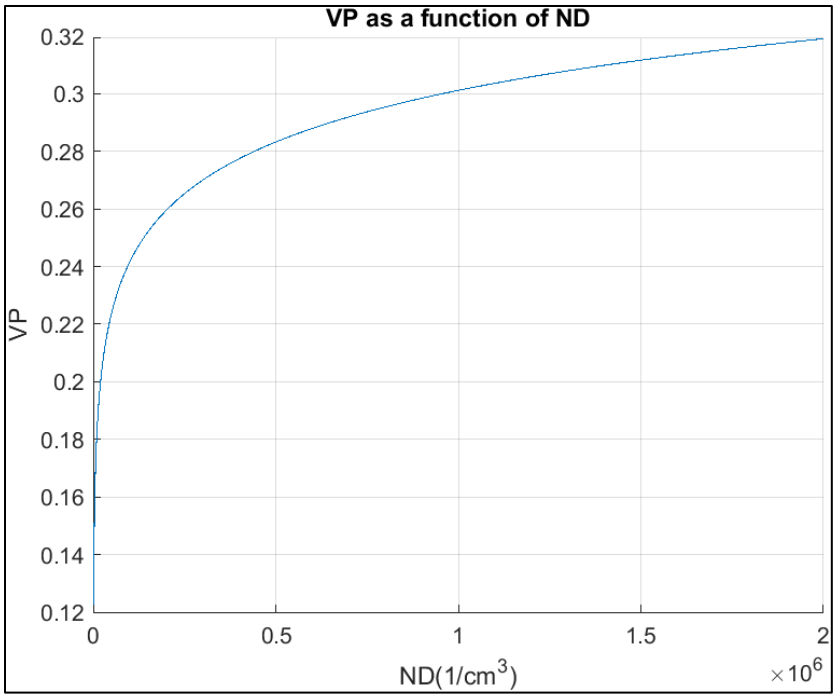
Part 4 L = 5e-5



Part 5 G0 vs Nd Varied from 0 to 2e6



Part 5 VP vs Nd Varied from 0 to 2e6



Discussion

In part one, we can see that increasing the value of ND compressed the current into almost a single line. Decreasing ND spread the values out more and required lower threshold voltage. The variation of VG showed that increasing the gate voltage ever so slightly also increased the amount of current that could pass through our JFET. Decreasing VG had the opposite effect. The variation of the width Z dramatically increased the passing current when we increased the width. This is most likely because electrons are bottle-necked through smaller widths and move slower. Increasing the length L however decreased the passing current. G0 increased linearly with ND. VP increased logarithmically with an increase in ND.