UG-2832HSWEG04

Evaluation Kit User Guide

Writer:

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Version: Preliminary

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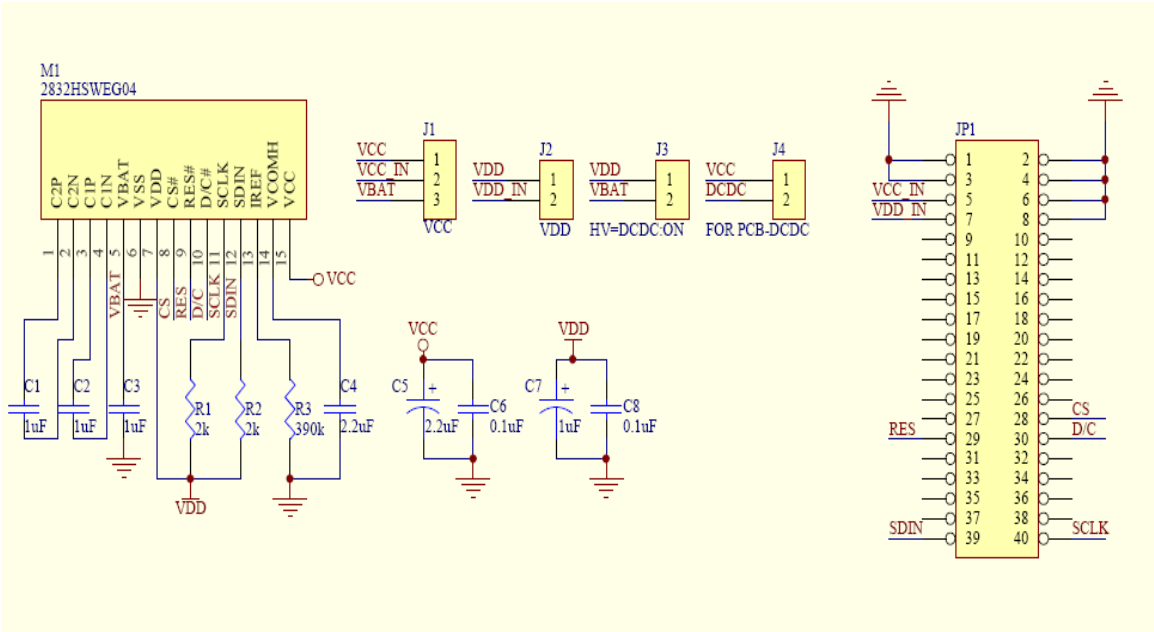
1.REVISION HISTORY

Date	Page	Contents	Version
200X/XX/XX		Preliminary	Preliminary 0.0

2.EVK Schematic



3.Symbol define

SCLK: The transmission if information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.

SDIN: This pin acts as a communication channel. The input data through SDIN are latched at the rising edge of SCLK in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock.
SDIN is identified to display data or command by D/C# bit data at the rising of first SCLK.

D/C#: This is Data/Command control pin. When it is pulled HIGH (i.e. connect to VDD), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register.

RES#: This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin HIGH (i.e. connect to VDD) during normal operation.

CS#: This pin is the chip select input. (active LOW).

VCC: Power supply for panel driving voltage. This is also the most positive power voltage supply pin.

VDD: Power supply pin for core logic operation.

VSS: This is a ground pin.

VBAT : This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.

VCOMH : The pin for COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.

C1P / C1N / C2P / C2N:
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.

4.TIMMING CHARACTERISTICS

4.1 SPI-Series MPU parallel Interface

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Table 4-1 : 4-wire Serial Interface Timing Characteristics

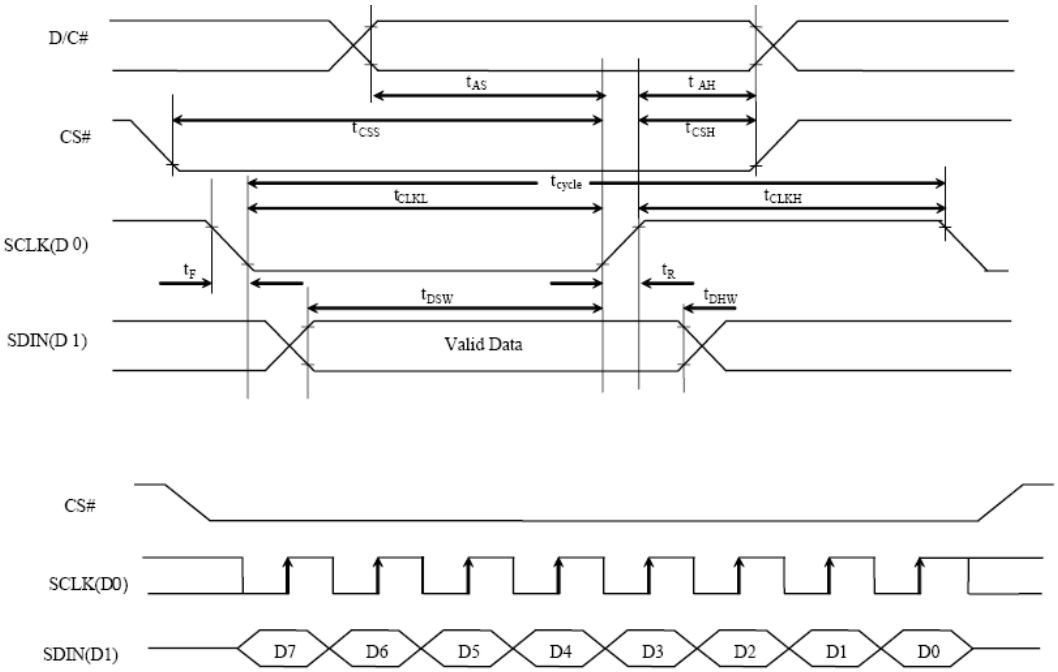


Figure 4-2 : 4-wire Serial interface characteristics

5.EVK use introduction

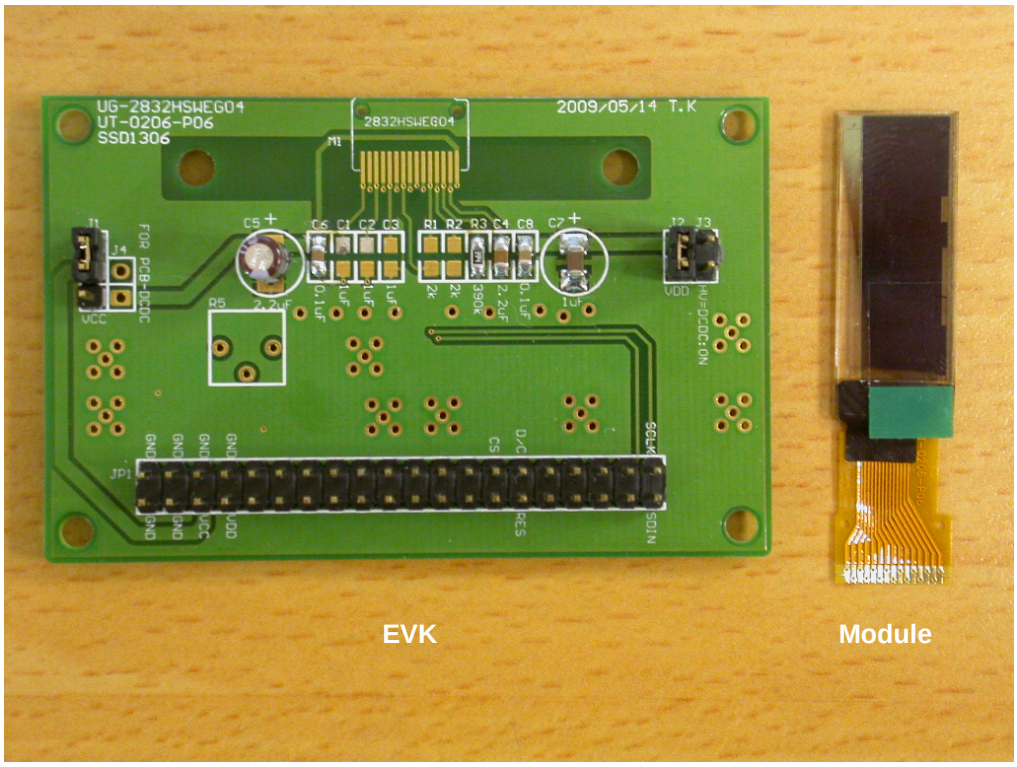


Figure 5 EVK PCB and OLED Module

UG-2832HSWEG01 is (TAB+FPC) type module, please refer to Fig5, Fig6.User can use leading wire to connect EVK with customer's system. The example shows as Fig7.

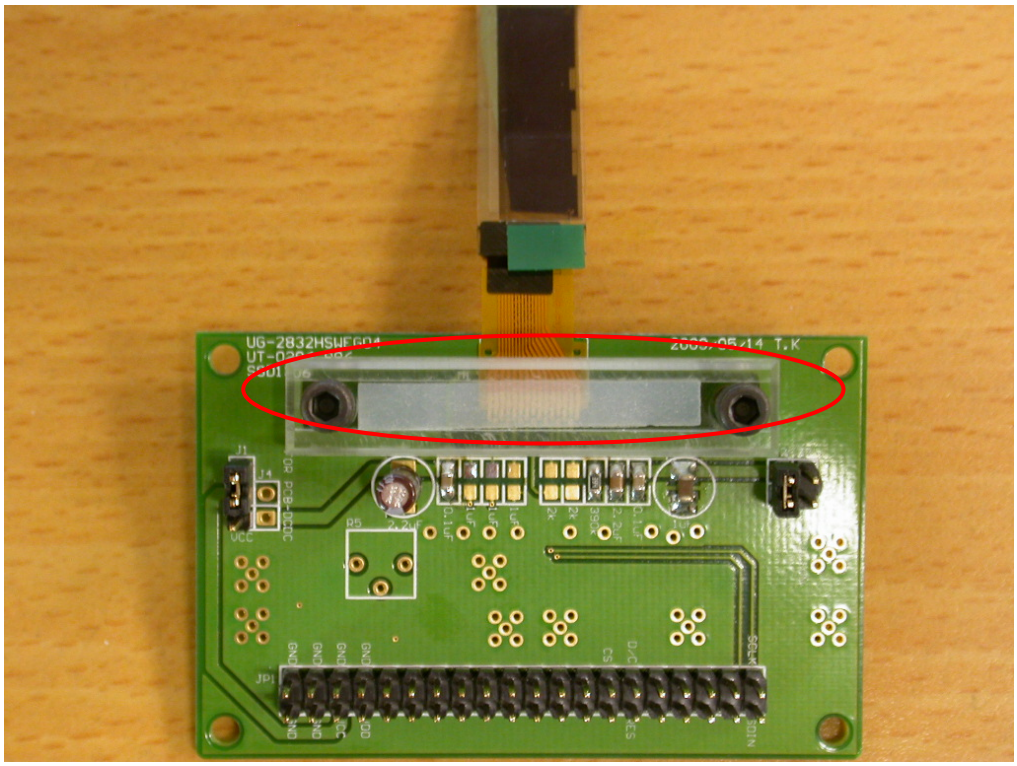


Figure 6 The combination of the module and EVK

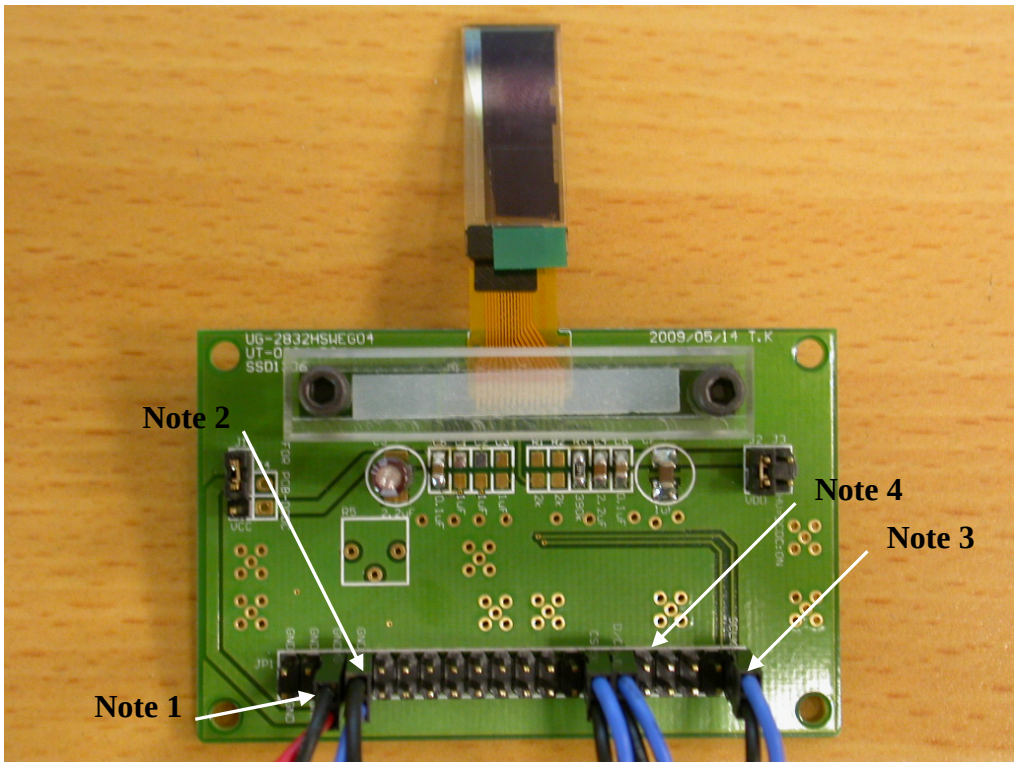


Fig 7 EVK with test platform

Note 1：It is OLED high voltage supply.

Note 2：It is logic voltage supply.

Note 3：Those are leading wire connect to control board. Those are data pin.(D0-D7)

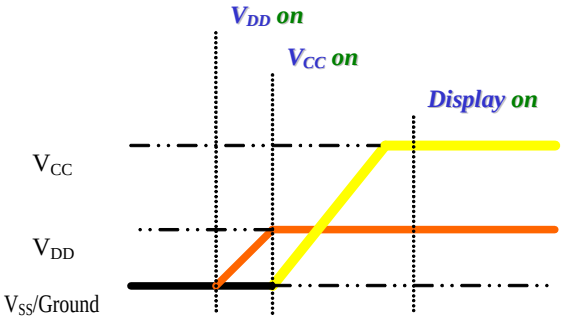
Note 4：Those are leading wire connect to control board. Those are control pin.
(A0,CSB,RDB,WRB,RSTB)

6.Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

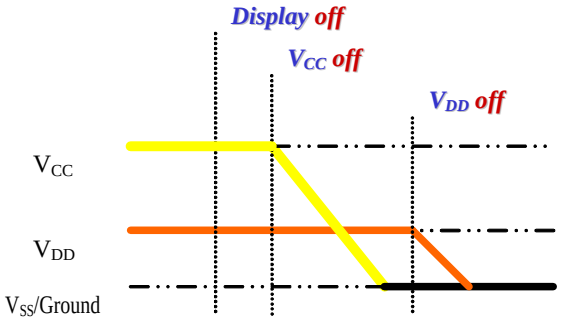
Power up Sequence:

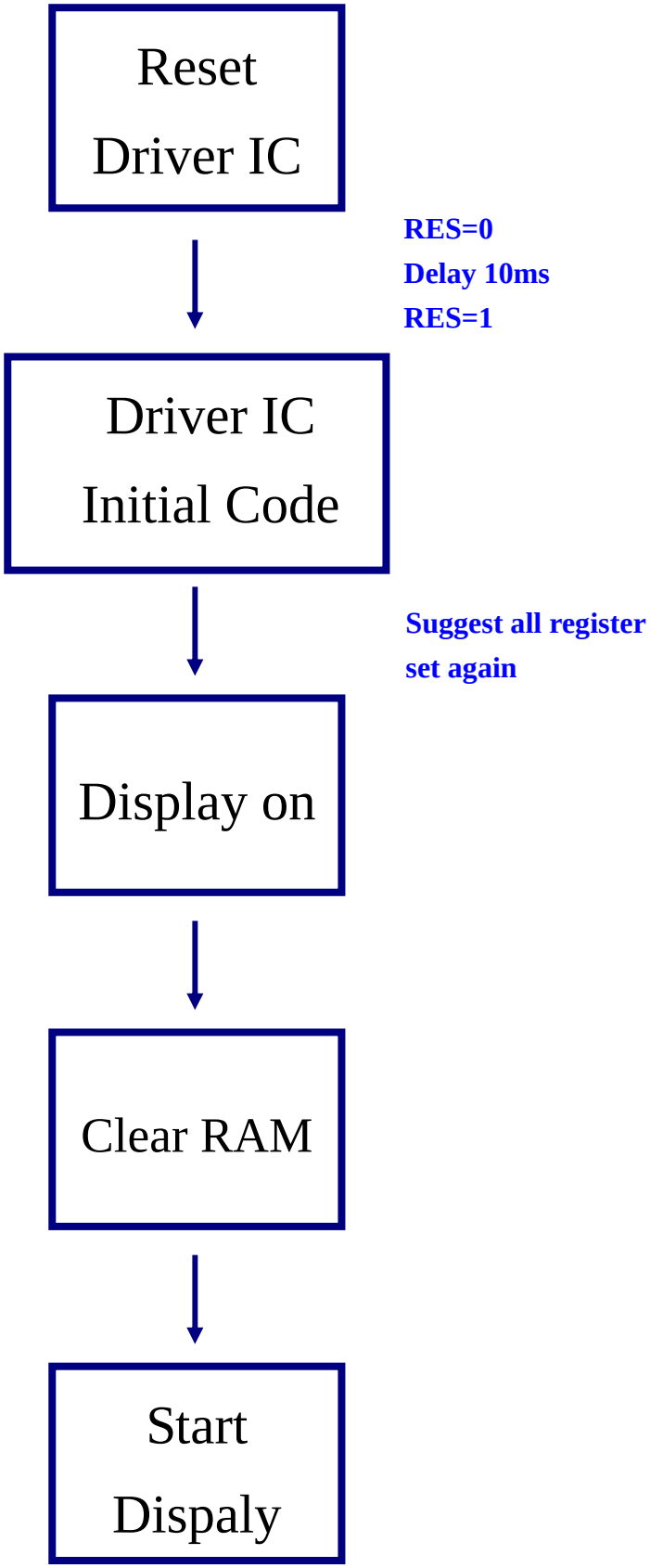
1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



7.How to use SSD1306 module

7.1 Initial Step Flow