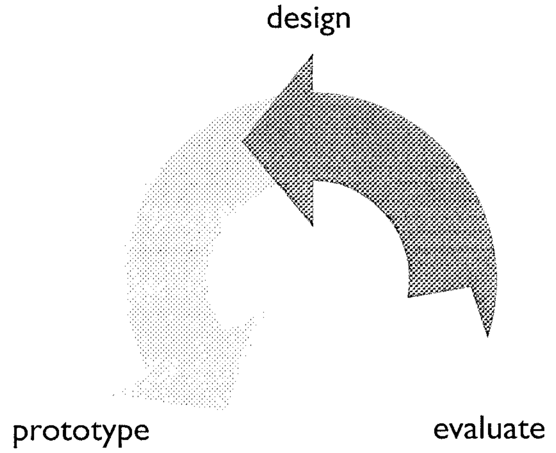
Section A. Human Computer Interaction

1 a) What is iterative design? Use a diagram in your answer.

[5]

Lecture material:

- *Iterative design is a process of system design that repeatedly moves from making designs [1], to prototyping [1] and then to evaluation [1] of the prototypes, and then back to making designs again.*



[1] for a diagram showing the three stages in the right order, in a loop

- *Users should be involved all the throughout this process, and needs and requirements for the system should be set out before it starts [1].*

b) Prototyping can be split into low fidelity and high fidelity approaches. Explain and compare these approaches. In your answer, give at least one example of each approach.

[9]

Lecture material, but involving simple analysis/comparison
Lo-fi prototypes are generally made using simple materials/techniques [1] such as sketching screen layouts on card or paper [1], hand-drawn storyboards of the stages of an interaction [1], and 'Wizard-of-Oz' simulation where an evaluator carries out the actions that an envisioned system should perform [1]. Their main advantage is that are quick to make and easily changed, and cheap to produce. [1]
Hi-fi prototypes are generally made using a programming language such as Macromind Director [1], so the appearance and behaviour of the prototype is much more realistic than in lo-fi [1]. Such a prototype generally takes longer and costs more to make than lo-fi [1]. On the other hand, users may mistakenly think that they have a final product at hand even though performance may be poor/patchy and the graphic design may be rough [1]. Extra [1] for clear explanation/comparison.

c) You have been asked to evaluate the interface to a new mobile phone application for runners and joggers, used with the phone strapped to the arm and earphones providing output. The interface will allow a user to use the phone's touch screen to enter commands in the form of gestures, and the phone will then give the required information to the runner. For example, a runner might gesture a '?' on the screen, and phone will give basic statistics such as the length of the run so far and average speed.

Choose an evaluation technique and describe how you would use it to assess the effectiveness of the application, and what potential problems or dangers you might face in running your evaluation.

[11]

Essay based on unseen design example

- *Basic issue is the difficulty of physical movement in use [1]. A controlled lab environment might be possible with a treadmill [1], but features such as accuracy of distance tracking would not be tested [1]. Such features could be tested in a real world use setting, but the evaluator will be faced with potentially keeping up with running trial subjects [1].*

- *In either case, evaluators could, ask users about the run afterwards in an interview [1]*

- *Example approach: system logging to generate raw quantitative data on runner's motion and use of gestural comments. (Other approaches would be fine too, if also explained well.) [1]*

- *Should test with the particular group of users the product is aimed at: runners. Shouldn't just be tested on you and the design team, or random members of population [1]*

- *Should do this in a relevant environment of use, i.e. people's normal running routes [1].*

- *A post-run interview could be based on jointly looking at the data to guide questions [1]. You would then video or audio tape the subjects so that later on you can hear what they are saying and doing [1]*

- *You should test the users doing an appropriate set of tasks that covers the basic interface features. [1]*

- *Need to check if the is too big or bulky to be comfortable on the arm [1]*

CS1Q June 2011

Section B: Information Management.

1.

a) Draw an Entity-Relationship diagram for the following scenario, indicate clearly all primary keys and the cardinality and totality of all relationships.

Academic staff have unique identification numbers, a surname and title. Students have a unique matric number, a surname and firstname. All students have an academic staff member as their advisor. Some academic staff advise several students and some academic staff advise no students. Some students work in a shop and some work in a pub. Several students may work in the same shop, but not in the same pub. Pubs and shops may be close to each other, in which case the distance between them is recorded. Each member of academic staff buys food from a single shop, but they don't necessarily all shop at the same venue.

[11]

b) Assume there is a relational database that implements part of the scenario above, with three tables as follows:

Student = (Surname:Text, Firstname:Text, <u>Matricno</u>:Text, Worksh:Text)
Staff =(Surname:Text, Fname:Text, <u>Staff-id</u>:Text, Title:Text, Shopping: Text)
Shop = (<u>Name</u>:Text)

Assume that underlined attributes are primary keys and Worksh and Shopping are foreign keys referring to the Name attribute of Shop.

i) Write an SQL query that returns the surnames of academic staff who buy their food at "Tesco".

[2]

ii) Write an SQL query that returns the firstnames and surnames of students who work in a shop where Dr Gay buys his food.

[4]

c) Given the following sets: A={1,3,7,9}, B = {1,4,6}, C={7,9}

give the following. Assume that $\wp$ is the powerset operator.

i) $|B|$
ii) $\wp(B)$
iii) $|\wp(C)|$
iv) B X C
v) $A \cup B$
vi) $A \cap C$
vii) A - C
viii) Which of the following are true
   a. $C \subseteq A$
   b. $C \subseteq B$
   c. $\langle 1,6 \rangle \in A \times B$

[8]

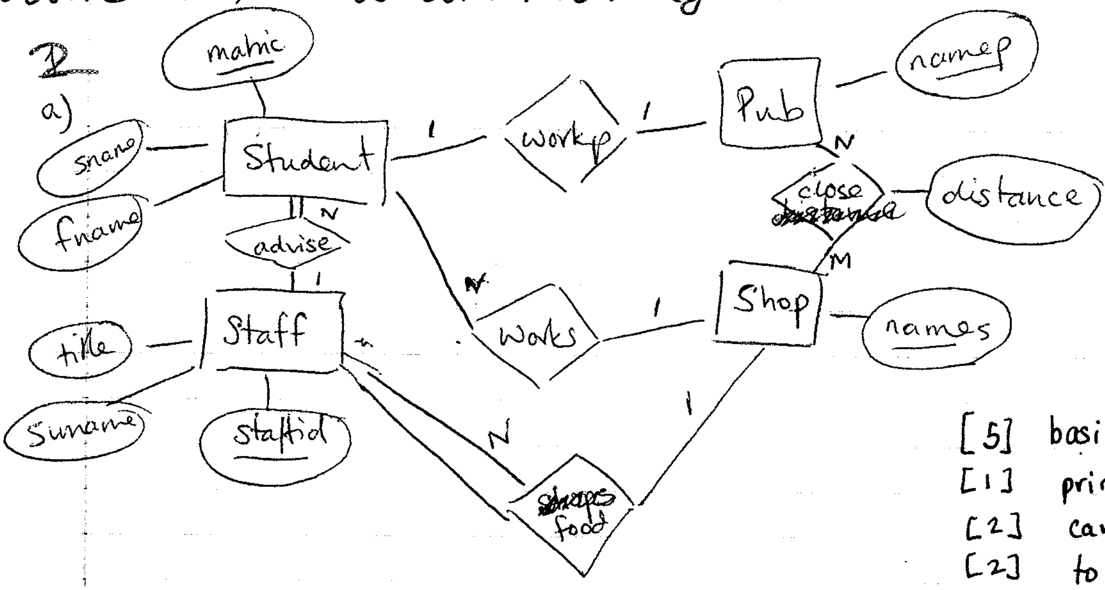
Section B - Information Management.

JUNE

ANSWERS

2

a)



[5] basic entities + relns
[1] primary keys
[2] cardinalities
[2] totalities
[1] distance

b) i)

```
Select Surname
  from Staff
  where Shopping = "Tesco"
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[2]

ii)

```
Select Firstname, Surname
  from Student, Shop
  where Student.Worksh = Staff.Shopping
    and Staff.Surname = "Gay"
    and Staff.Title = "Dr"
```

[4]

c). $A = \{1,3,7,9\}$ $B = \{1,4,6\}$ $C = \{7,9\}$

i $|B| = 3$

ii $\mathcal{P}(B) = \{\{\}, \{1\}, \{4\}, \{6\}, \{1,4\}, \{1,6\}, \{4,6\}, \{1,4,6\}\}$

iii $|\mathcal{P}(C)| = 4$

iv $B \times C = \{\langle 1,7\rangle, \langle 1,9\rangle, \langle 4,7\rangle, \langle 4,9\rangle, \langle 6,7\rangle, \langle 6,9\rangle\}$

v $A \cup C = \{1,3,7,9\}$

vi $A \wedge C = \{7,9\}$

vii $A - C = \{1,3\}$

viii $C \subseteq A$ ✓

$C \subseteq B$ ✗

$\langle 1,6\rangle \in A \times B$ ✓

[8]

Section C - Systems (Q3 & 4)

3. (a) Modern digital computers are based on the use of binary arithmetic. Give two reasons why the binary system of representing numbers is used.

[2]

Binary requires only two states to be represented per digit: on and off, 1 and 0 etc., potentially simplifying logic gate implementations, and these states can be represented unambiguously using physical quantities such as the presence or absence of electric charge or magnetic field direction etc. (will accept variation on this answer)

[2]

(b) Given a decimal number D explain how to determine how many binary digits N are required to represent D. Illustrate your answer by explaining how many bits are needed to represent 257

[2]

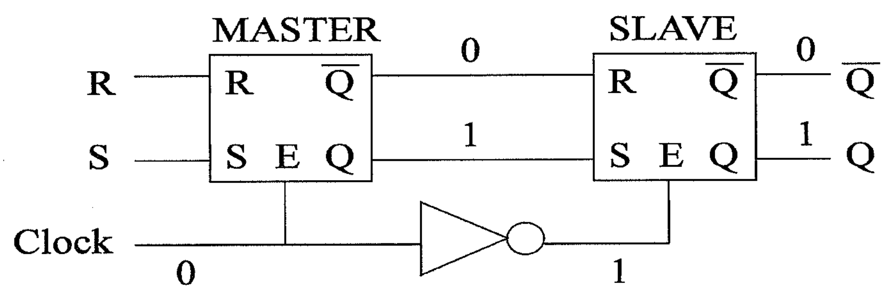
If the number is at least 2^N but less than 2^{N+1} then $N+1$ bits are needed.

[1]

257 is at least $2^8 = 256$ but less than $2^9 = 512$ therefore $N = 9$ bits are needed to represent 257.

[1]

(c) The following circuit schematic implements a Set-Reset flop, explain the operation of this circuit.



[4]

When the clock is 1, the master flipflop is enabled and responds to its inputs. It can therefore be set or reset by the S and R inputs. [1]

The slave flipflop is not enabled, because it receives the inverted clock, which is 0. Therefore the outputs of the circuit, corresponding to the value stored in the slave flipflop and are not affected by the S and R inputs. [1]

When the clock changes to 0, the master flipflop is no longer enabled, so its stored value is fixed according to whether the S or R input was the last one to have value 1. The slave flipflop is now enabled, so the outputs of the master flipflop set or reset the value stored in the slave. [1]

Therefore as the clock changes from 1 to 0, the value represented by the inputs to the master flipflop is transferred to the slave flipflop. Once the slave has received this value, its outputs are fixed until the next time the clock changes from 1 to 0. This circuit is a negative edge-triggered RS flipflop. [1]

(I will accept variations on the above)

(d) The two's complement representation for negative binary numbers was devised to allow ordinary binary arithmetic operations to work correctly when performing calculations involving both positive and negative binary numbers.

Explain how to compute the two's complement of a 3 bit binary word, stating the range of positive and negative values that can be represented using only a 3 bit word.

[2]

The twos' complement representation of a binary number is computed by inverting the bits of the input number and then adding 1, ignoring overflows. [1]

The range of values that can be expressed in a two's complement 3 bit number is from -4 to +3. [1]

(e) You are required to design a circuit which will perform the two's complement operation you defined in question (d).(i) on an input 3 bit word *xyz*, and output a 3 bit word *abc* containing the results of this operation.

(i) Draw a truth table which shows *a*, *b*, *c* as functions of *x*, *y*, *z*.

[4]

x	y	z	a	b	c
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

(0.5 marks for each correct row.)

(ii) Draw a Karnaugh map for each of *a*, *b*, *c*.

[3]

Karnaugh map for a: (1 mark)

	not(y)	y	y	not(y)
not(x)	0	1	1	1
x	1	0	0	0
	not(z)	not(z)	z	z

Karnaugh map for b: (1 mark)

	not(y)	y	y	not(y)
not(x)	0	1	0	1
x	0	1	0	1
	not(z)	not(z)	z	z

Karnaugh map for c: (1 mark)

	not(y)	y	y	not(y)
not(x)	0	0	1	1
x	0	0	1	1
	not(z)	not(z)	z	z

1 mark for each correct table

(iii) Use the Karnaugh maps to work out formulae for *a*, *b* and *c* in terms of *x*, *y* and *z*, and simplify these as far as you can.

[3]

$$a = \overline{x}y + \overline{x}z + x\overline{y}\,\overline{z} = \overline{x}(y+z) + x\overline{y}\,\overline{z}$$

$$b = \overline{z}y + z\overline{y} = z \oplus y$$

$$c = z$$

(1 mark each for *a*, *b*, and *c*.)

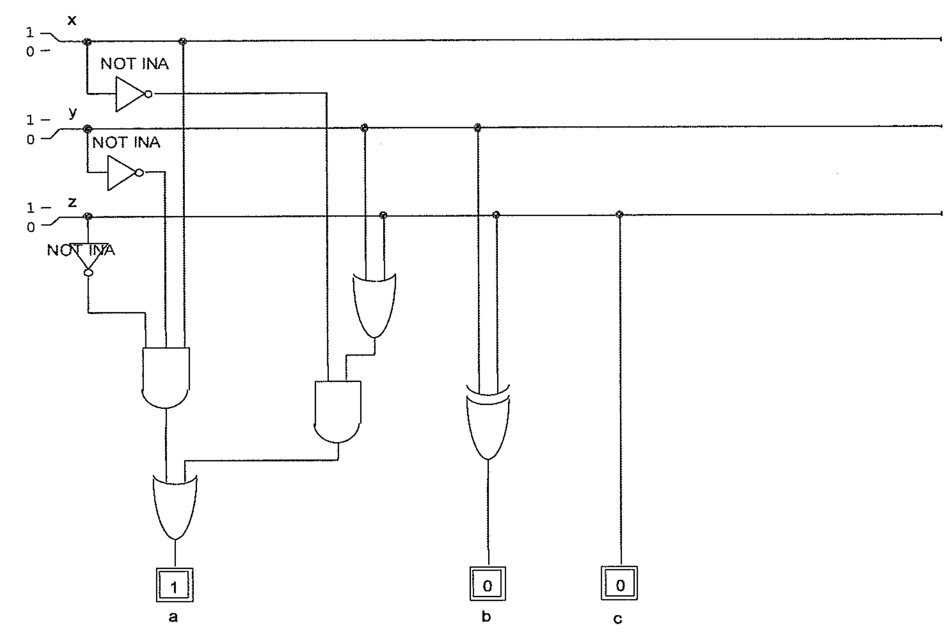
(iv) Consider the truth table you constructed for the two's complement operation you defined in (d).(i) applied to a 3 bit word. What anomaly do you notice and why is this so?

[2]

The two's complement for -4 becomes 100 in binary, since +4 cannot be expressed within a 3 bit two's complement representation [1]. This leads to the negation of -4 remaining equal to -4, while all other inputs that can be represented invert correctly. [1]

(v) Draw a circuit schematic that given an input *xyz* representing a 3 bit word, implements the equations you derived in section (iv) above to produce a 3bit output word *abc*.

[3]



[3]

4. **(a)** **(i)** Explain what is a compiler, what it does and suggest two circumstances that would instead require a cross-compiler to be used. [4]

A compiler is a program that converts high-level source language statements into low-level machine codes that can execute directly on the same machine architecture executing the compiler. [2]

A cross-compiler is used when a compiler executing on the target machine architecture is not available (because it has not yet been developed), or the target architecture is not suitable for hosting a compiler. [2]

(ii) A C compiler is available, running on an X86 computer, that translates C source statements into machine codes that can execute on an ARM architecture machine and this compiler has also been coded in C. Explain how to migrate this C compiler to execute on an ARM architecture machine. [2]

(i) Compile the C compiler source statements by the C compiler itself [1] and copy this compiler executable code to the ARM machine. This C compiler will now run directly on the ARM and will translate source C statements into ARM machine codes. [1]

(iii) Considering your answers to questions (i) & (ii) above, explain why it is a good idea to implement a compiler in the same language that it is intended to compile.

[4]

I will accept variations such as the following, up to a maximum up to 4 marks:

(ii) Since it is possible to compile the compiler by itself, once a basic compiler has been implemented this can be expanded incrementally [1] or improved incrementally in terms of its code optimization performance [1] and compiled by itself to generate a new compiler implemented using the previous version's machine codes [1]. If the new compiler is then used to compile itself, then this new compiler will also benefit at run-time from any improvements made by optimizing the current machine codes implemented by its source [1]. Compiler portability is improved, since the C source statements can be compiled by any C compiler regardless of it's underlying architecture to produce a cross compiler [1]. Only the code generator section of the C compiler needs to be updated to produce a cross-complier that can migrate to a new machine architecture, as described in (ii) [1]

(b) Currently many Internet Service Providers are offering increasingly higher bandwidth products. Write a brief report explaining why such claimed raw bandwidth does not always translate into proportionally increased network access speeds for the home computer user.

[15]

The speed advertised by many ISPs is not always available to end users. Typically, by subscribing to premium services, for instance up to 40Mbps in 2011, a customer will reduce the level of contention that they face when sharing the ISPs resources because the ISP will provide a preferential share of their bandwidth [1] than is allocated to other customers at a lower tariff [2].

Further problems can affect the throughput – ranging from the distance between the consumer and the local exchange [1] through to the nature of the cabling used [1] – for example optic fiber may be more resilient to the interference that would otherwise create delays for error correction [1]. Many of these issues are outside the immediate control of the ISP [1]. For example, delays may commonly be experienced in accessing external resources because of the limited capacity of routers given relatively high demand on key connections [2].

There may be other reasons for the delays that end users often diagnose as the result of inadequate bandwidth – for example, better response on secondary tasks may be achieved from dual and quad core architectures [1]. Performance should be profiled to consider the other bottlenecks that may arise – for example through insufficient RAM [1].

Other delays stem from limited ability of remote servers to process requests from client machines [2]. Increasing the capacity of servers may only provide a short term solution – as more users may be drawn to a resource by performance improvements [1]. Mirror sites [1] and more effective use of end-user caching [1] can also be used to mitigate these problems.

Many other solutions are possible – the key aim is for answers to connect different aspects of the systems and architecture material with aspects of the HCI course. Up to a total of 15 marks.