Proiect SCIA

Supervisor:

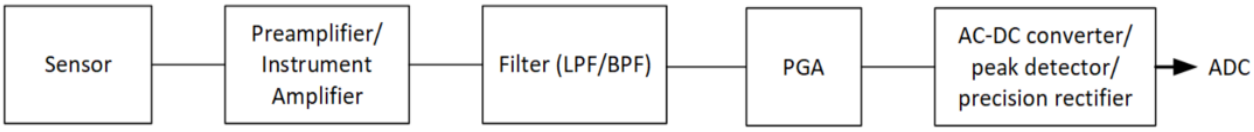
Dr.Ing.Prof.Marius Neag
Dr.Ing.Prof Onet Raul Ciprian

Student:

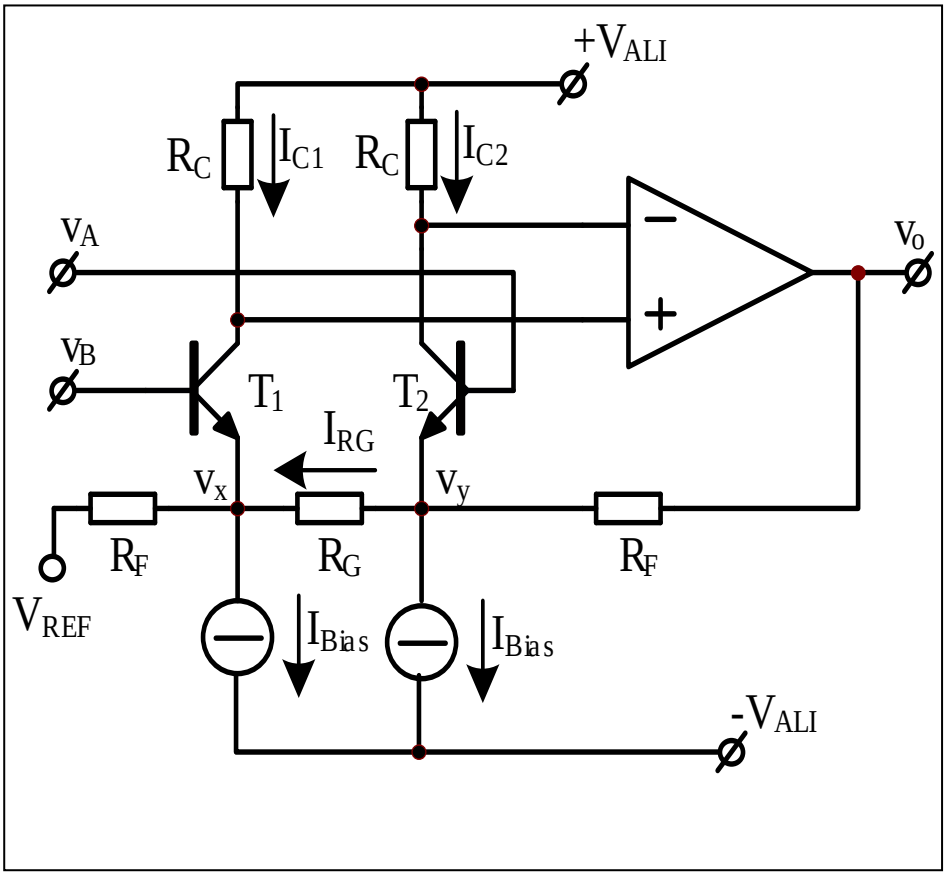
Morar Horea-Razvan
Gr 2331

1.Project Thematic

The project aims to design and implement an analog interface that meets the specific requirements for use in analog signal processing applications. The interface consists of 4 blocks, connected in cascade, each with a specific role:



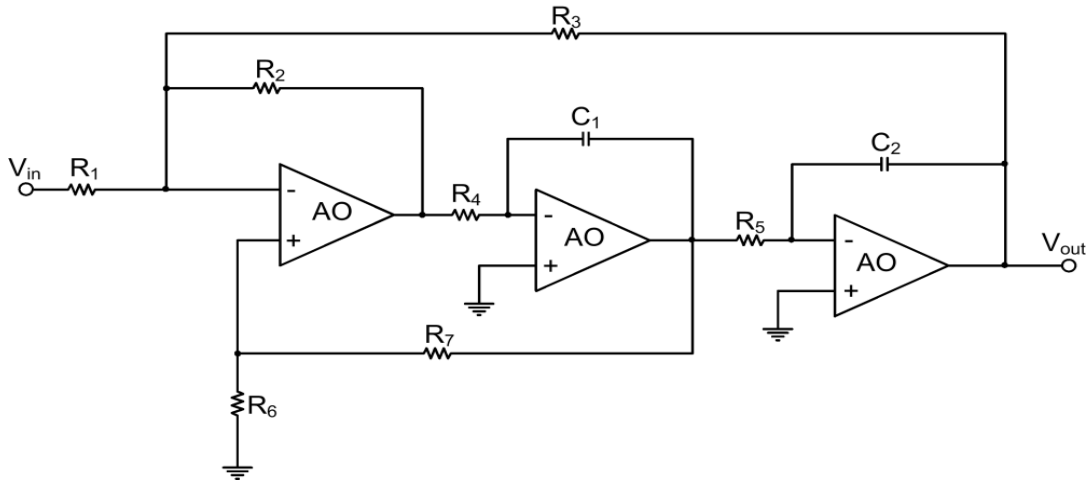
Given specifications: The first stage was configured as a passive current feedback instrumentation amplifier, with the following circuit:



And it has the following specifications:

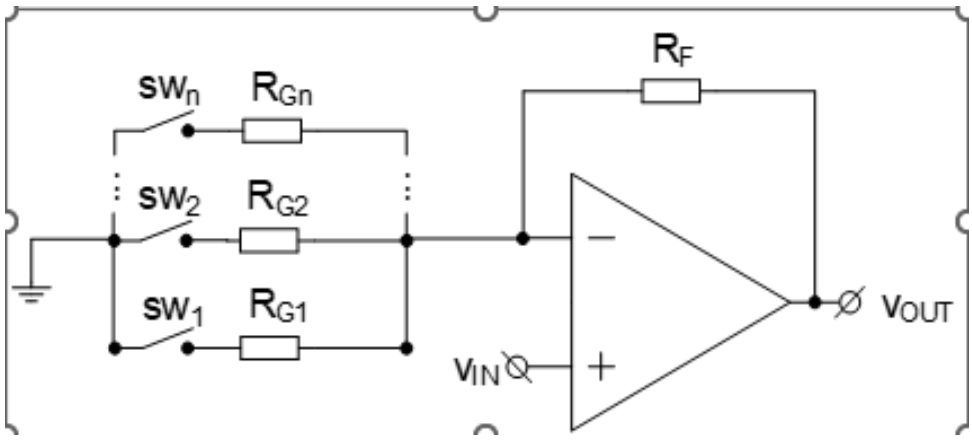
1.Maximum amplitude (for minimum PGA gain): 1.06E-01
2. Minimum amplitude(for maximum PGA gain) : 5.33E-02
3.Unit of measurement : Voltage(differential)
4.Linear and modulus gain : 10

The second stage is a Analog Low-Pass Filter (KHN) with the following circuit:



And it had the given specifications:
1.|H0| , linear gain in pass band : 1.00E+00
2.Minimum input resistance: 1.00E+03
3.Band : 6000 Hz
4.Quality factor, Q : 0.707

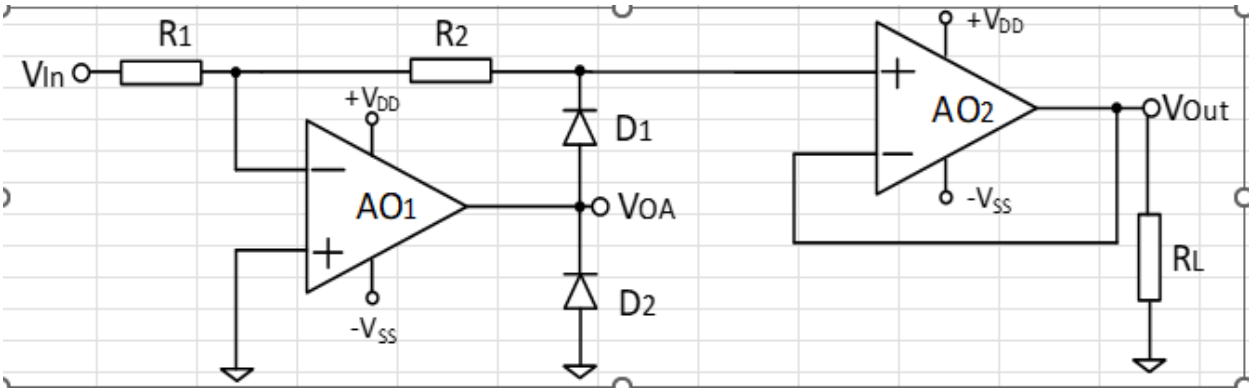
The third stage is a programmable gain amplifier with RG Parallel with the following circuit:



And it has the given specifications:

1.Minimum gain in dBs : 9 dB
2.Resolution(minimum step) : 2 dB
3.Total number of steps : 4
4.Maximum gain in dBs : 1.50E+01

The fourth stage is a precision full-wave rectifier with the following circuit:



And it has the given specifications:

1. Gain (modulus and linear) : 1

2.Sizing of Stages 1 / 2 / 3 / 4

2.1.Sizing of the first stage:

Based on the following formula:

$$Av = \frac{Vo}{Vid} = \frac{Vo}{Va-Vb} = 1 + 2 * \frac{Rf}{Rg} \quad (1)$$

And the already known gain Av = 10 results the following:

$$10 = 1 + 2 * \frac{Rf}{Rg} \quad (2)$$

$$9=2*\frac{Rf}{Rg} \quad (3)$$

From which we get the following ratios of $\frac{Rf}{Rg} = \frac{9k\Omega}{2k\Omega}$

And knowing this we could just select a value for the Rc resistances from the above circuit , which was 5k. This ensured us the necessary gain of 10.

2.2.Sizing of the second stage:

Dimensional parameters:

1. Resistors:

$$R1 = R2 = R3 = \ldots = R7 = R => Ho = 1; \omega_0 = \frac{1}{R\sqrt{C1C2}}; Q = \frac{2}{3}\sqrt{\frac{C1}{C2}}$$

I chose R=15.9k **Ω**

2. Capacitors:

$$\omega_0 = 2\pi f_c = 2\pi 6000 = 37.680 \quad (1)$$

$$C_1 = \frac{3Q}{2\omega_0 R} = \frac{3*0.707}{2*37.680*15.9k} = 1.77nF \quad (2)$$

$$C_2 = \frac{4C_1}{9Q^2} = \frac{2}{3Q\omega_0 R} = \frac{2}{3*0.707*37.680*15.9k} = 1.57nF \quad (3)$$

2.3.Sizing of the third stage:

Resistors:

We choose Rf=10k

$$|A_v| = \{9dB, 11dB, 13dB, 15dB\} = \{2.82V, 3.55V, 4.47V, 5.62V\} \quad (1)$$

$$A_v = \frac{R_f}{R_g} => R_g = \frac{R_f}{A_v} => \quad (2)$$

$$\begin{cases} R_1 = 3.6k\Omega \\ R_2 = 2.82k\Omega \\ R_3 = 2.23k\Omega \\ R_4 = 1.8k\Omega \end{cases} \quad (4)$$

SW1	SW2	SW3	SW4	$R_f[\Omega]$	R[Ω]	$A_v[dB]$	$A_v[\frac{V}{V}]$
VDD	0	0	0	10k	3.6k	9	2.82
0	VDD	0	0	10k	2.82k	11	3.55
0	0	VDD	0	10k	2.23k	13	4.47
0	0	0	VDD	10k	1.8k	15	5.62

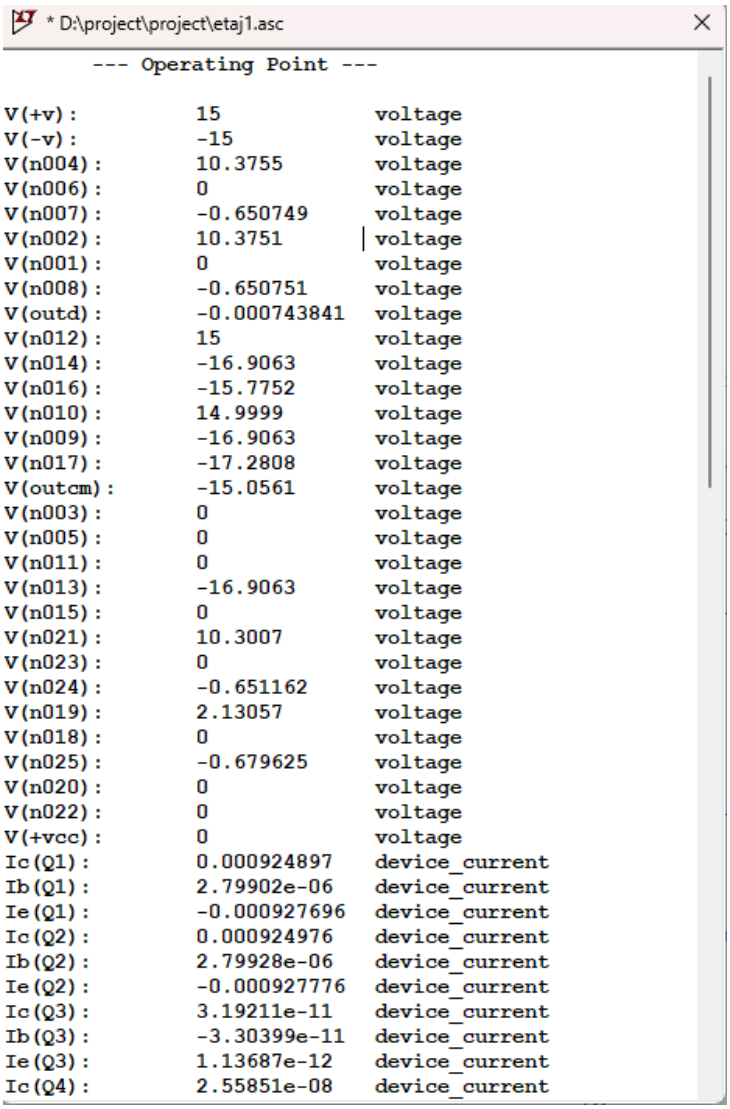
2.4.Sizing of the fourth stage:

For the fourth stage we choose R=10kΩ and we keep in mind the fact that the resistors need to be equal in order to get the gain 1.

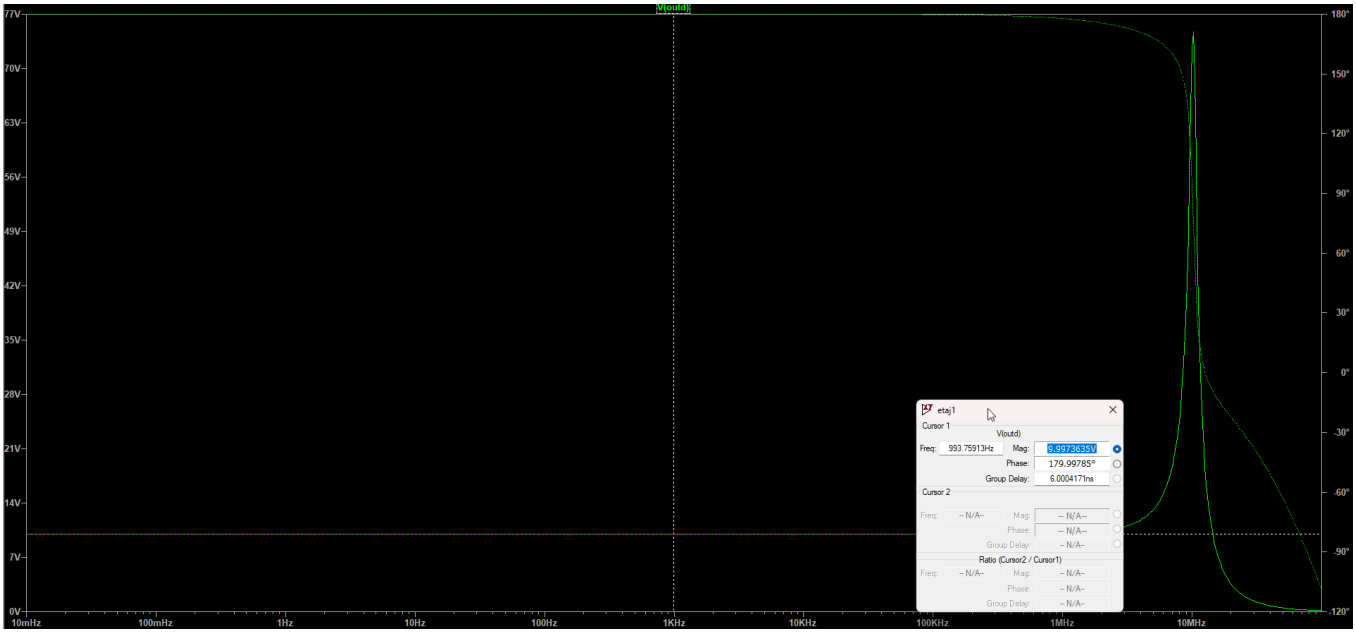
3.Characterization of Stages 1 / 2 / 3 / 4

3.1.Characterization of Stage 1

DCOP Parameters:

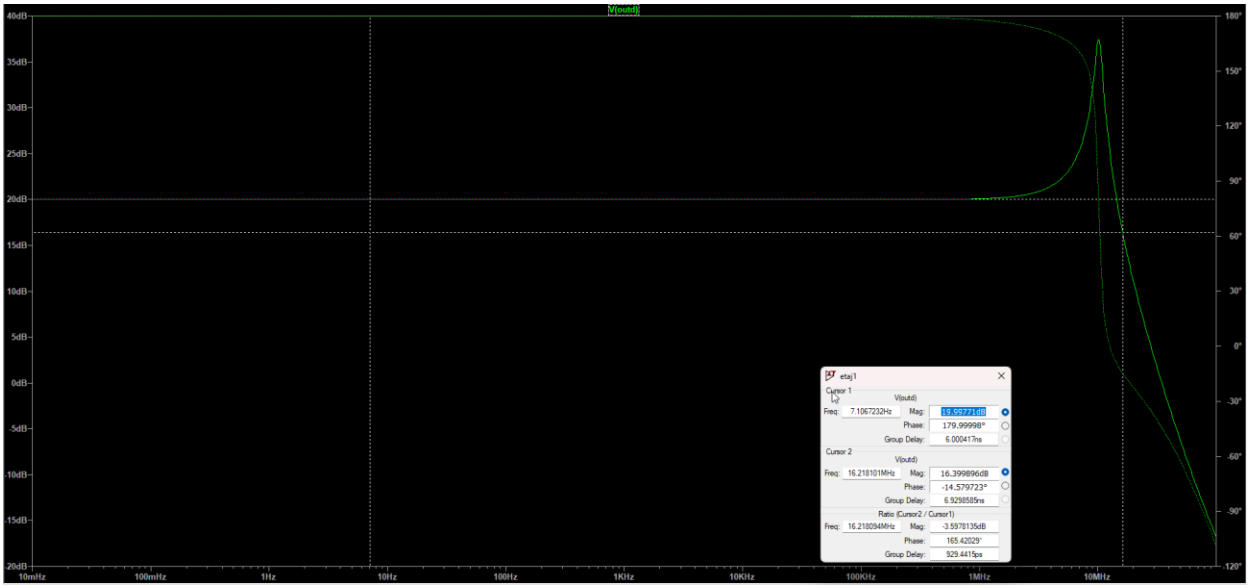


Demonstration of low frequency gain:
Simulation used: .ac dec 100 .01 100Meg



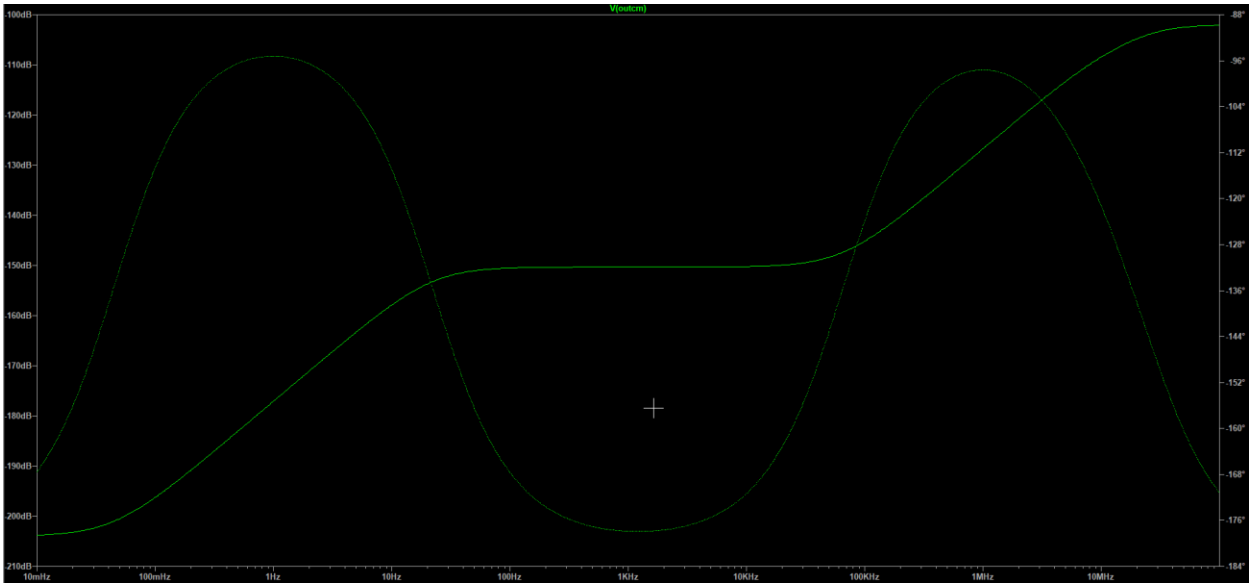
Value obtained is 9.997 which approximately is 10 , which was the given spec.
The spike is a overshoot because of the Opamp AD8065

Demonstration of band higher than that of filter
Simulation used: .ac dec 100 .01 100Meg

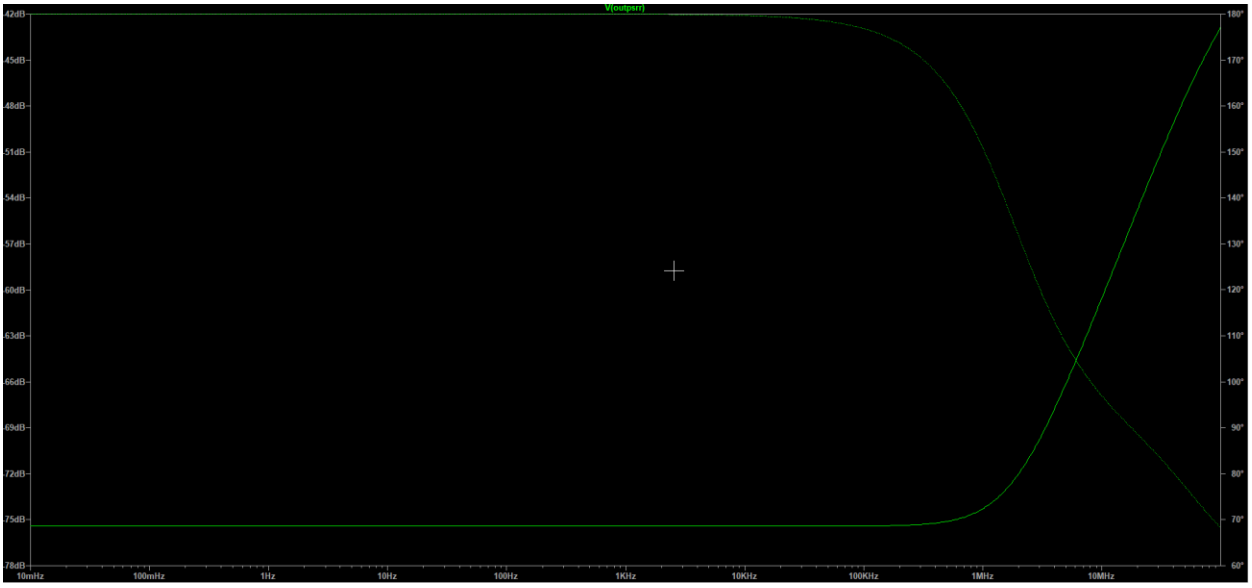


Demonstration of CMRR,PSRR along with proper values.
Simulation used: .ac dec 100 .01 100Meg

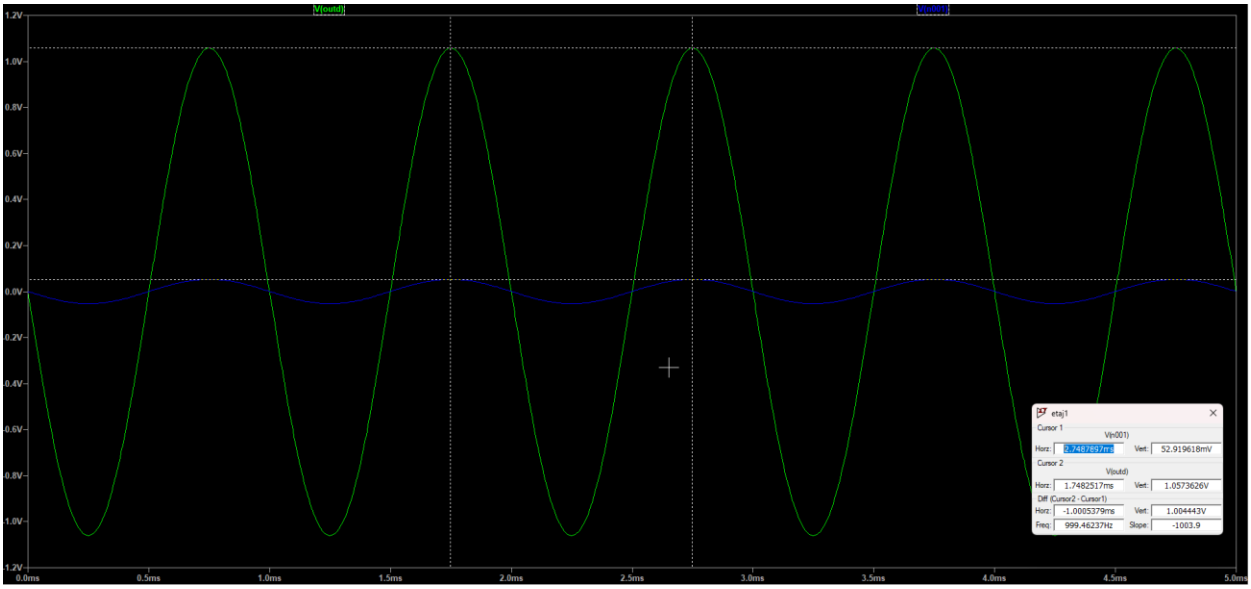
CMRR:



PSRR:

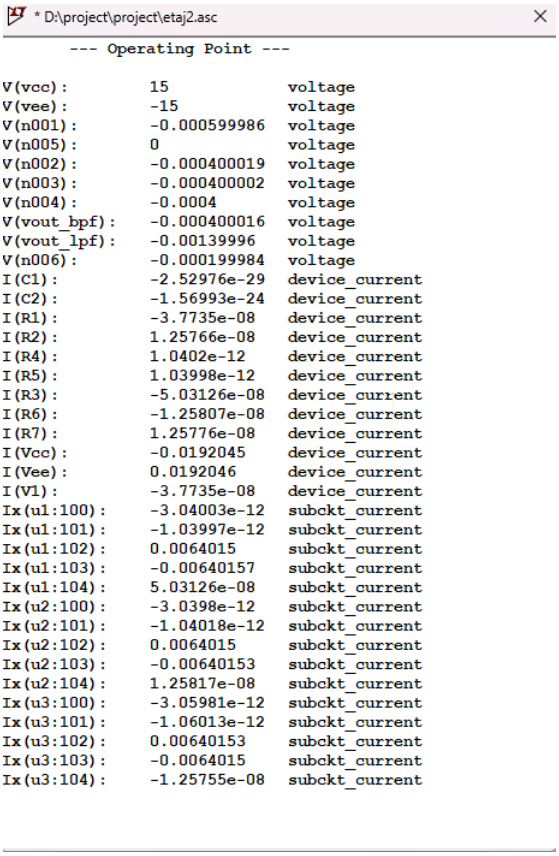


Demonstration of linearity conditions
Simulation used: .tran 0 5m 0



3.2.Characterization of Stage 2

DCOP Parameters:

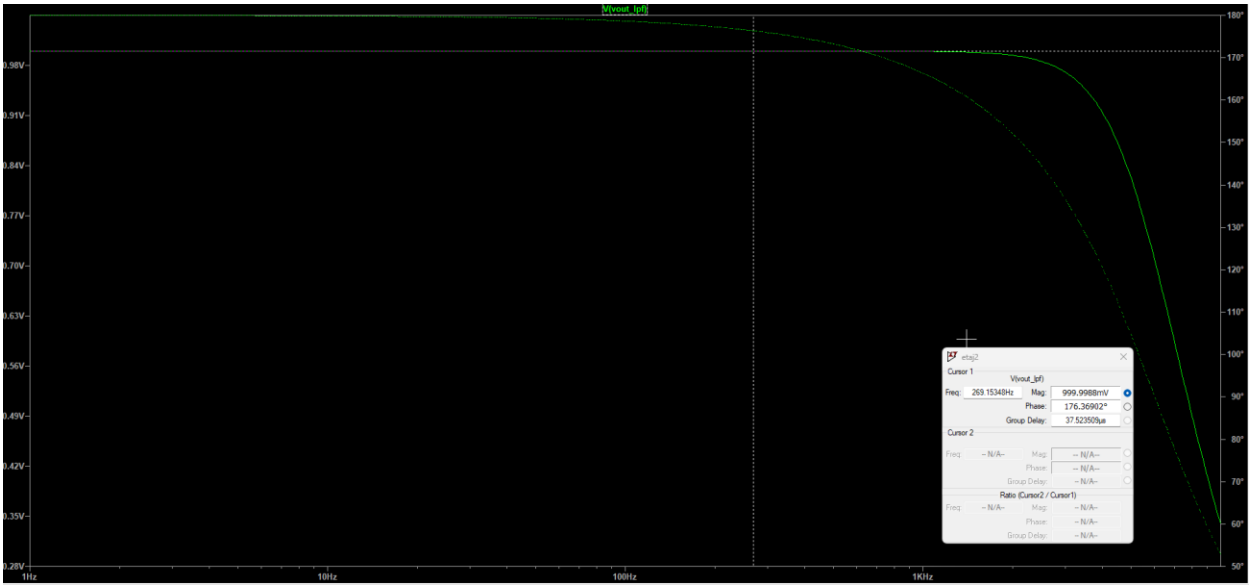


* D:\project\project\etaj2.asc

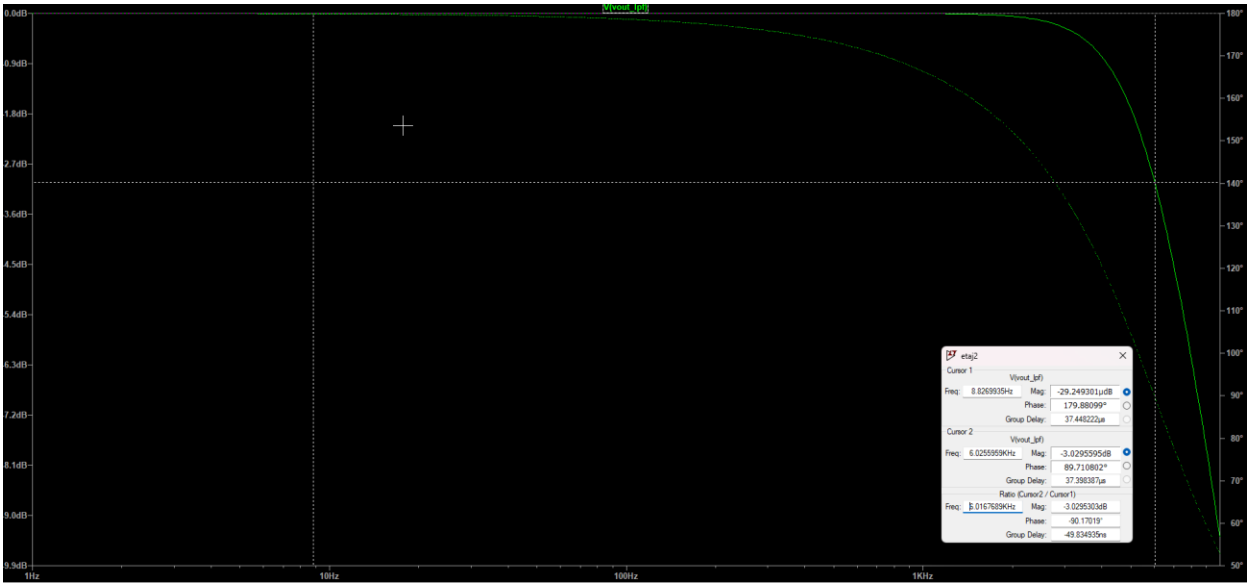
--- Operating Point ---

V(vcc):	15	voltage
V(vee):	-15	voltage
V(n001):	-0.000599986	voltage
V(n005):	0	voltage
V(n002):	-0.000400019	voltage
V(n003):	-0.000400002	voltage
V(n004):	-0.0004	voltage
V(vout_bpf):	-0.000400016	voltage
V(vout_lpf):	-0.00139996	voltage
V(n006):	-0.000199984	voltage
I(C1):	-2.52976e-29	device_current
I(C2):	-1.56993e-24	device_current
I(R1):	-3.7735e-08	device_current
I(R2):	1.25766e-08	device_current
I(R4):	1.0402e-12	device_current
I(R5):	1.03998e-12	device_current
I(R3):	-5.03126e-08	device_current
I(R6):	-1.25807e-08	device_current
I(R7):	1.25776e-08	device_current
I(Vcc):	-0.0192045	device_current
I(Vee):	0.0192046	device_current
I(V1):	-3.7735e-08	device_current
Ix(u1:100):	-3.04003e-12	subckt_current
Ix(u1:101):	-1.03997e-12	subckt_current
Ix(u1:102):	0.0064015	subckt_current
Ix(u1:103):	-0.00640157	subckt_current
Ix(u1:104):	5.03126e-08	subckt_current
Ix(u2:100):	-3.0398e-12	subckt_current
Ix(u2:101):	-1.04018e-12	subckt_current
Ix(u2:102):	0.0064015	subckt_current
Ix(u2:103):	-0.00640153	subckt_current
Ix(u2:104):	1.25817e-08	subckt_current
Ix(u3:100):	-3.05981e-12	subckt_current
Ix(u3:101):	-1.06013e-12	subckt_current
Ix(u3:102):	0.00640153	subckt_current
Ix(u3:103):	-0.0064015	subckt_current
Ix(u3:104):	-1.25755e-08	subckt_current

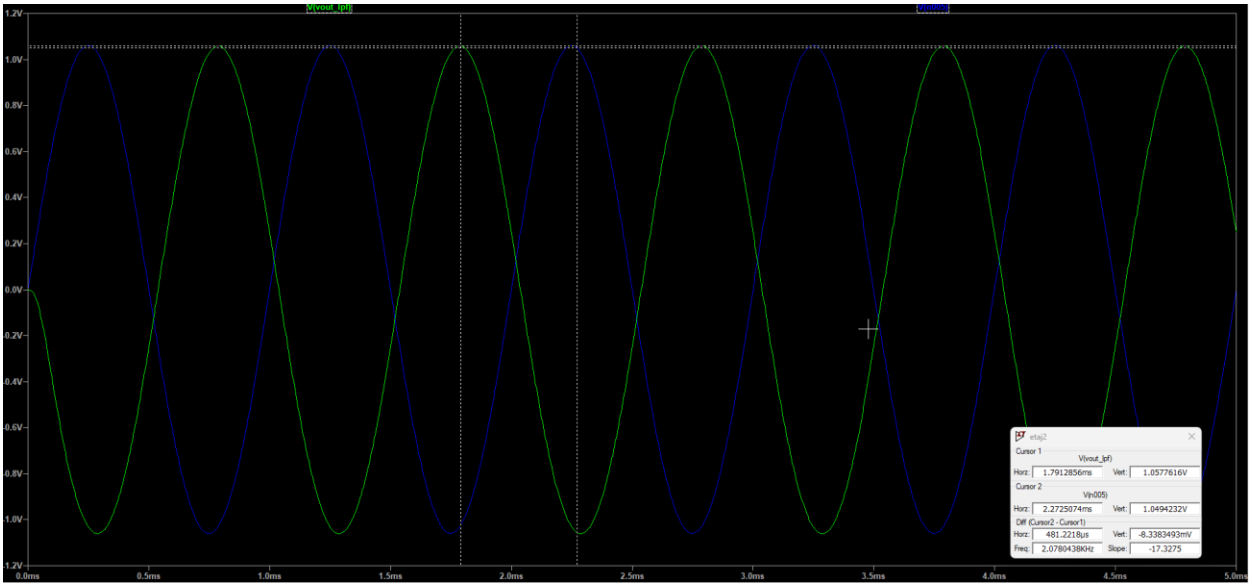
Demonstration of proper band
Simulation used: .ac dec 100 1 10k



Demonstration of GBW.
Simulation used: .ac dec 100 1 10k



Demonstration of linearity.
Simulation used: .tran 0 5m 0



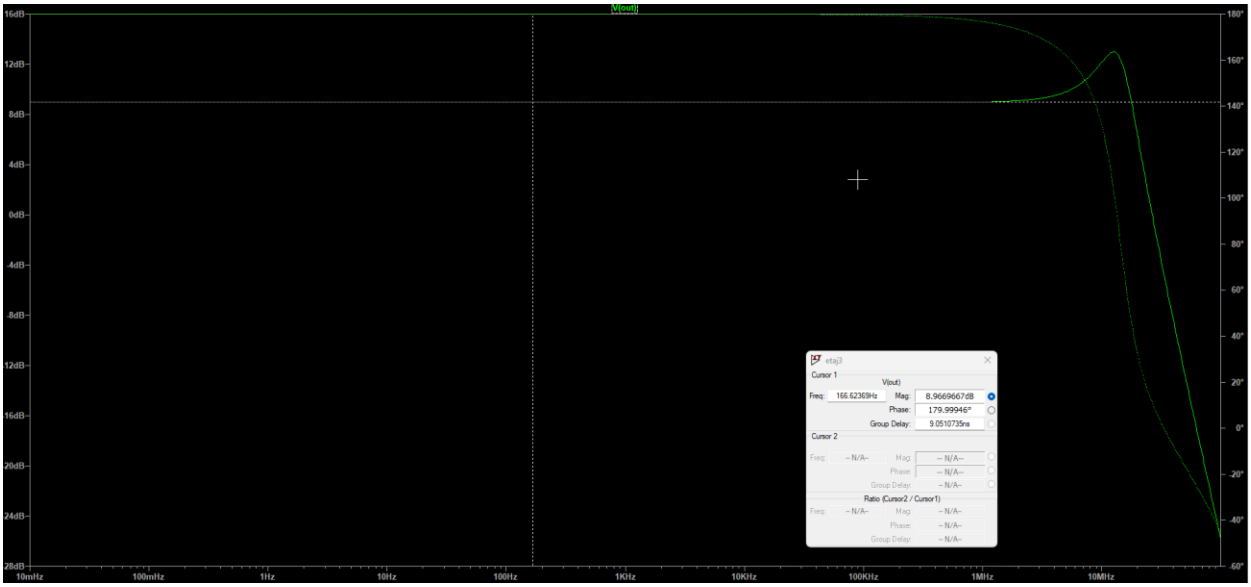
3.3.Characterization of Stage 3

DCOP Parameters:

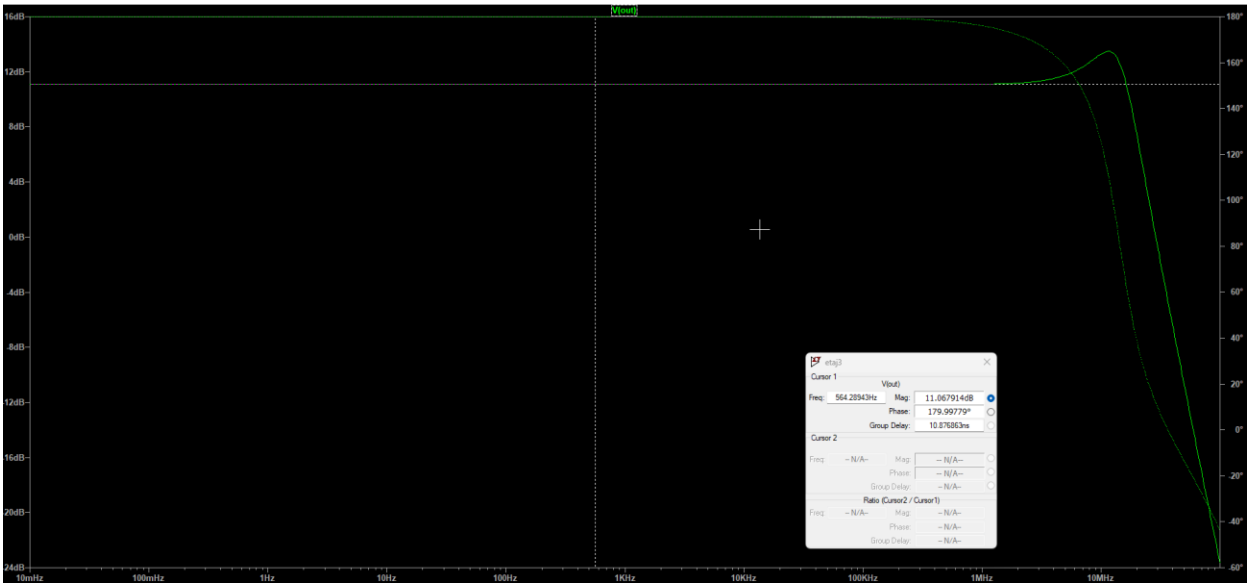
```
      --- Operating Point ---

V(in):          0              voltage
V(c1):          0              voltage
V(n004):        -1.12482e-06   voltage
V(out):         -0.00220569    voltage
V(n002):        -0.000399998   voltage
V(n003):        -0.000399998   voltage
V(n001):        -7.18703e-07   voltage
V(c2):          0              voltage
V(c3):          15             voltage
V(c4):          0              voltage
V(vcc):         15             voltage
V(vee):         -15            voltage
V(n005):        -1.43483e-06   voltage
I(R2):          3.98874e-10    device_current
I(Rf):          -1.80569e-07   device_current
I(R3):          1.79371e-07    device_current
I(R4):          3.9928e-10     device_current
I(R1):          3.98564e-10    device_current
I(S1):          -1.79371e-07   device_current
I(S2):          -3.9928e-10    device_current
I(S3):          -3.98874e-10   device_current
I(S4):          -3.98564e-10   device_current
I(Vin):         -1.80568e-07   device_current
I(Vc1):         0              device_current
I(Vc2):         0              device_current
I(Vc3):         0              device_current
I(Vc4):         0              device_current
I(Vcc):         -0.0064015     device_current
I(Vee):         0.0064017      device_current
Ix(u1:100):     -3.04021e-12   subckt_current
Ix(u1:101):     -1.0398e-12    subckt_current
Ix(u1:102):     0.0064015      subckt_current
Ix(u1:103):     -0.0064017     subckt_current
Ix(u1:104):     1.80569e-07    subckt_current
```

Demonstration of all of the gain steps obtained.
Simulation used: .ac dec 100 .01 100Meg

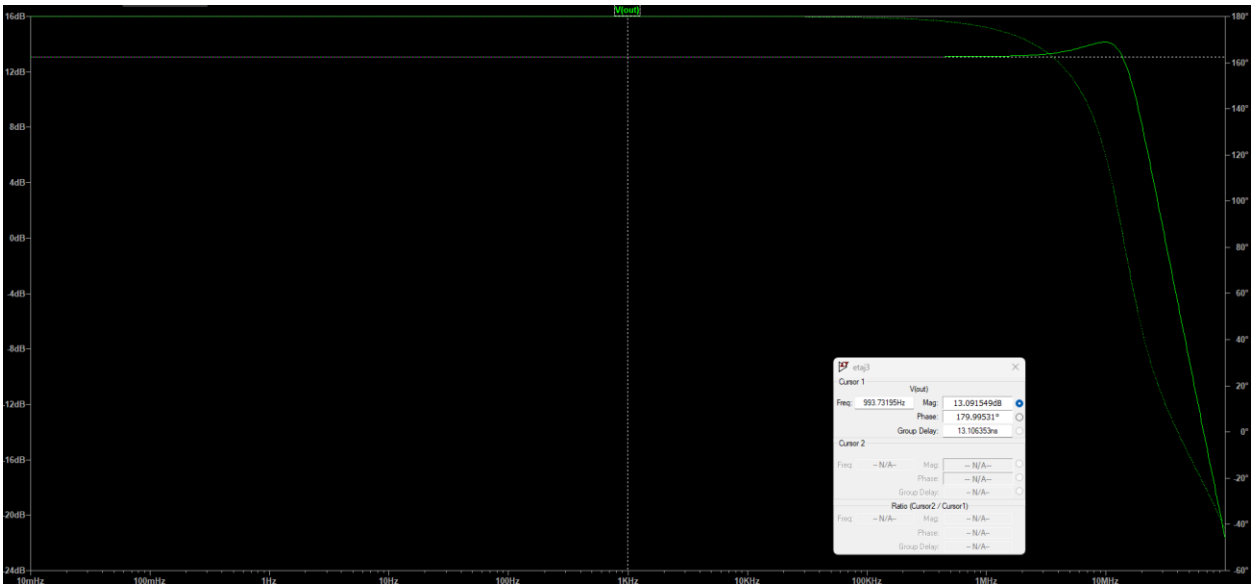
SW1:



SW2:



SW3:

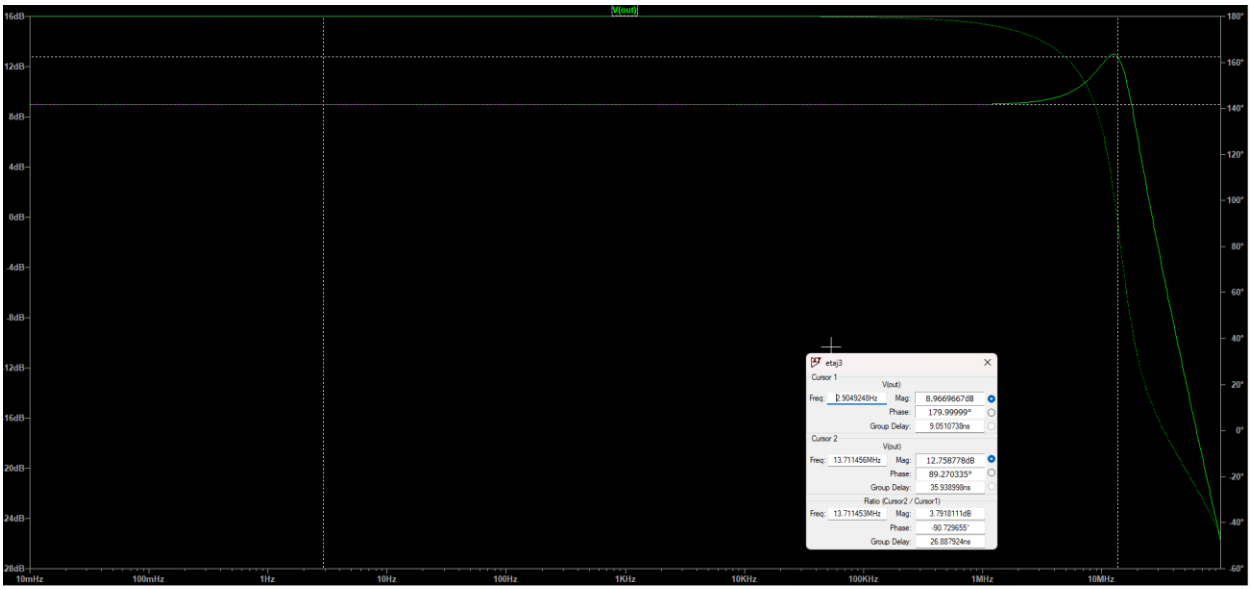

V(out)
16dB
12dB
8dB
4dB
0dB
-4dB
-8dB
-12dB
-16dB
-20dB
-24dB
180°
160°
140°
120°
100°
80°
60°
40°
20°
0°
-20°
-40°
-60°
10mHz
100mHz
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
etaj3
Cursor 1
V(out)
Freq: 993.73195Hz
Mag: 13.091549dB
Phase: 179.99531°
Group Delay: 13.106353ns
Cursor 2
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
Ratio (Cursor2 / Cursor1)
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--

SW4:

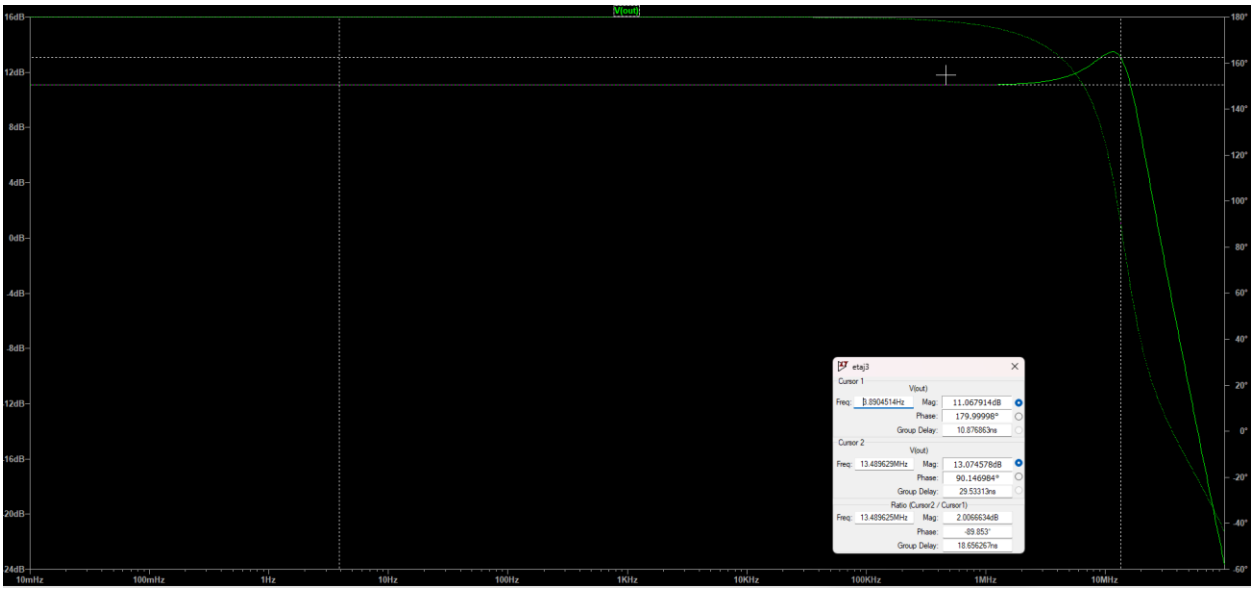

V(out)
16dB
12dB
8dB
4dB
0dB
-4dB
-8dB
-12dB
-16dB
-20dB
180°
160°
140°
120°
100°
80°
60°
40°
20°
0°
-20°
-40°
-60°
10mHz
100mHz
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
etaj3
Cursor 1
V(out)
Freq: 993.73195Hz
Mag: 14.94106dB
Phase: 179.9944°
Group Delay: 15.651996ns
Cursor 2
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
Ratio (Cursor2 / Cursor1)
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--

Demonstration off all band values for the gain steps.
Simulation used: .ac dec 100 .01 100Meg

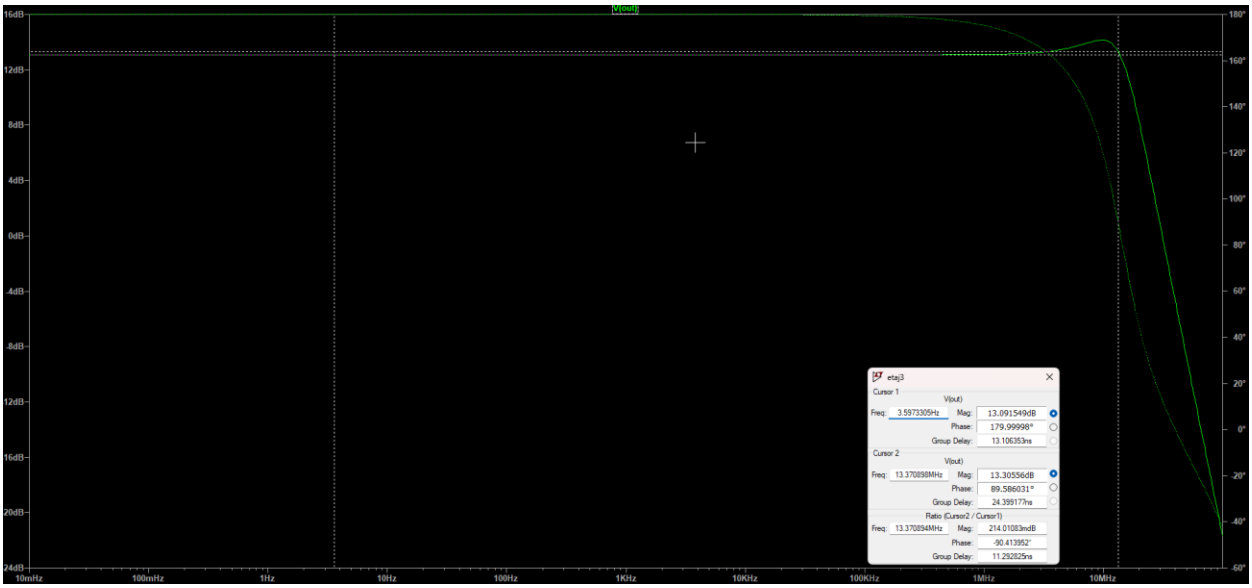
SW1:



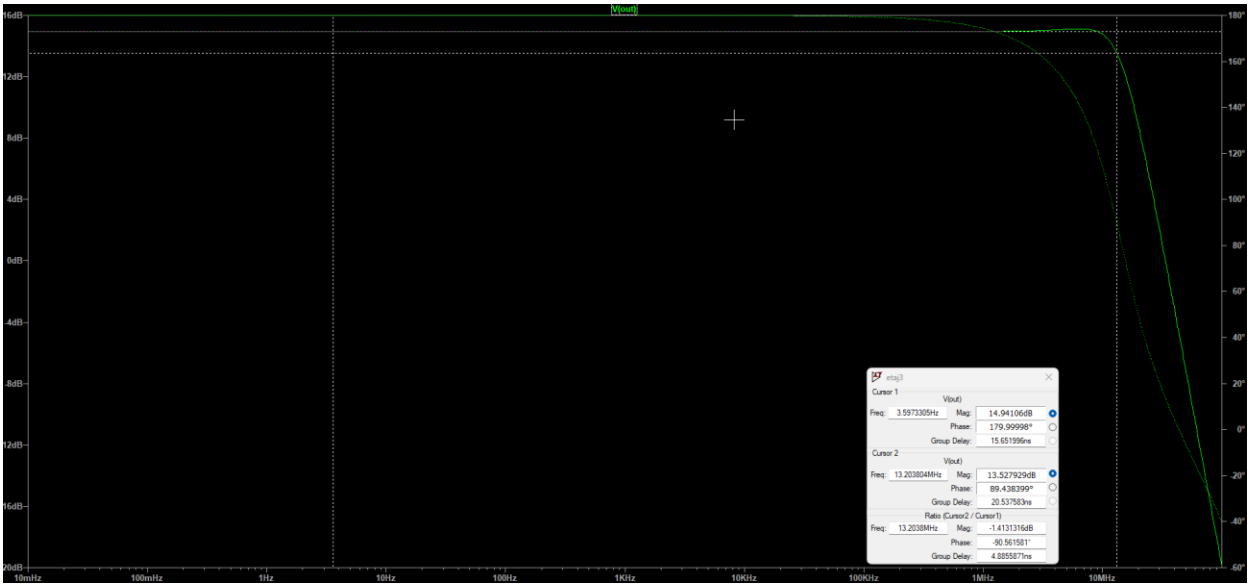
SW2:



SW3:

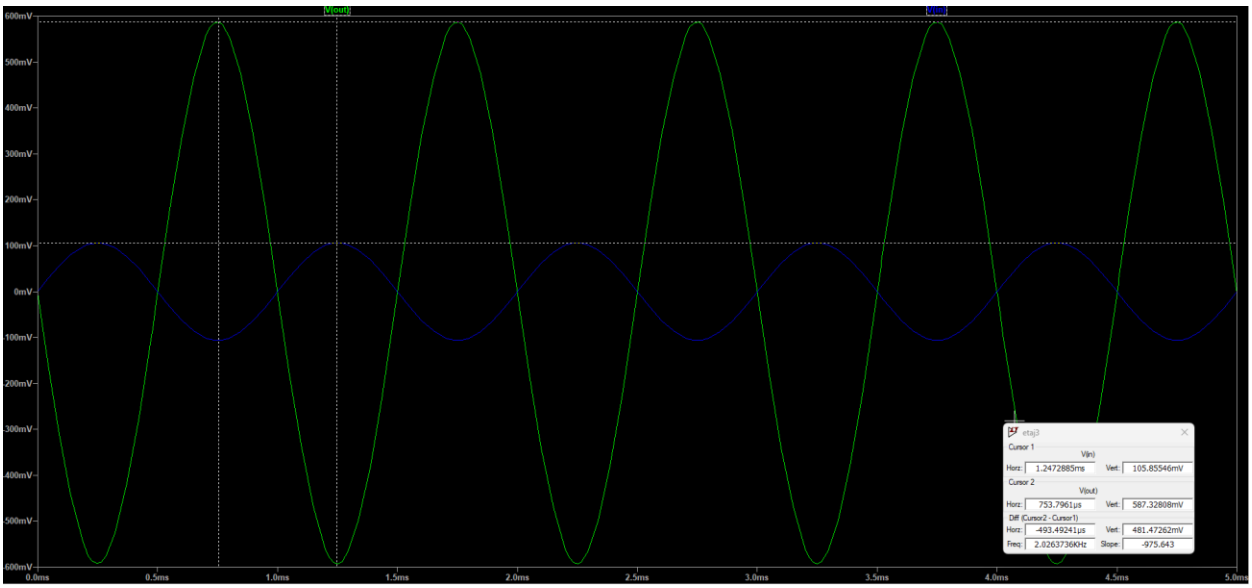

Vout
16dB
12dB
8dB
4dB
0dB
-4dB
-8dB
-12dB
-16dB
-20dB
-24dB
180°
160°
140°
120°
100°
80°
60°
40°
20°
0°
-20°
-40°
-60°
10mHz
100mHz
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
etaj3
Cursor 1
Vout)
Freq: 3.5973305Hz
Mag: 13.091549dB
Phase: 179.99998°
Group Delay: 13.106353ns
Cursor 2
Vout)
Freq: 13.370898MHz
Mag: 13.30556dB
Phase: 89.586031°
Group Delay: 24.399177ns
Ratio (Cursor2 / Cursor1)
Freq: 13.370894MHz
Mag: 214.01083mdB
Phase: -90.413952°
Group Delay: 11.292825ns

SW4:

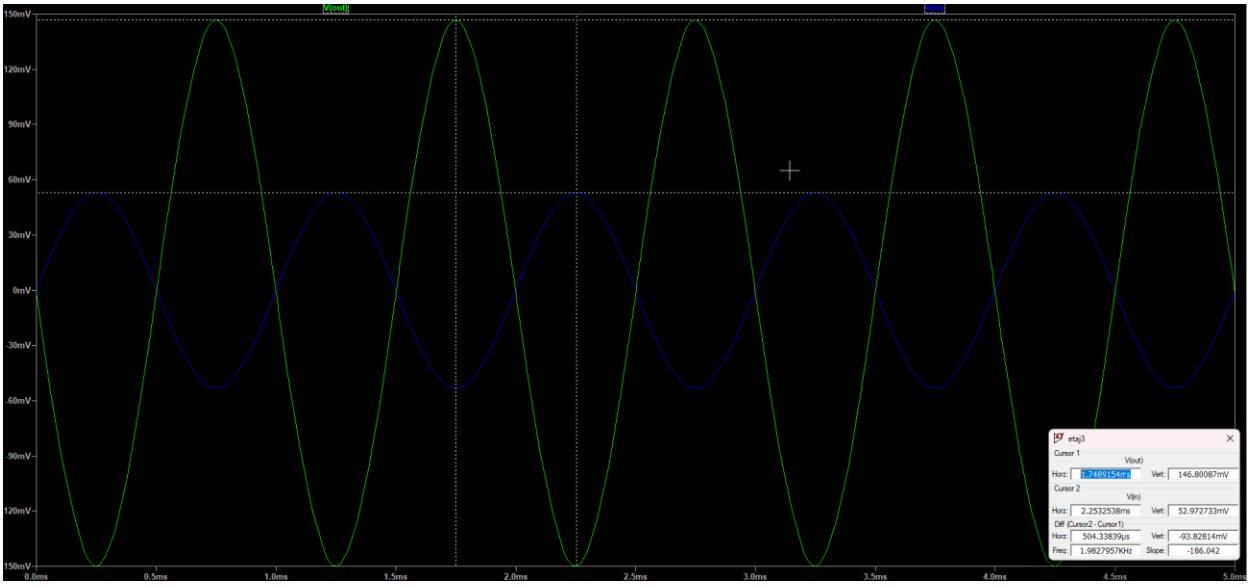

Vout
16dB
12dB
8dB
4dB
0dB
-4dB
-8dB
-12dB
-16dB
-20dB
180°
160°
140°
120°
100°
80°
60°
40°
20°
0°
-20°
-40°
-60°
10mHz
100mHz
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
etaj3
Cursor 1
Vout)
Freq: 3.5973305Hz
Mag: 14.94106dB
Phase: 179.99998°
Group Delay: 15.651996ns
Cursor 2
Vout)
Freq: 13.203804MHz
Mag: 13.527929dB
Phase: 89.438399°
Group Delay: 20.537583ns
Ratio (Cursor2 / Cursor1)
Freq: 13.2038MHz
Mag: -1.4131316dB
Phase: -90.561581°
Group Delay: 4.885587ns

Demonstration of THD and linearity
Simulation used: .tran 0 5m 0 50u

Linearity > specs for minimum gain and maximum input amplitude (for THD < 1%)



Linearity > specs for maximum gain and minimum input amplitude (for THD < 1%)



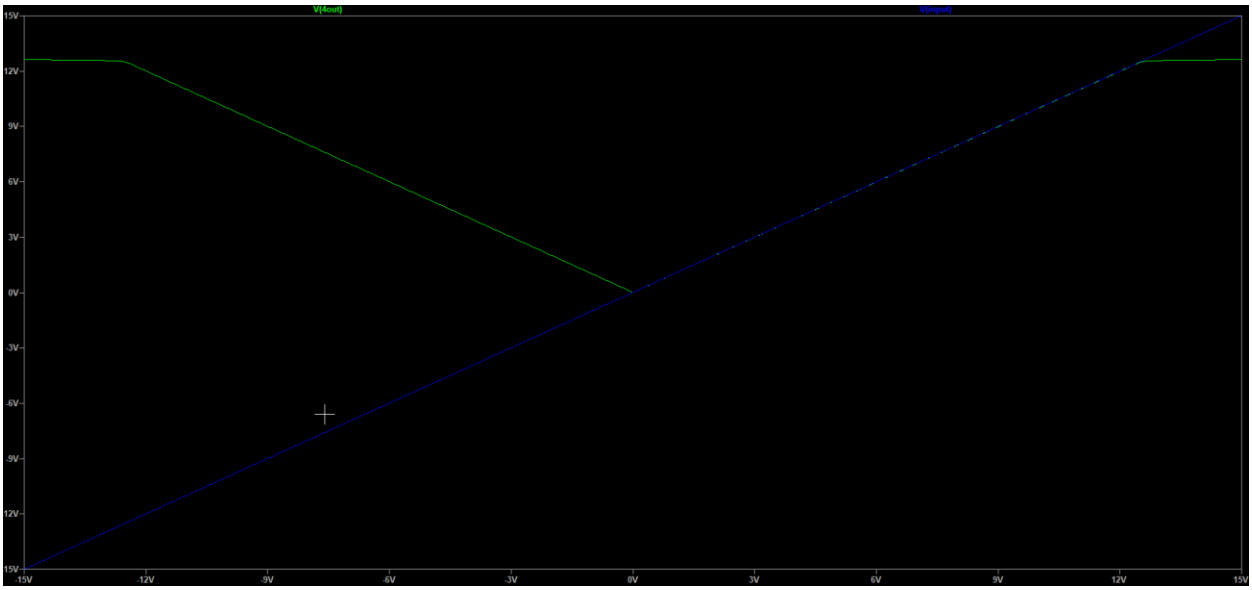
3.4.Characterization of Stage 4

DCOP Parameters:

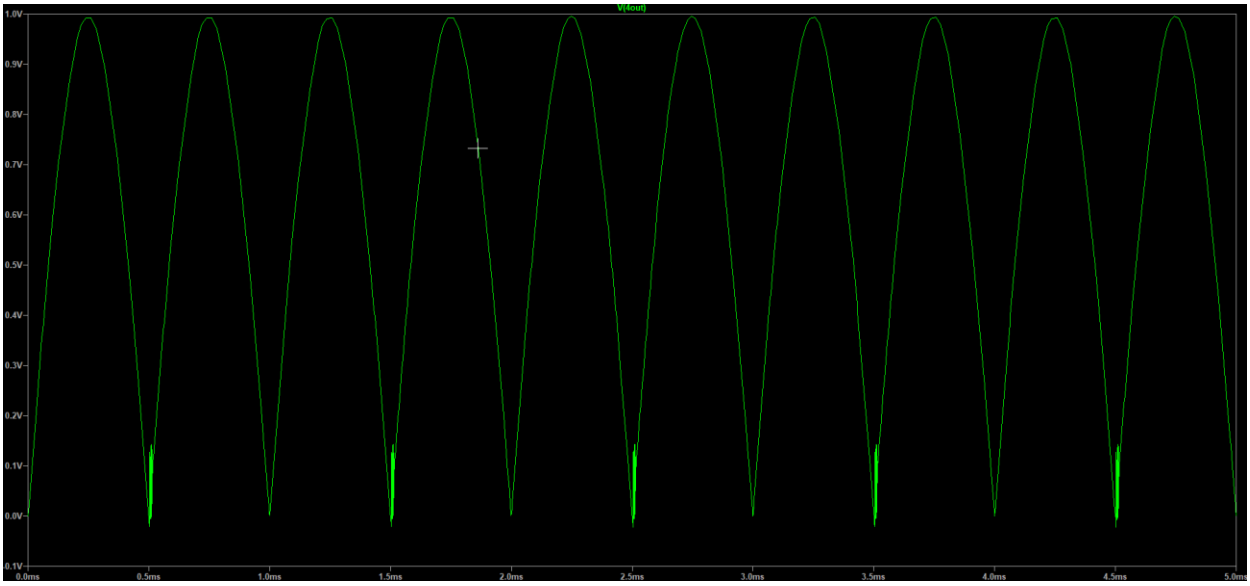
* D:\project\project\etaj4.asc

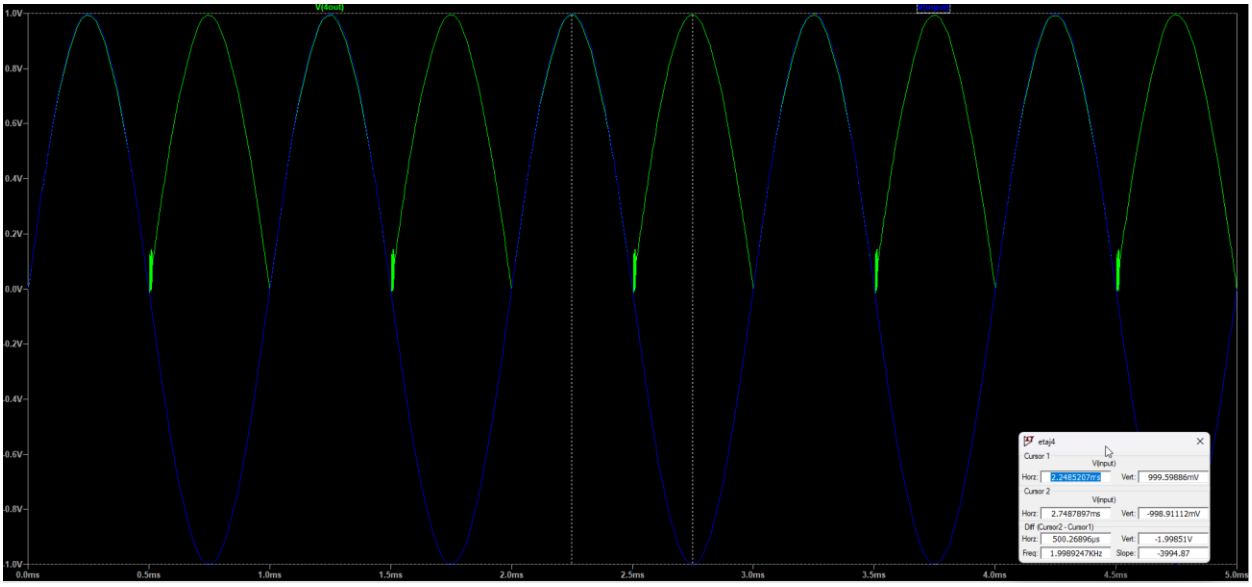
```
        --- Operating Point ---

V(n001):        0.998999        voltage
V(input):       1               voltage
V(n002):        0.998998        voltage
V(n003):        -0.771679       voltage
V(vcc):         15              voltage
V(-vcc):        -15             voltage
V(4out):        0.998595        voltage
I(D3):          -1.78068e-12    device_current
I(D4):          0.0906042       device_current
I(R1):          -1.00138e-07    device_current
I(R2):          -9.88208e-11    device_current
I(V1):          -1.00138e-07    device_current
I(V2):          -0.012803       device_current
I(V3):          -0.103407       device_current
Ix(u4:100):     -9.99429e-08    subckt_current
Ix(u4:101):     1.00039e-07     subckt_current
Ix(u4:102):     0.0064015       subckt_current
Ix(u4:103):     -0.0970057      subckt_current
Ix(u4:104):     0.0906042       subckt_current
Ix(u2:100):     9.70335e-11     subckt_current
Ix(u2:101):     9.86988e-11     subckt_current
Ix(u2:102):     0.00640152      subckt_current
Ix(u2:103):     -0.00640152     subckt_current
Ix(u2:104):     -9.86988e-11    subckt_current
```

Demonstration of casting in DC sweep
Simulation used: .dc V1 -15 15 0.01



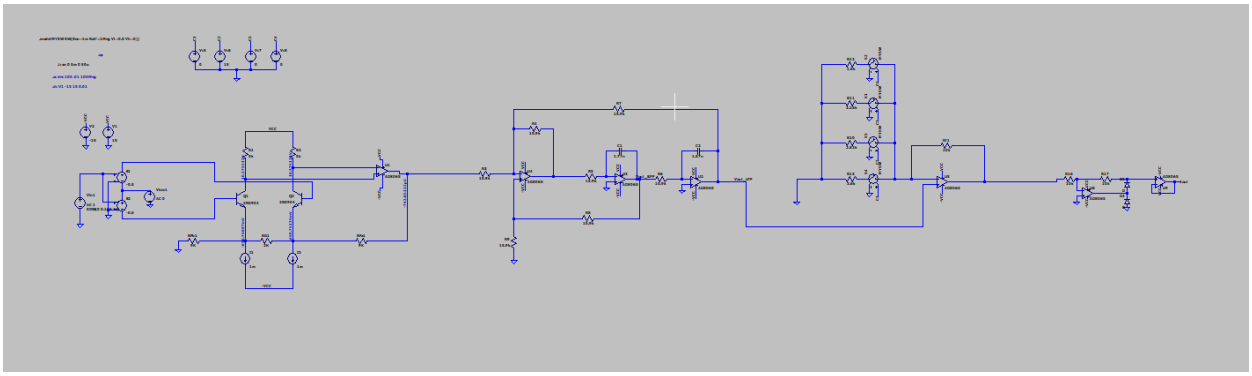
Demonstration of implementing circuit functionality
Simulation used: .tran 0 5m 0 50u



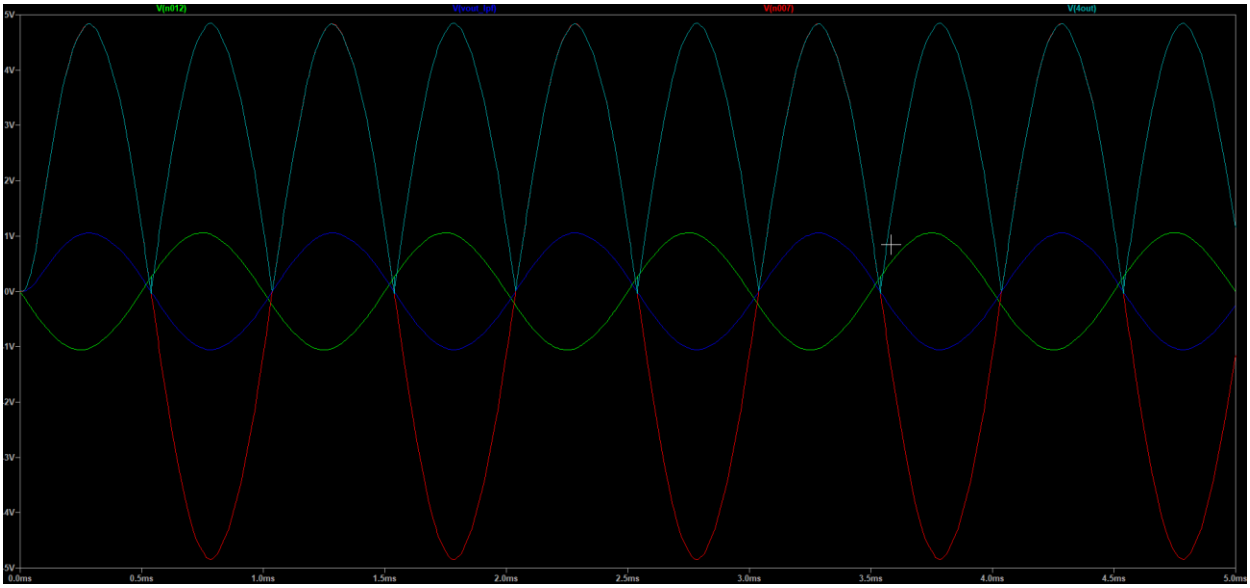


4. Validation and characterisation of the analog interface

The complete analog interface circuit is shown below. It integrates all the designed stages, including all the previously dimensioned components.



Demonstration of .tran 0 5m 0 50u simulation:



5. Conclusion

	Specifications	Measurements
|Gain| stage 1	10	9.997
|H0| stage 2	1	1
Bandwidth stage 2	6000	6.016
Gain 1 stage 3	9dB	3.6
Gain 2 stage 3	11dB	2.82
Gain 3 stage 3	13dB	2.23
Gain 4 stage 3	15dB	1.8
|Gain| stage 4	1	1

Following the measurements of each stage and comparing the results with the required specifications, there are no significant errors or differences, which indicates the correct functionality of the circuit within the required parameters.

The design, dimensioning, and characterization of the proposed analog interface have demonstrated the functionality of the circuit, according to the imposed requirements. The results obtained from the AC and Transient simulations confirm the correct operation of the circuit, validating the design parameters, namely gain, bandwidth, and linear range.