Appendix A

Further Memory Fault Modeling

Extended Listing

The fault models in this appendix include those not described in chapter eight. It is recommended that the reader first become familiar with the faults covered in that chapter as they describe real manufacturing defects which must be covered during memory testing. The fault models covered here will help in the understanding of nomenclature and will aid readers as they review other literature on memory testing. Some of the fault models covered here are only mathematical curiosities while others provide helpful insight.

1. LINKED FAULTS

Since more than one defect can exist in a memory, the multiple faults can interact. As these interact they are referred to as linked fault models. Fault models that are linked can be of similar or dissimilar types [207]. They can also work in such a manner that one fault can mask the behavior of another fault. The occurrence of this kind of a fail must be rare in order to get reasonable chip yield. The probability of having two fails needs to be rarer still. The probability of having two fails, that in fact interact, must be exceedingly rare. Therefore linked faults should normally be of little concern. The only possibility for linked faults, which would be of concern, is if one defect activates two faults, which in turn are linked.

When multiple faults do not interact they are said to be *unlinked.* This is the normal case with multiple faults.

2. COUPLING FAULT MODELS

2.1 Inversion coupling fault

An inversion coupling fault involves an aggressor and a victim cell where the aggressor causes the victim cell's data to invert. A Markov diagram of this fault model is shown in figure A-1. This figure illustrates an example whereby any transition in cell "j" from a "0" to a "1" causes cell "i" to invert. No known defects will cause this type of defective operation nor is it known if such a fault has ever been seen.

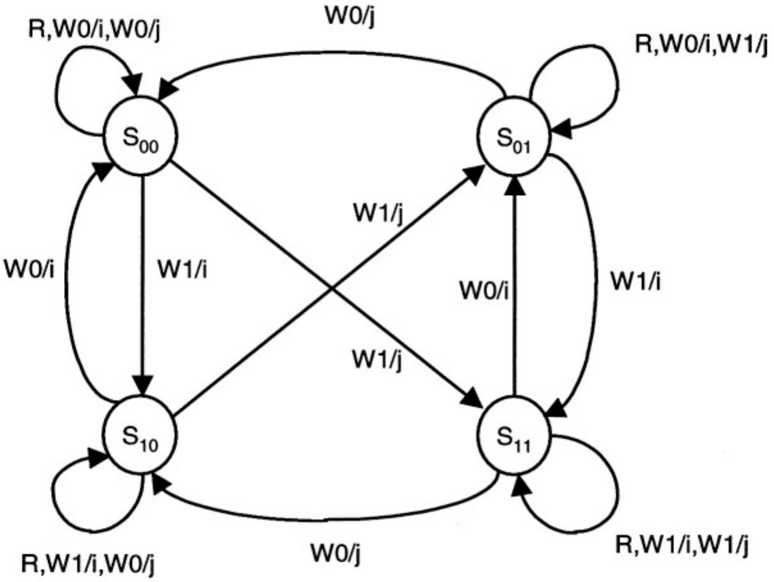


Figure A-1. Markov diagram of an inversion coupling fault.

2.2 Idempotent coupling fault

An idempotent coupling fault describes an event where writing a specific state in an aggressor cell causes a victim cell to go to a specific unintended state. Figure 8-8 shows an idempotent coupling fault where writing cell "j" to a "1" erroneously forces cell "i" to a "1" as well [208]. The source of the name for this fault is curious, although idempotent is a well understood mathematical term [209]. After some searching and dialog with others in this field, it seems that the reason for the name "idempotent" and its source have been lost in the annals of time. Since idempotent can refer to having the same singular result, even if an operation is repeated multiple times, it is possible that the idempotent coupling fault was so named in converse to the inversion coupling fault. The inversion coupling fault gets different results in the victim cell based on the number of times the aggressor cell is written. In contrast is the idempotent coupling fault, where a single erroneous value is maintained in the victim cell, as long as the victim cell itself is not purposely re-written.

2.3 Complex coupling fault

A complex coupling fault describes a defect where multiple cells must be in a specific state in order to sensitize a victim cell to a certain aggressor. A k-complex coupling fault is one where k is a value describing the number of cells which must interact [210]. If k is 5, then k-1 or 4 cells must be in a specific state in order for a 5th cell's transition to cause a failure in the victim cell.

2.4 State coupling fault

A state coupling fault does not require an operation to be performed nor a transition to occur. If an aggressor cell is in a specific state then the victim cell is forced to an erroneous state.

2.5 V coupling fault

A fault which requires two aggressor cells to transition, thereby forcing more charge into a victim cell and causing it to flip, is described by the V-type coupling fault model [211]. If only one of the aggressor cells transitions then the victim cell will not go to an erroneous state. Having two cells transition in direct adjacency to a victim cell can only happen in certain circumstances. If all of the bits in a word are written into a single sub array, then a cell in one row can be immediately adjacent to one cell and diagonally adjacent to another. If there is a two-to-one column decode, then a victim cell can be wedged between the two aggressor cells. Further, if a multi-port memory is employed then two ports can be writing to two cells adjacent to the victim cell and thus cause it to flip. In the case of a multi-port memory, the adjacencies can be from any pair of cells in the eight cells surrounding the base cell.

3. NEIGHBORHOOD PATTERN SENSITIVE FAULT MODELS EXPANDED

3.1 Pattern Sensitive Fault Model

The pattern sensitive fault model is the all encompassing form of the neighborhood pattern sensitive fault model (NPSF). When the neighborhood becomes all of the cells in the memory the fault model is referred to as the pattern sensitive fault model (PSF) and is sometimes called an unrestricted PSF [212, 213,214].

3.2 Active Neighborhood Pattern Sensitive Fault Model

The active or dynamic neighborhood pattern sensitive fault model [215, 216] refers to a defect that is exhibited when one of the neighborhood cells transitions causing a deleterious impact on the base or victim cell. The other cells in the neighborhood must be in specific states as is the case for a NPSF.

3.3 Passive Neighborhood Pattern Sensitive Fault Model

A passive neighborhood pattern sensitive fault model describes a defect where, as all of the neighborhood cells are in specific states, the base or victim cell is unable to transition. When active and passive neighborhood pattern sensitive faults are collectively discussed they sometimes are referred to by the acronym APNPSF.

3.4 Static Neighborhood Pattern Sensitive Fault Model

A static neighborhood pattern sensitive fault model describes a defect where, as all of the neighborhood cells are in specific states, the base or victim cell is forced to a specific erroneous state.

4. RECOVERY FAULT MODELS

4.1 Sense amplifier recovery fault model

A sense amplifier can saturate due to numerous reads of one data type [217]. When the opposite data type is read the sense amplifier has a defective tendency toward the previous data type and thus does not read correctly. This type of defective operation is described by the sense amplifier recovery fault model.

4.2 Write recovery fault model

When a write is performed, the address decoder can be slow to recover. This slowness can prevent a new address from being correctly read or written. The subsequent incorrect read or write is described as by the write recovery fault model.

4.3 Slow write recovery fault model

A slow write recovery fault model is similar to the previous write recover fault model [218]. The difference is that in a slow write recovery fault a subsequent read is correct but is delayed in time.

5. STUCK OPEN FAULT MODELS

5.1 Stuck open cell fault model

A cell can have a stuck off transfer device. The transfer device can be open or the gate can simply be stuck-at a zero [219]. In either case the result is a cell, which effectively has a stuck open connection to a bit line. In the case of an SRAM, since a true and a complement bit line are utilized the stuck-open defect may only affect one data type.

5.2 Stuck open bit line fault model

A column bit line can be open part way along its path to the cells [220,221] causing some of the cells can be connected to the bit line and others, beyond the break, are inaccessible. If the sense amplifier and the write driver circuitry are on the same side of the memory array then the cells up to the point of the break can function normally.

6. IMBALANCED BIT LINE FAULT MODEL

Defective cells along a DRAM bit line can be leaking onto the bit line and inducing an erroneous potential. This kind of a defect causes unintended cells to be “accessed” and they in turn drive the bit line into an imbalanced state resulting in incorrect reads. Thus, the name of an imbalanced bit line fault model is utilized. An SRAM can also be impacted by this type of fault if leakage occurs more on one of the bit lines in a pair than on the other.

7. MULTI-PORT MEMORY FAULTS

Faults, which can be sensitized by exercising a single port, are logically referred to as single-port faults [222] and are often use the notation "1PF". Faults, which require two ports to be exercised in order to sensitize a defect, are referred to as two-port faults. These are referred to by the notation "2PF". Faults can impact one or more cells. A single-port fault that impacts one cell or two cells is referred to by the notation "1PF1s" and "1PF2s", respectively. This notation is clearly extensible [223].

A strong fault is one that can be sensitized by performing a single port operation. A weak fault is one that creates insufficient disturbance to result in a fail when only one port is exercised. When multiple ports are exercised, multiple weak faults can cumulatively impact the operation and result in a memory failure. This is similar to the V-type coupling fault.

Appendix B

Further Memory Test Patterns

Extended Listing

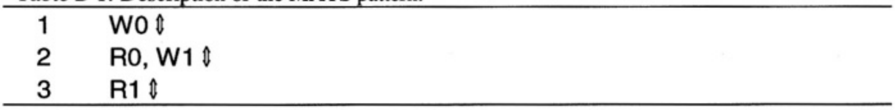
The memory test patterns listed in this appendix are a supplement to those described in chapter nine of this text. The reader should first examine chapter nine and familiarize themselves with the patterns covered there. The patterns included in chapter nine are utterly essential to successfully producing high quality memories and thereby good chips. The patterns contained in this appendix are for reference and are especially helpful as one reads literature on memory testing. Some of the patterns discussed here are only mathematically interesting while others provide very helpful insight.

1. MATS PATTERNS

1.1 MATS

The modified algorithmic test sequence, also known as MATS, is a 4N pattern [224,225]. It is focused on finding stuck-at faults as well as detecting some address decoder faults. MATS has the same length as the Zero-One pattern but is far superior.

Table B-1. Description of the MATS pattern.



1	W0 ⇕
2	R0, W1 ⇕
3	R1 ⇕

1.2 MATS+

The MATS+ pattern requires 5N operations and is considered optimal for unlinked stuck-at faults [226].

Table B-2. Description of the MATS+ pattern.

1	W0 ⇕
2	R0, W1 ⇑
3	R1, W0 ⇓

1.3 MATS++

The MATS++ pattern is an improvement on the Marching 1/0 pattern (covered next in this appendix). It is a 6n pattern and eliminates certain redundancies [227]. (A *redundancy* is a repeat of an operation that does not allow any further faults to be detected. A pattern without redundancies is said to be *irredundant.*) This pattern detects some address decoder faults, stuck-at faults, and transition faults, along with some coupling faults.

Table B-3. Description of the MATS++ pattern.

1	W0 ⇕
2	R0, W1 ⇑
3	R1, W0, R0 ⇓

1.4 Marching 1/0

The Marching 1/0 pattern detects the same faults as the MATS++, but is longer. It is a 14n pattern.

Table B-4. Description of the Marching 1/0 pattern.

1	W0 ⇑
2	R0, W1, R1 ⇑
3	R1, W0, R0 ⇓
4	W1 ⇑
5	R1, W0, R0 ⇑
6	R0, W1, R1 ⇓

2. LETTERED MARCH PATTERNS

2.1 March A

The March A pattern is a 15n pattern. It focuses on detecting linked idempotent coupling faults. It also detects address decoder faults, stuck-at faults, and transition faults not linked with idempotent coupling faults.

Table B-5. Description of the March A pattern.

1	W0 ⇕
2	R0, W1, W0, W1 ⇑
3	R1, W0, W1 ⇑
4	R1, W0, W1, W0 ⇓
5	R0, W1, W0 ⇓

2.2 March B

The March B pattern can detect linked transition and idempotent coupling faults as well as detecting address decoder faults and stuck-at faults [228]. It is a 17n pattern.

Table B-6. Description of the March B pattern.

1	W0 ⇕
2	R0, W1, R1, W0, R0, W1 ⇑
3	R1, W0, W1 ⇑
4	R1, W0, W1, W0 ⇓
5	R0, W1, W0 ⇓

2.3 March C

The March C pattern [229] had the March C- pattern derived from it. The March C is not irredundant, as can be seen in the fourth march element. Chapter nine can be examined for a detailed discussion of the March C- pattern.

Table B-7. Description of the March C pattern.

1	W0 ⇕
2	R0, W1 ⇑
3	R1, W0 ⇑
4	R0 ⇕
5	R0, W1 ⇓
6	R1, W0 ⇓
7	R0 ⇕

2.4 March X

The March X pattern takes 6n cycles and is focused on finding unlinked inversion coupling faults.

Table B-8. Description of the March X pattern.

1	W0 ⇕
2	R0, W1 ⇑
3	R1, W0 ⇓
4	R0 ⇕

2.5 March Y

The March Y pattern enables testing of linked transition and inversion coupling faults. It also detects address decoder faults and stuck-at faults. It is an 8n pattern.

Table B-9. Description of the March Y pattern.

1	W0 ⇕
2	R0, W1, R1 ⇑
3	R1, W0, R0 ⇓
4	R0 ⇕

2.6 March C+, C++, A+, A++ Patterns

The March C+ and March C++ patterns are based on the March C pattern [230]. In the March C+, each read from the March C pattern is replaced with three reads to detect disconnected pull-up and pull-down paths inside a cell. The March C++ pattern includes two delay elements that look for retention type defects. Some refer to a different pattern that is called by the same name. This March C+ pattern is like the PMOVI pattern but with a read "0" element added at the end.

The March A+ and March A++ have the same changes, i.e. the triple reads and the added delay elements, as described in the preceding paragraph.

2.7 March LA

March LA is a 22n pattern with three consecutive writes in each of the key march elements [231]. It can detect all simple faults and many linked faults.

Table B-10. Description of the March LA pattern.

1	W0 ⇕
2	R0, W1, W0, W1, R1 ⇑
3	R1, W0, W1, W0, R0 ⇑
4	R0, W1, W0, W1, R1 ⇓
5	R1, W0, W1, W0, R0 ⇓
6	R0 ⇓

2.8 March SR+

The march test for simple realistic faults, also known as March SR+, is an 18n pattern [232]. It detects stuck-at faults, transition faults, coupling faults, and numerous other faults as well. Further, the double back-to-back read detects deceptive destructive reads.

Table B-11. Description of the March SR+ pattern.

1	W0 ⇓
2	R0, R0, W1, R1, R1, W0, R0 ⇑
3	R0 ⇓
4	W1 ⇑
5	R1, R1, W0, R0, R0, W1, R1 ⇓
6	R1 ⇑

This pattern was further enhanced by the inclusion of a delay to detect subtle retention faults. This is referred to as a March SRD+ pattern.

Table B-12. Description of the March SRD+ pattern.

1	W0 ⇓
2	R0, R0, W1, R1, R1, W0, R0 ⇑
3	Pause
4	R0 ⇓
5	W1 ⇑
6	R1, R1, W0, R0, R0, W1, R1 ⇓
7	Pause
8	R1 ⇑

3. IFA PATTERNS

3.1 9N Linear

Some patterns have become known simply by their numbers. One such pattern is the 9N linear test algorithm [233]. It is also often referred to as the inductive fault analysis-9 pattern or IFA-9. This pattern is commonly used and employs a pause for retention testing.

Table B-13. Description of the 9N linear test algorithm.

1	W0 ⇕
2	R0, W1 ⇑
3	R1, W0 ⇑
4	R0, W1 ⇓
5	R1, W0 ⇓
6	Pause
7	R0, W1 ⇑
8	Pause
9	R1 ⇑

3.2 13N

The 13N pattern detects coupling faults for bits within the same word [234,235]. This pattern is also referred to as the inductive fault analsysis-13 or IFA-13 pattern. Multiple background data types are required. Chapter nine can be examined for a discussion on background data types, which are needed in some patterns. The 13N pattern was developed to detect stuck-open cell errors.

Table B-14. Description of the 13N pattern.

1	W0 ⇕
2	R0, W1, R1 ⇑
3	R1, W0, R0 ⇑
4	R0, W1, R1 ⇓
5	R1, W0, R0 ⇓
6	Pause
7	R0, W1 ⇑
8	Pause
9	R1 ⇑

4. OTHER PATTERNS

4.1 MovC

The movC was developed to ease BIST pattern implementation [236]. It is not, however, irredundant. The pattern requires 33N for each data background type.

Table B-15. Description of the movC pattern.

1	W0 ⇕
2	R0, W0, W1, R1 ⇓
3	R1, W1, W0, R0 ⇓
4	R0, W0, W1, R1 ⇓
5	R1, W1, W0, R0 ⇓
6	R0, W0, W1, R1 ⇑
7	R1, W1, W0, R0 ⇑
8	R0, W0, W1, R1 ⇑
9	R1, W1, W0, R0 ⇑

4.2 Moving Inversion

The moving inversion or MOVI pattern [237] was the precursor to the PMOVI pattern discussed in chapter nine. It involved all of the elements of the PMOVI pattern but repeated them based on the number of address inputs to the memory.

4.3 Butterfly

The butterfly pattern is quite complicated but does take fewer steps than the galloping pattern. The essence of the butterfly pattern is that the base cell is modified following a walking algorithm. After each write of a base cell, the four cells adjacent to it are read. These are in the north, south, east, and west directions. Once these four cells are read the base cell is again read. The butterfly pattern may be continued by reading the next farther out cells in these four directions, followed again by the base cell. The distance continues to be doubled until the edge of the memory or sub-array is reached. It can be seen that this pattern is rather convoluted and only DRAMs have been helped uniquely through this test.

5. SMARCH

The SMARCH pattern was described in chapter nine. The pseudo-code for this pattern is described below.

Table B-16. Pseudo-code description of the SMARCH pattern.

```
// Initialize memory to all 0s
for i = 0..N {
    for j = 0..m { Rx, W0 }
    for j = 0..m { W0, R0 }
}
// like a R0, W1, R1, W1 ⇑ march pattern element
for i = 0..N {
    for j = 0..m { R0, W1 }
    for j = 0..m { R1, W1 }
}
// like a R1, W0, R0, W0 ⇑ march pattern element
for i = 0..N {
    for j = 0..m { R1, W0 }
    for j = 0..m { R0, W0 }
}
// like a R0, W1, R1, W1 ⇓ march pattern element
for i = N..0 {
    for j = 0..m { R0, W1 }
    for j = 0..m { R1, W1 }
}
// like a R1, W0, R0, W0 ⇓ march pattern element
for i = N..0 {
    for j = 0..m { R1, W0 }
    for j = 0..m { R0, W0 }
}
// Read all the cells at 0
for i = 0..N {
    for j = 0..m { R0, W0 }
    for j = 0..m { W0, R0 }
}
```

6. PSEUDO-RANDOM

Pseudo-random patterns were described in chapter nine. In table B-16 a five-bit pseudo-random sequence is provided for reference. Note that the first and 32nd entries match as do the second and 33rd entries. After 31 cycles the pseudo-random sequence has re-started. Note also that the all zeros state is not present.

Table B-17. Example five-bit pseudo-random sequence.

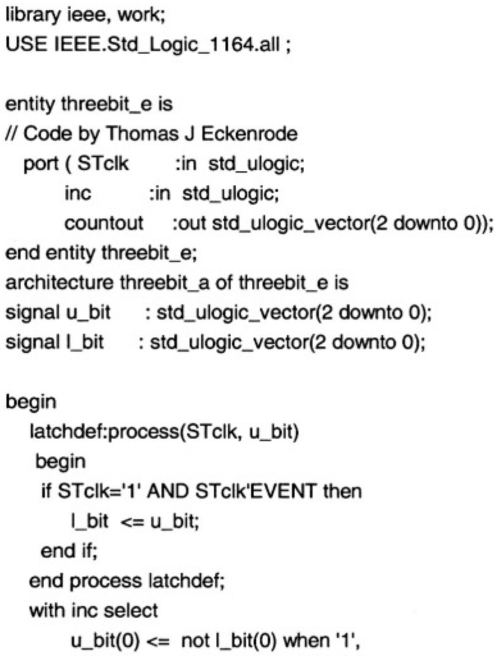
Pass	X[0]	X[1]	X[2]	X[3]	X[4]
1	1	0	0	0	0
2	0	1	0	0	0
3	1	0	1	0	0
4	0	1	0	1	0
5	1	0	1	0	1
6	1	1	0	1	0
7	1	1	1	0	1
8	0	1	1	1	0
9	1	0	1	1	1
10	1	1	0	1	1
11	0	1	1	0	1
12	0	0	1	1	0
13	0	0	0	1	1
14	1	0	0	0	1
15	1	1	0	0	0
16	1	1	1	0	0
17	1	1	1	1	0
18	1	1	1	1	1
19	0	1	1	1	1
20	0	0	1	1	1
21	1	0	0	1	1
22	1	1	0	0	1
23	0	1	1	0	0
24	1	0	1	1	0
25	0	1	0	1	1
26	0	0	1	0	1
27	1	0	0	1	0
28	0	1	0	0	1
29	0	0	1	0	0
30	0	0	0	1	0
31	0	0	0	0	1
32	1	0	0	0	0
33	0	1	0	0	0

Appendix C

State Machine HDL

Example Code

In chapter 11 a discussion was included of state machine BISTs. A series of interrelated counters define the stimulus to the memory. Table 11-2 included some VHDL code for a three-bit ripple counter. The complete VHDL follows in figure C-1.



```
library ieee, work;
USE IEEE.Std_Logic_1164.all ;

entity threebit_e is
// Code by Thomas J Eckenrode
  port ( STclk       :in  std_ulogic;
         inc         :in  std_ulogic;
         countout    :out std_ulogic_vector(2 downto 0));
end entity threebit_e;
architecture threebit_a of threebit_e is
signal u_bit     : std_ulogic_vector(2 downto 0);
signal l_bit     : std_ulogic_vector(2 downto 0);

begin
   latchdef:process(STclk, u_bit)
    begin
     if STclk='1' AND STclk'EVENT then
         l_bit  <= u_bit;
     end if;
   end process latchdef;
   with inc select
         u_bit(0) <=  not l_bit(0) when '1',
                    l_bit(0) when others;
   with inc select
        u_bit(1) <= (l_bit(0) XOR l_bit(1)) when '1',
                  l_bit(1) when others;
   with inc select
        u_bit(2) <= ((l_bit(0) AND l_bit(1)) XOR l_bit(2)) when '1',
                  l_bit(2) when others;
   countout <= l_bit;

                              end architecture threebit_a;
```

Figure C-1. VHDL deck for a three-bit ripple counter.

A key portion of a memory BIST is the read/write controller. It generates the read-enable and write-enable signals. A segment of code was included in Table 11-4. The complete Verilog code for generating the read-enable, write-enable, and data signals for the first two elements of the March C- pattern are given in figure C-2.

```
module RWGEN( clock, start, max_addr, read, write, data );
// Code by Garret S. Koch
input  clock, start, max_addr;
output read, write, data;

reg  next_state0,
   next_state1,
   next_state2,
   next_state3;

reg  state0,
   state1,
   state2,
   state3;

initial
 begin
  state0 = 1 ;
  state1 = 0 ;
  state2 = 0 ;
  state3 = 0 ;
 end
```

```
    always @ (posedge clock)
     begin
      state0 = next_state0 ;
      state1 = next_state1 ;
      state2 = next_state2 ;
      state3 = next_state3 ;
     end

    always @ (start or state0 or state3 or max_addr)
        if      ( start    )         next_state0 = 0 ;
        else if ( max_addr & state3 ) next_state0 = 1 ;
        else                         next_state0 = state0;

    always @ (start or state1 or max_addr)
        if      ( start    )         next_state1 = 1 ;
        else if ( max_addr )         next_state1 = 0 ;
        else                         next_state1 = state1;

    always @ (state1 or state3 or max_addr)
        if      ( max_addr & state1 ) next_state2 = 1 ;
        else if (!max_addr & state3 ) next_state2 = 1 ;
        else                         next_state2 = 0 ;

    always @ (state2 or max_addr)
        if      (           state2 ) next_state3 = 1 ;
        else                         next_state3 = 0 ;

    assign write = state1  | state3;
    assign read  = state2;
    assign data  = !(state1 | state2);

endmodule
```

Figure C-2. Sample Verilog for read/write generator.

The BIST address counter should be able to increment or decrement addresses and perform these operations on either a ripple word or ripple bit basis. When decrementing, the maximum address must first be loaded into the counter. All of these features are included in the counter shown in Figure C-3 [238].

```
module address_counter (a, b, c, f, inc_dec, increment, word_limit,
   bit_limit, w_limit, b_limit, word_address, bit_address,
   next_word_r, next_bit_r, scan_in, scan_out,add_comp, word_match);

// Code by R. Dean Adams, Robert M. Mazzarese, Esq.

   input a, b, c, f, scan_in, inc_dec, add_comp, word_match, increment;
   input [7:0] word_limit, bit_limit, w_limit, b_limit;

   output [7:0] word_address, bit_address, next_word_r, next_bit_r;
   output scan_out ;

   reg [7:0] next_word_r, next_bit_r, word_address, bit_address;
   reg [7:0] tempword, tempbit;

   initial begin
       next_word_r = 8'b00000000; next_bit_r = 8'b00000000;
       word_address = 8'b00000000; bit_address = 8'b00000000;
   end

   //TRANSFER pipeline values to output

   always @ (posedge f)  begin
       #1;
       word_address <= next_word_r;
       bit_address <= next_bit_r;
   end

//CALCULATE new address when increment signal received
   always @ (posedge increment) begin #1;
       casez ({add_comp,inc_dec,word_match})
           3'b10z: begin
               next_word_r = 8'b00000000;
               next_bit_r = 8'b00000000; end
           3'b11z: begin
               next_word_r = w_limit;
               next_bit_r = b_limit; end
           3'b000: begin
               next_word_r = next_word_r+1; end
           3'b010: begin
               next_word_r = next_word_r - 1; end
```

```
            3'b001: begin
                next_bit_r = next_bit_r + 1;
                next_word_r = 8'b00000000; end
            3'b011: begin
                next_bit_r = next_bit_r - 1;
                next_word_r = w_limit; end
            default: begin
                $display("address counter default");
                next_word_r = 8'b00000000;
                next_bit_r = 8'b00000000; end
        endcase
    end

/* RELOAD COUNTER whenever inc_dec changes */
    always @(inc_dec) begin #1;
        case (inc_dec)
            1'b1: begin
                next_word_r = 0; next_bit_r = 0;
                next_bit_r <= bit_limit; next_word_r <= word_limit;
                end
            1'b0: begin
                next_word_r = 1; next_bit_r = 1;
                next_bit_r <= 8'b00000000; next_word_r <= 8'b00000000;
                end
        endcase
    end
endmodule
```

Figure C-3. Address counter example.

References

[1] G.E. Moore, “Cramming more components onto integrated circuits,” Electronics, Vol. 38 No. 8, 4/19/65.

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GLOSSARY / ACRONYMS

ABIST – Array built-in self-test. This term is synonymous with memory built-in self-test.
AF – Address decoder fault.
Aggressor – Cell which causes erroneous operation in a victim cell.
ATE – Automated test equipment.
ATPG – Automatic test pattern generation.

Beta ratio – Typically the ratio between the pull-down strength and transfer strength in an SRAM cell.
BIST – Built-in self-test
Bit oriented – A memory which is accessed one bit at a time.
Bridging defect – A short between to signal lines.

CAM – Content addressable memory
CF – Coupling fault.

DRAM – Dynamic random access memory.

EEPROM – Electrically erasable programmable read only memory.

FeRAM – Ferroelectric random access memory.
Flash – A type of EEPROM where large portions of memory can be erased simultaneously.

Galloping pattern – Pattern which ping-pong addresses through all possible address transitions.

LFSR – Linear feedback shift register. Used to generate pseudo-random patterns.

Marching pattern – Sequentially addresses memory, leaving new data type in its wake.
MISR – Multiple input signature register.
MRAM – Magnetoresistive random access memory.

NPSF – Neighborhood pattern sensitive fault.

PROM – Programmable read only memory.

ROM – Read only memory.

SOC – System on chip.
SOI – Silicon on insulator.
SRAM – Static random access memory.

Ternary CAM – CAM which stores "1", "0", or “don’t care” on a per bit basis.
TF – Transition fault.

Victim – Cell which is impacted by operation in aggressor cell.

Walking pattern – Sequentially addresses memory, leaving old data type in its wake.
Word oriented – A memory which is accessed one word at a time.

INDEX

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R. Dean Adams has over 20 years of experience in the design and development of embedded and stand-alone memories, high-performance custom logic, and DFT/BIST circuits for IBM. He is currently a member of IBM's Design-For-Test (DFT) department, where he consults on numerous memory and advanced microprocessor design projects. Dean is a leading expert in high-performance memory BIST, as well as the modeling and testing of standard and custom logic for leading edge semiconductor technologies.

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