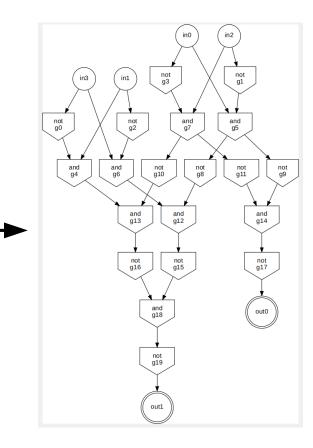
```
module abs_diff (pi0, pi1, pi2, pi3, po0,
po1);
 input pi0, pi1, pi2, pi3;
 output po0, po1;
 wire n5, n6, n7, n8, n9, n10, n11, n12;
 assign n5 = pi0 \& \sim pi2;
 assign n6 = \sim pi0 \& pi2;
 assign n7 = \sim n5 \& \sim n6;
 assign n8 = pi1 \& \sim pi3;
 assign n9 = \sim n6 \& n8;
 assign n10 = \sim pi1 \& pi3;
 assign n11 = \sim n5 \& n10;
 assign n12 = \sim n9 \& \sim n11;
 assign po0 = \sim n7;
 assign po1 = \simn12;
endmodule
```



Verilog to Verilog

Translator