6	6	6	0000 0 110
7	7	7	0000 0 111
8	10	8	0000 1000
9	11	9	0000 1001
10	12	A	0000 1010
11	13	B	0000 1011
12	14	C	0000 1100
13	15	D	0000 1101
14	16	E	0000 1110
15	17	F	0000 1111
16	20	10	0001 0000
17	21	11	0001 0001
18	22	12	0001 0010
19	23	13	0001 0011
20	24	14	0001 0100

- In above table the binary bits are divided in groups to indicate binary equivalent of Octal and binary equivalent of Hexadecimal.

Where bits are combined in group of three, it shows binary equivalent of octal number in that Row.

Where bits are combined in group of Four, it shows binary equivalent of Hexadecimal number in that Row.

Convert : $(29)_{10}$ to ($)_2$ ($)_8$ ($)_{16}$

2 | 29 → 1
2 | 14 → 0
2 | 7 → 1
2 | 3 → 1
1 → 1

$(11101)_2$

011101
3 5

$(35)_8$

0001 1101
1 13

$(1D)_{16}$

Convert : $(101101)_2$ to $(\ )_{10}$ $(\ )_8$ $(\ )_{16}$

101101

$5 \quad 5$

$(55)_8$

00101101

$2 \quad 13$

$(2D)_{16}$

$(101101)_2$

$\rightarrow 1\times2^0 + 0\times2^1 + 1\times2^2 + 1\times2^3 + 0\times2^4 + 1\times2^5$

$= 32+8+4+1$

$= (45)_{10}$

Convert : $(1011011101)_2$ to $(\ )_8$ $(\ )_{16}$

$001\ 011\ 011\ 101$

$1 \quad 3 \quad 3 \quad 5$

$(1335)_8$

$0010\ 1101\ 1101$

$2 \quad 13 \quad 13$

$(2DD)_{16}$

CONCLUSION :-

Be learn an understand how to convert 1 type of numbering system to another type of numbering system.

$=(2^6 - 2^0)_{10} - (101100)_2$

$=(2^6 - 1)_{10} - (101100)_2$

$=(111111)_2 - (1001100)_2$

Steps of conversion method is,

GIVEN NUMBER =

1	1	1	1	1	1
-1	0	1	1	0	0
0	1	0	0	1	1

RESULT = $(010011)_2$

Q.1 Find 9's complement of $(456)_{10}$

9	9	9
-4	-5	-6
5	4	3

(543) 9's complement.

Q.2 Find 9's complement of $(456)_{10}$

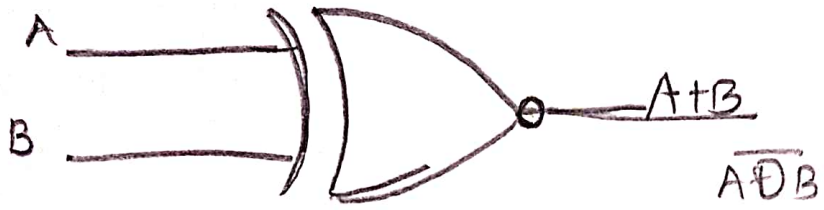
9	9	9
-4	-5	-6
5	4	3

CONCLUSION :-

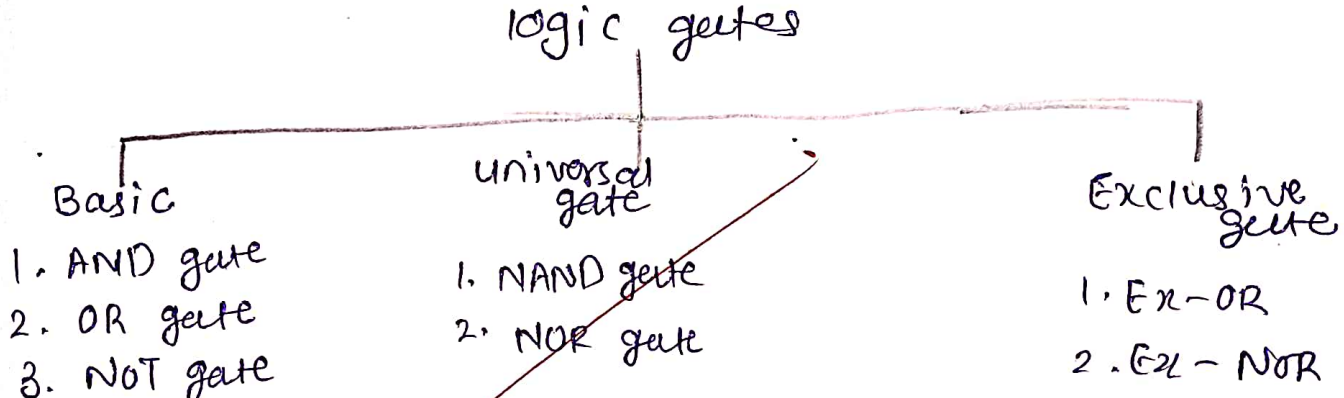
PROCEDURE : -

1. Connect the circuit diagram for one gate.
2. Give the input as shown in observation table and see the output on the related pin nos.
3. Tabulate the outputs.
4. Then connect the other ICs one by one and verify the outputs of that ICs.

Q.1 Draw the symbol of Ex- OR Gate ?



Q.2 List different types of logic Gates ?



Q.3 Write truthtable and Boolean Expression for EX-NOR Gate.

A	B	$Y = \overline{A}B + A\overline{B}$
0	0	1
0	1	0
1	0	0
1	1	1

Q.4 Write truth table and Boolean Expression for NAND Gate.

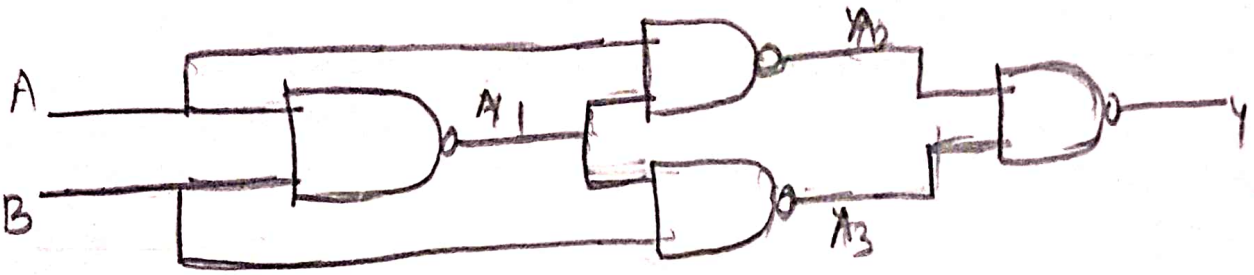
A	B	$y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

CONCLUSION :-

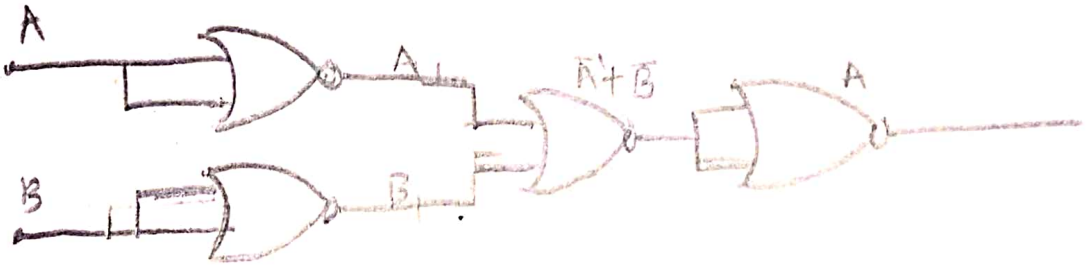
Q.1 Define Universal Gate ?

→ A gate which can implement any boolean function without need to use any other gate type.

Q.2 Draw EX-OR Gate from NAND Gate write true



Q.3 Draw NOR Gate from NAND Gate write true



Q.4 Draw AND Gate from NAND Gate and write its true table.

CONCLUSION : -

OBSERVATION TABLE: -

NOR gate as Universal

1) NOR as NOT

A	B	$\overline{A}$
0	0	1
0	1	0
1	0	0
1	1	0

2) NOR as OR

A	B	$A+B$
0	0	1
0	1	1
1	0	1
1	1	0

3) NOR as AND

A	B	$A.B$
0	0	1
0	1	0
1	0	0
1	1	0

4) NOR as NAND

A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

Q2 Truth table.

A	B	$Y = \overline{\bar{A}B + A\bar{B}}$
0	0	0
0	1	1
1	0	1
1	1	0

Q3 Truth table.

A	B	$Y = (A+B)'$
0	0	1
0	1	0
1	0	0
1	1	0

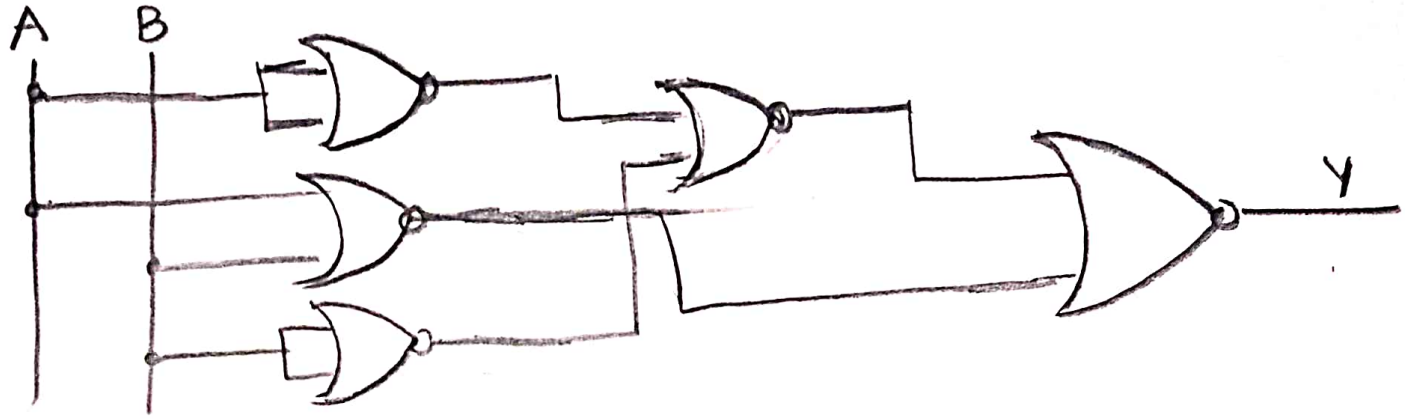
Q4

Questions:

Q.1 What are the applications of logic gates ?

→ 1. Computers , 2. Digital electronics , 3. Telecommunication
4. Robotics , 5. control system , 6. instrumentation .
7. medical devices , 8. transportation systems
9. security system , & and many more.

Q.2 Draw EX-OR Gate from NOR Gate write true table.

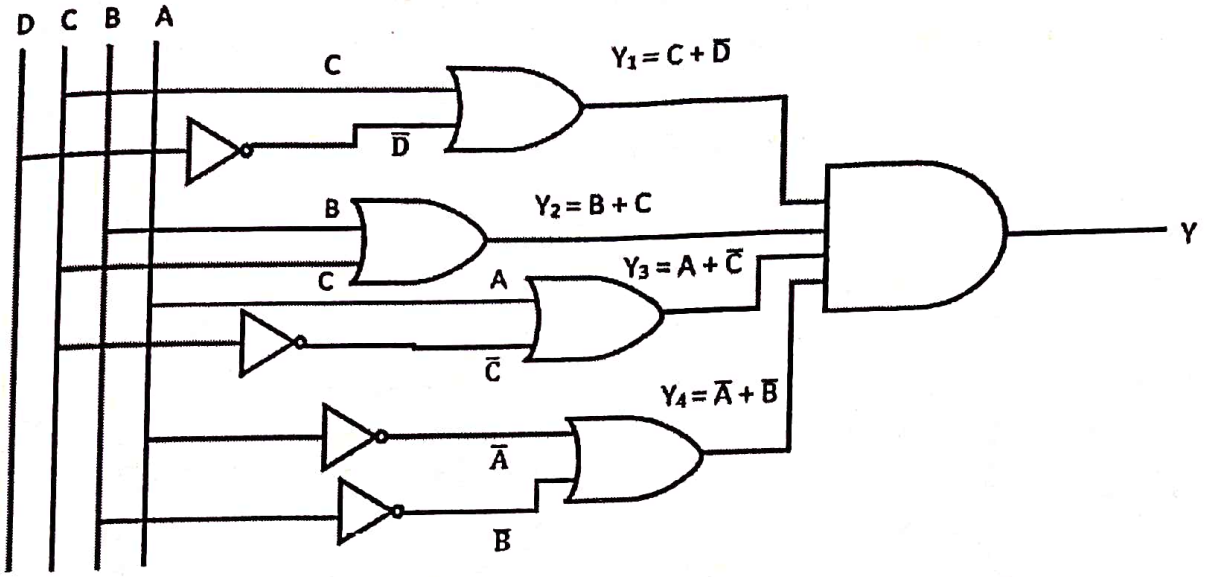


Q.3 Draw OR Gate from NOR Gate and write true table.

Q.4 Draw NAND Gate from NOR Gate and write true table.

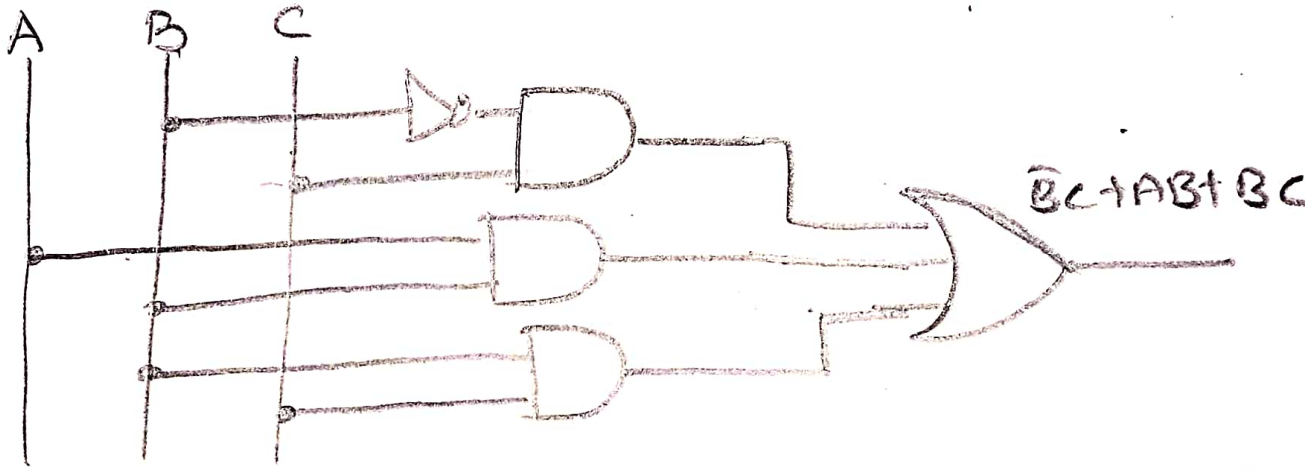
CONCLUSION: -

$Y = (C + \overline{D}) \cdot (B + C) \cdot (A + \overline{C}) \cdot (\overline{A} + \overline{B})$



Q.1 Simplify and draw logic circuit using basic gates for the following equation:

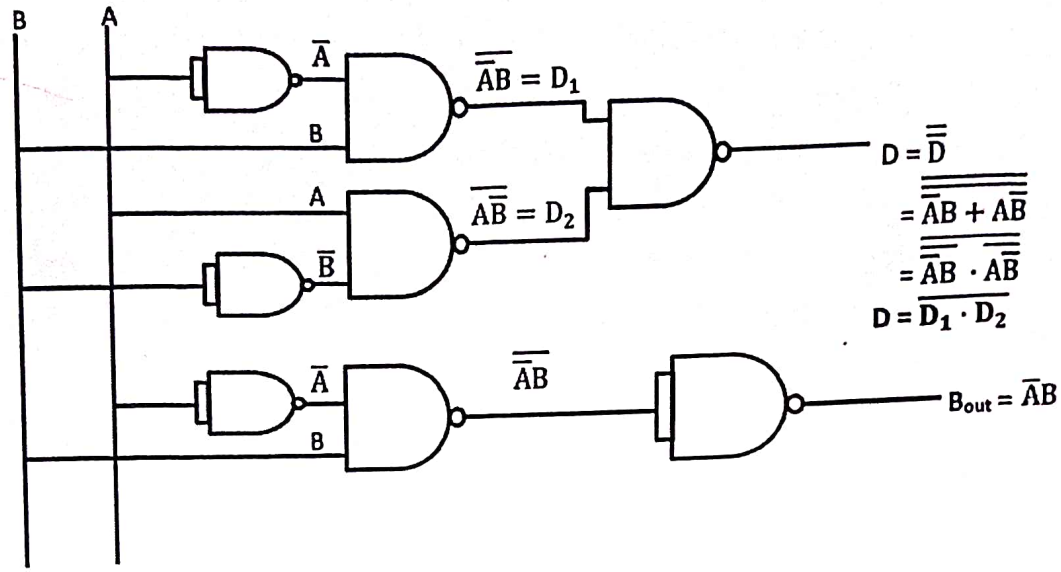
$\overline{B}C + AB + BC$



CONCLUSION :-

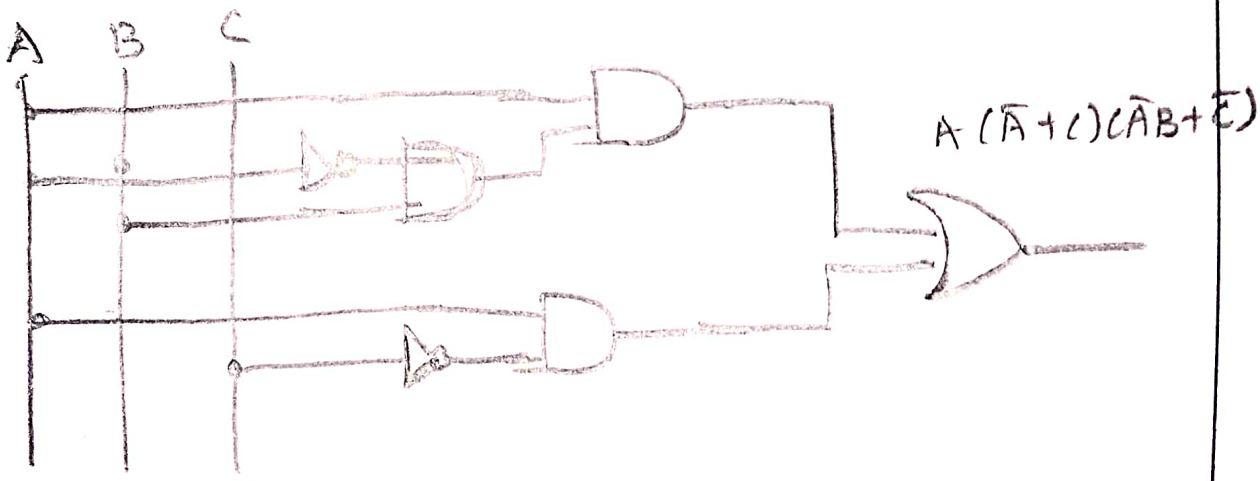
PRACTICAl : 7

AIM : Simplify and design Boolean expression using universal logic gates.



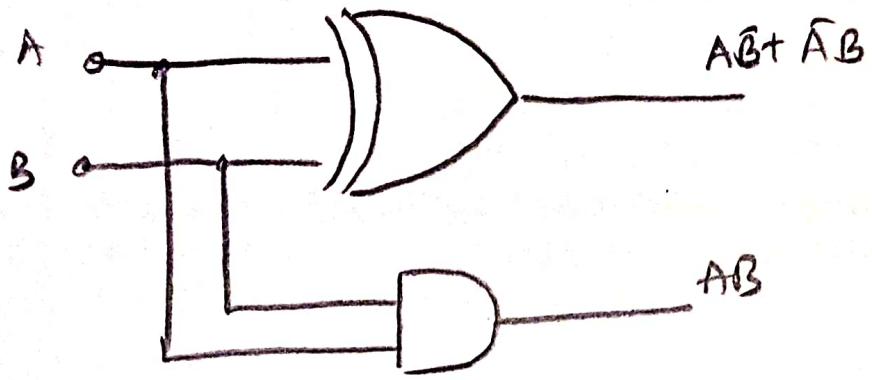
Q.1 Simplify and design Boolean expression using universal logic gates for the given equation:

$A(\overline{A} + C)(\overline{A}B + \overline{C})$

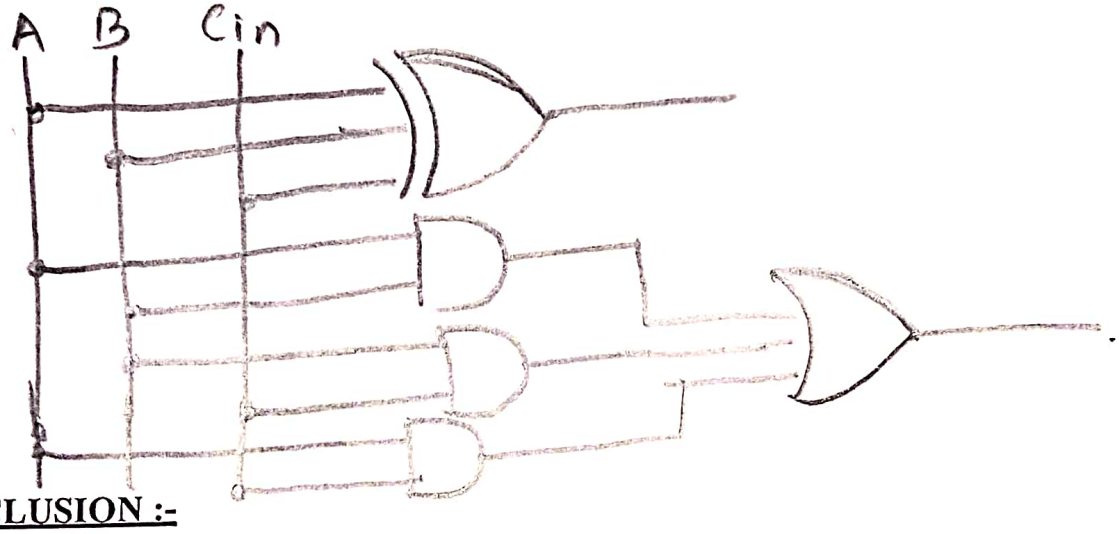


Q.1 Design Half Adder And Full Adder Circuit Using Basic Gates

→ Half adder :-

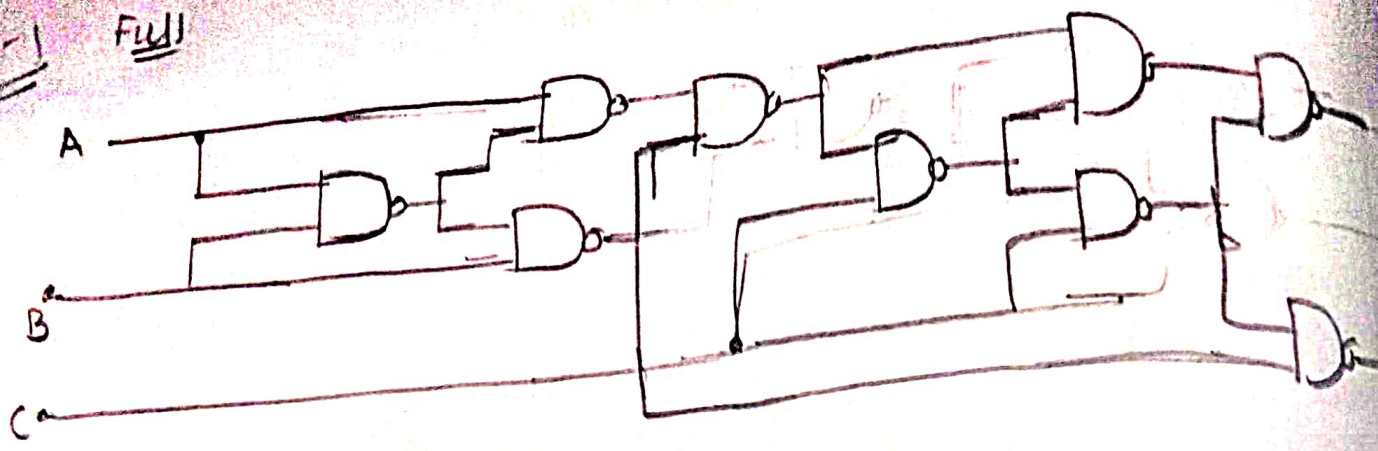


→ full adder :-

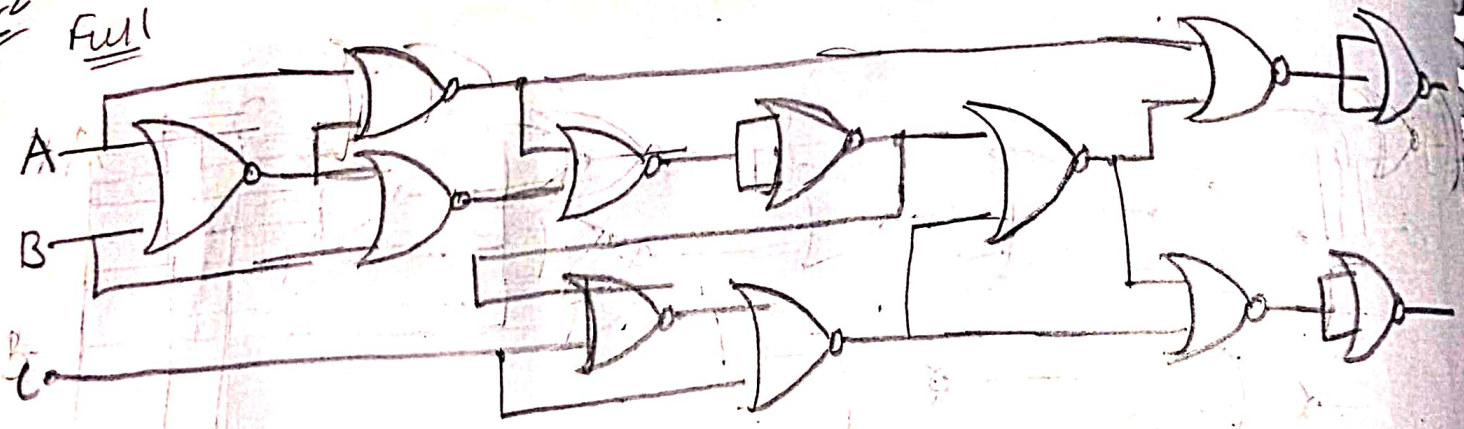


CONCLUSION :-

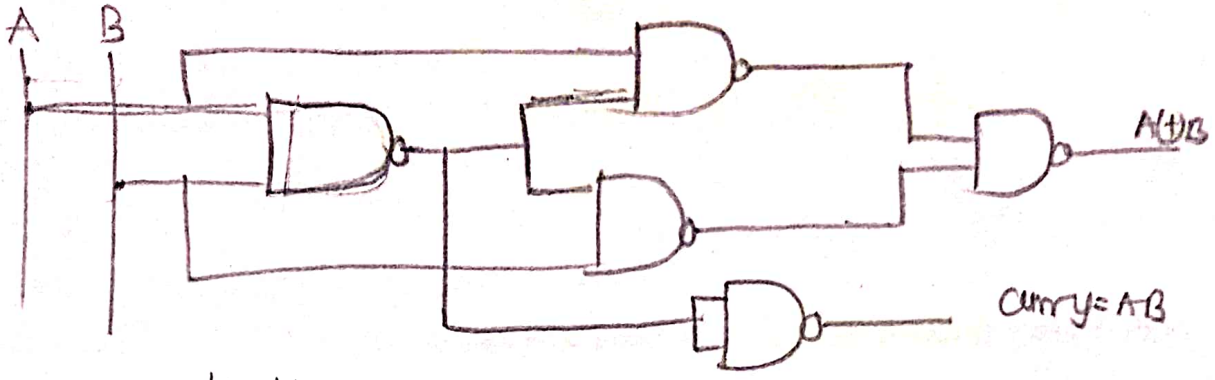
2-1 Full



2-2 Full



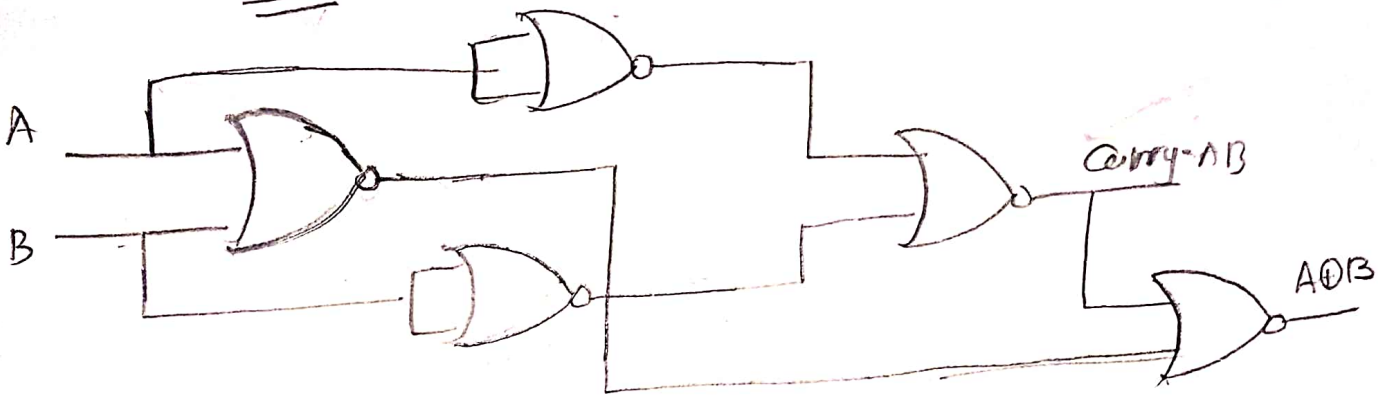
Q.1 Draw half substractor and full substractor using nand gates



Half

Q.2 Draw half substractor and full substractor using Nor gates

Half

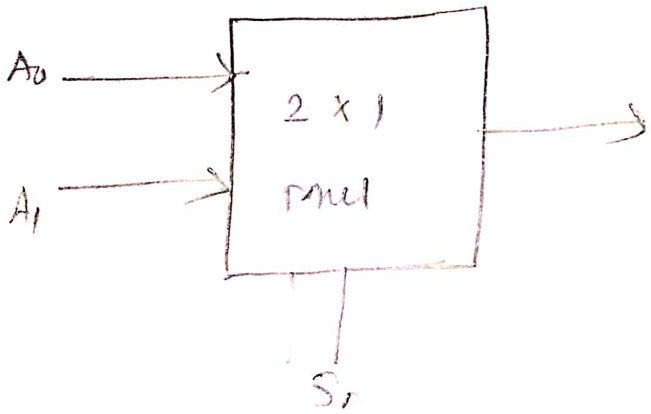


CONCLUSION :-

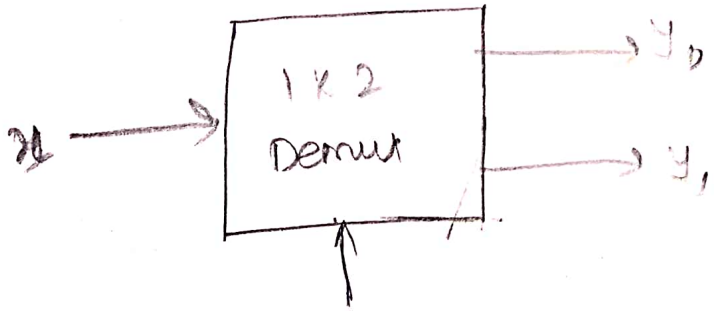
1 × 4 Demultiplexer :

1. Connections are made as per the Fig. 2.
2. By varying the select inputs S_1 & S_0, the information on the single input E istransmitted to any one of 4 output lines and the truth table is verified.

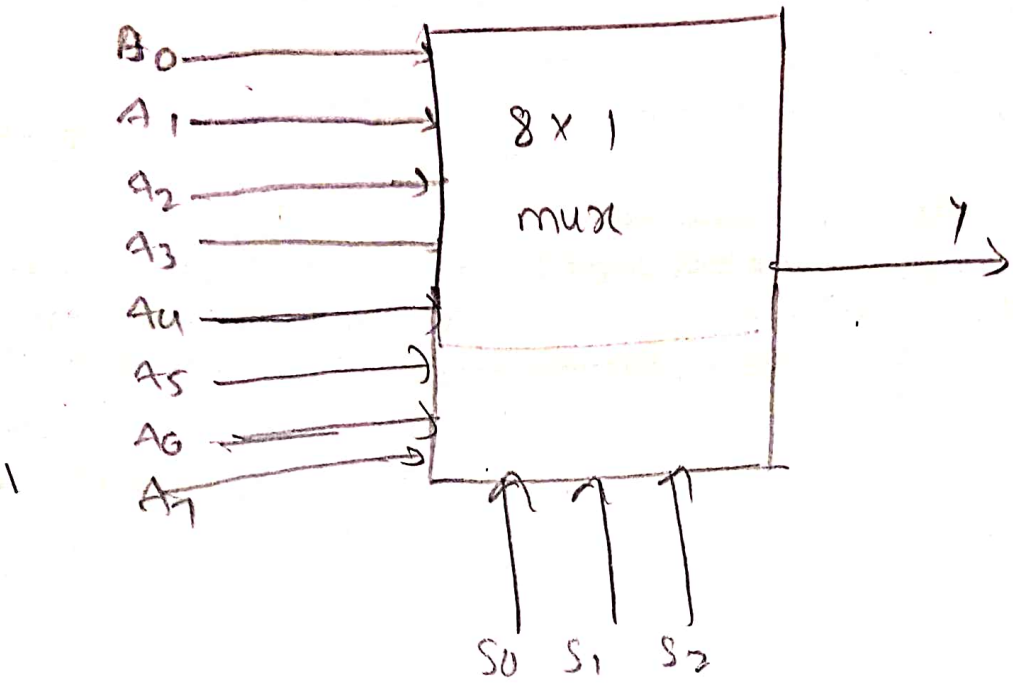
Q.1 Design 2 x 1 MUX.



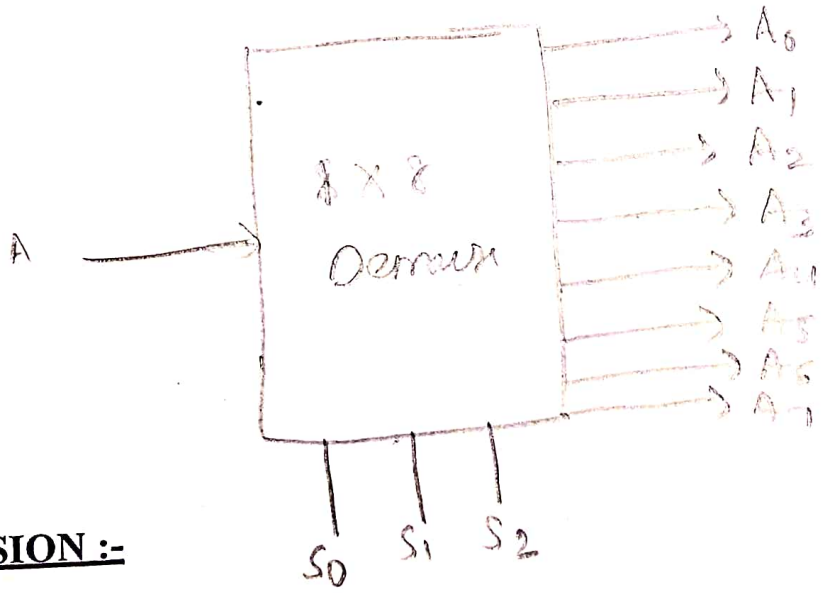
Q.2 Design 1 x 2 DEMUX.



Q.3 Design 8 x1 MUX.

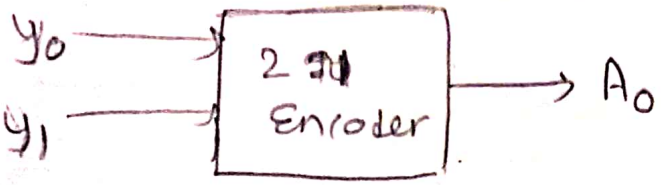


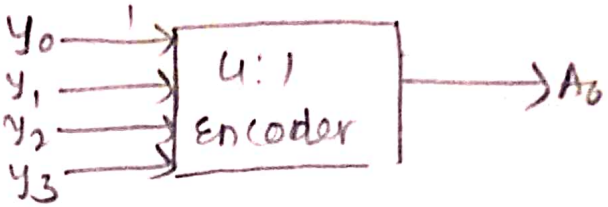
Q.4 Design 1 x8 DEMUX.



CONCLUSION :-

Q.1 Draw 2:1 , 4:1 encoder





CONCLUSION :-

PROCEDURE :-

1.Connect the circuit as shown in figure.

2.Apply Vcc & ground signal to every IC.

3.Observe the input & output according to the truth table.

QUESTIONS AND ANSWERS :

Q-1 What is Flip Flop?

→ Flip Flop is also a basic building block of Synchronous sequential circuits. It has two stable states : It can stroe one bit of information.

Q-2 What is limitation of RS Flip-Flop ?

→ The limitation ~~with of~~ S-R Filp-Flop :

- It is a bistable circuit, which means that it can only be in one of two states, either '0' or '1'
- It is not a synchoronous circuit, which means that does't have a clock signal to control its opreation.