Intro to Computer Architecture

Quiz-1

This is a closed book test. No "book" materials are permitted during the test.
Ask me if you have any questions.
Show all steps of your solutions for full/partial credits.

Try to have one empty seat between two students.

No connected devices such as cellphone during this test.

Intro to Computer Architecture

Regarding Quiz-1

- **30 points, 30 minutes; class after quiz**
- **Includes Lectures 2-7**
  - ➢ Important Topics from lectures
    - ✓ Major steps to execute an instruction
  - ➢ Important Topics from Introduction to Computers (Ch. 1 from zyBooks)
    - ✓ Ch. 1 >> 1.1-1.9
- **Questions: Short questions (HW), Math-related, True/False, …**
- **Any not-allowed activities → Zero, etc. (applies to all tests)**

If you do not return your papers right after the STOP time,
I will not accept/grade your papers.

Intro to Computer Architecture

Quiz-1

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Ask me if you have any questions.
Show all steps of your solutions for full/partial credits.

Try to have one empty seat between two students.

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Corrections: ?

STOP writing @ 10:10

We will have lecture after quiz.

Intro to Computer Architecture

Lecture 8 Presented by Md "Raihan" Uddin

Reading: See Reading Assignments on Blackboard

Tests: Quiz-1 (Week 4), Exam-1 (Week 5), HW-3 (Week 7), HW-4 (Week 8), …

- **Computer Milestones;**
- **Intro to Structured Computer Organization (Handout 2b)**
  - 1.2: Milestones in Computer Architecture
  - 1.3: The Computer Zoo
  - **1.4: Example Computer Families**

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Intro to Computer Architecture

Computer Generations

- **Zeroth Generation**
  Mechanical Computers (1642 – 1945)
- **First Generation**
  Vacuum Tubes (1945 – 1955)
- **Second Generation**
  Transistors (1955 – 1965)
- **Third Generation**
  Integrated Circuits (1965 – 1980)
- **Fourth Generation**
  Very Large-Scale Integration (1980 – ?)
- **More Generations?**
  (we'll see)

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Computer Generations (+)

- **Zeroth Generation: Mechanical Computers (1642 – 1945)**
  - **First calculating machine by Pascal (1623-1662) in 1642**
  - **Babbage (1792-1871), "different engine", speedometer**
  - **"Analytical engine" – storage (memory) 1000 words of 50 decimal digits, mill (computation unit – add, subtract, multiply, divide), input section (punched card reader), and output section (punched and printed output)**

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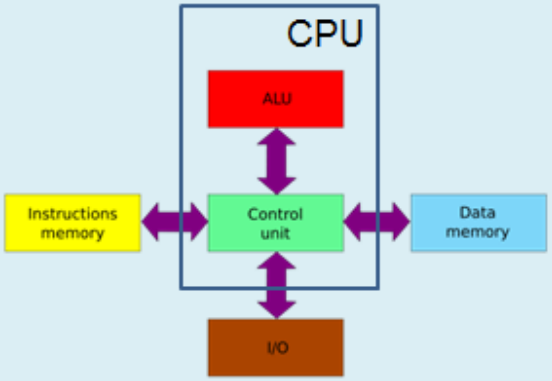
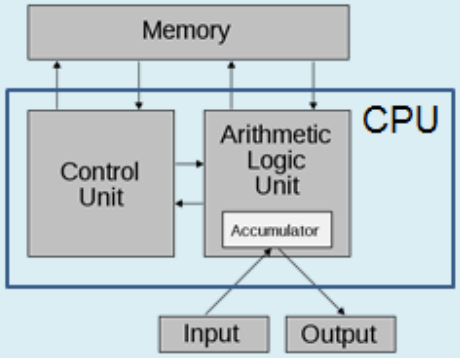
Computer Generations (+)

- **First Generation: Vacuum Tubes (1945 – 1955)**
  - **Enigma (Thomas Jefferson, former U.S. president)**
  - **Vacuum tubes – ENIAC (electronic numerical integrator and computer), 18,000 VTs and 1,500 relays, 30 tons, 140 KW power**
  - **The original von Neumann machine – CPU, memory (unified), I/O**
  - **The Harvard machine – CPU, memory (split into Instruction and Data), I/O**





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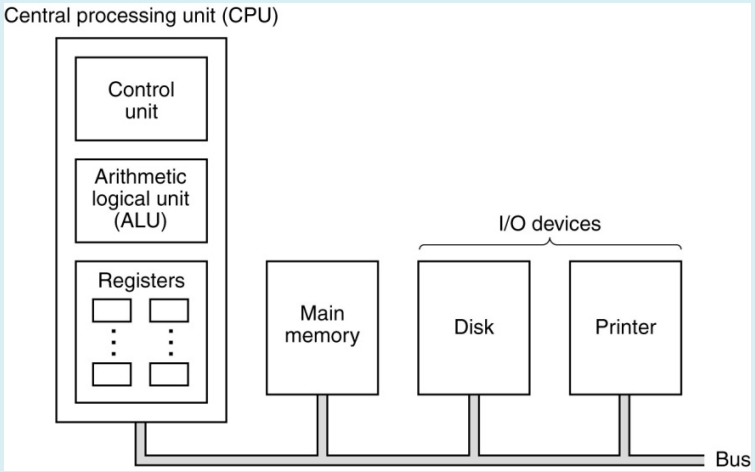
Computer Generations (+)

- **Second Generation: Transistors (1955 – 1965)**
  - **Transistor – tiny electronic switch**
  - **Size, power, cost**
  - **Programmed Data Processor (PDP)**
  - **MIT, TX-0**
  - **IBM 7094**
  - **PDP-1, MIT**
  - **Concept of supercomputers (Cray)**



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Computer Generations (+)

- **Third Generation: Integrated Circuits (1965 – 1980)**
  - **Integrated circuit (IC) – dozens of transistors in a chip**
  - **IBM System/360, multiprogramming**

Intro to Computer Architecture

Computer Generations (+)

- **Fourth Generation: Very Large-Scale Integration (1980 – ?)**
  - **VLSI – millions of transistors in a chip**
  - **IBM Personal Computer (PC), Intel CPU**
  - **Graphical User Interface (GUI)**
  - **FPGA (field programmable gate array)**

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Computer Generations

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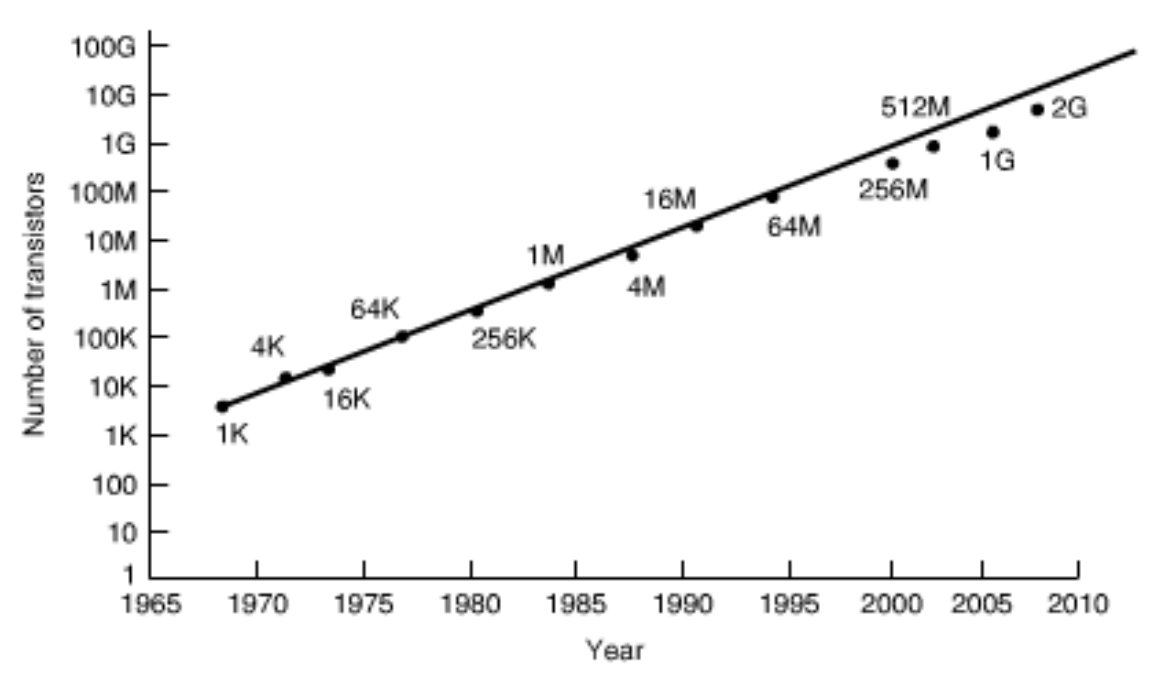
  Very Large-Scale Integration (1980 – ?)
- **More Generations?**

Intro to Computer Architecture

Moore's law and processor design

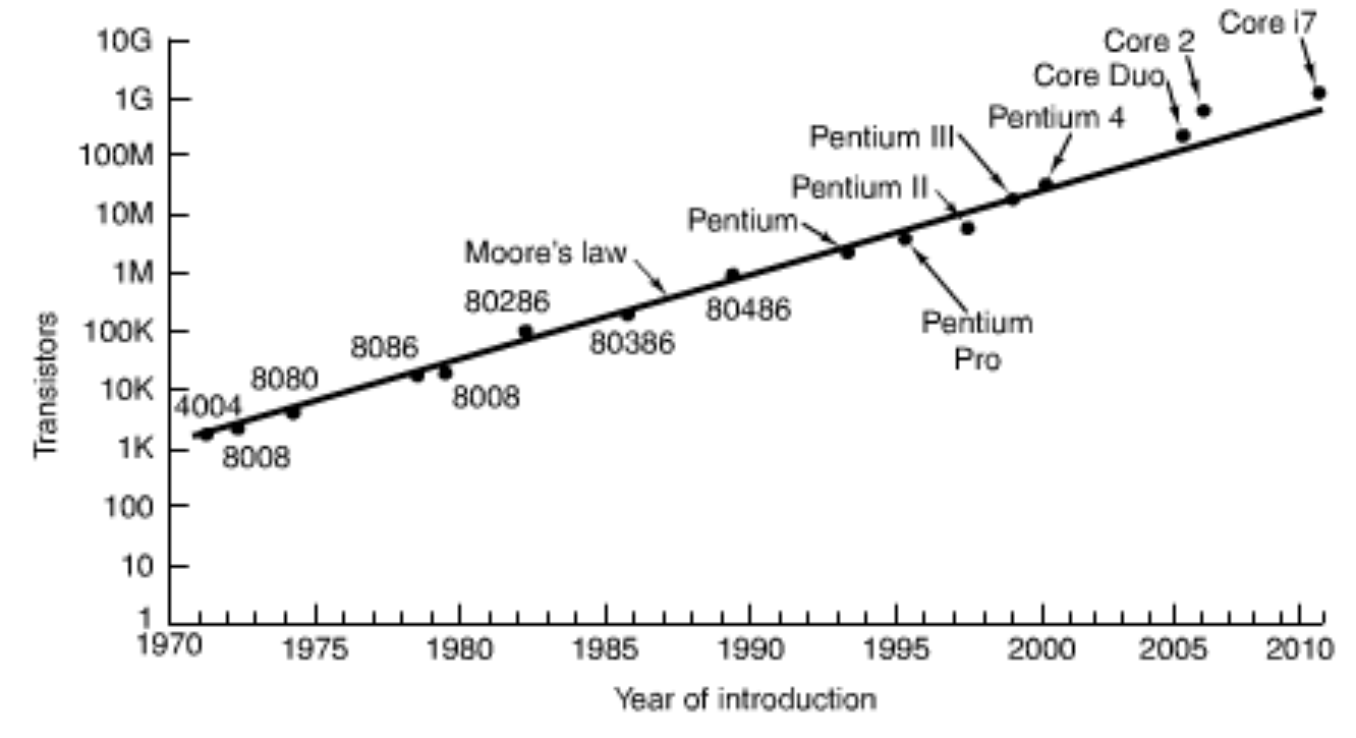
- Gordon Earle Moore: Co-founder and Chairman Emeritus of Intel Corp.
- **Moore's Law** predicts a 60-percent annual increase in the number of transistors that can be put on a chip. *(transistors doubles every two years)*



Intro to Computer Architecture

Moore's law and processor design (+)

- **Moore's Law** predicts a 60-percent annual increase in the number of transistors that can be put on a chip. Different chips/processors.



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Computer Generations (cont'd, +)

- **Zeroth Generation**
  Mechanical Computers (1642 – 1945)
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  Integrated Circuits (1965 – 1980)
- **Fourth Generation**
  Very Large-Scale Integration (1980 – ?)
- **Fifth Generation**
  (a) Low-Power and Invisible Computers (1980 – ?)
  (b) Multicore Computers (2000 – ?)

Intro to Computer Architecture

Computer Generations (+)

- **Fifth Generation: Low-Power and Invisible Computers (1980 – ?)**
  - **Embedded systems**
  - **Internet of Things (IoT), Artificial Intelligence,**
  - **GridPad (first Tablet from Grid Systems, 1989)**
  - **PDA (personal digital assistant), Smartphone (Simon)**
  - ~~Ubiquitous/pervasive/everyware computing is a post-desktop model of human-computer interaction in which information processing has been thoroughly integrated into everyday objects and activities. Example: refrigerators "aware" of their suitably tagged contents, able to both plan a variety of menus from the food actually on hand, and warn users of stale or spoiled food.~~

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Computer Generations (+)

- **Fifth Generation: Multicore Computers (2000 – ?)**
  - **VLSI – millions of transistors in a chip**
  - **2001, POWER4, first dual-core chip microprocessor, IBM**
  - **Advanced VLSI – billions of transistors in a chip (2008+)**
  - **System-on-a-chip (SoC)**
  - **Network-on-a-chip (NoC)**
  - **Multicore/many-core systems**

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The Computer Zoo

The Types/Classes of Computers

- **Current spectrum (i.e., categorization) of computers**

Type	Price ($)	Example application
Disposable computer	0.5	Greeting cards
Microcontroller	5	Watches, cars, appliances
Game computer	50	Home video games
Personal computer	500	Desktop or notebook computer
Server	5K	Network server
Collection of Workstations	50–500K	Departmental minisupercomputer
Mainframe	5M	Batch data processing in a bank

- **How about Supercomputers?**

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Do you have any questions?

12:33 PM

Intro to Computer Architecture

Lecture 8 Presented by Md "Raihan" Uddin

Reading: See Reading Assignments on Blackboard

Tests: Quiz-1 (Week 4), Exam-1 (Week 5), HW-3 (Week 7), HW-4 (Week 8), …

- Computer Milestones;
- Intro to Structured Computer Organization (Handout 2b)
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  - 1.3: The Computer Zoo
  - 1.4: Example Computer Families

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Example Computer Families

Tanenbaum and Austin book Ed. 5 (2005)

- (Intel) Pentium 4: (PC, Laptop)
- (Sun Microsystems) SPARC (Scalable Processor ARChitecture): Workstation, Server
- (Intel) Embedded CPU 8051: (Embedded systems)

Tanenbaum and Austin book Ed. 6 (2012)

- (Intel) x86 (PC, Server, HPC)
- (ARM) ARM (Mobile, Tablet, Smartphone)
- (AVR) AVR (Embedded systems)

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Example Computer Families (+)

Tanenbaum and Austin book Ed. 6 (2012)

- x86 (PC, Server, more)
  - ➢ PC, Server, more
- ARM (Mobile, Tablet, Smartphone)
  - ➢ Mobile, Tablet, Smartphone
- AVR (embedded systems, microcontroller)
  - ➢ Embedded systems, Microcontroller, Low-Power and Invisible Computers

Intro to Computer Architecture

Before x86 Architecture

- 1968, Intel Corporation
- 1969, Busicom to Intel, 12 custom chips for calculator
- 1970, first single-chip CPU 4004, 2300 transistors

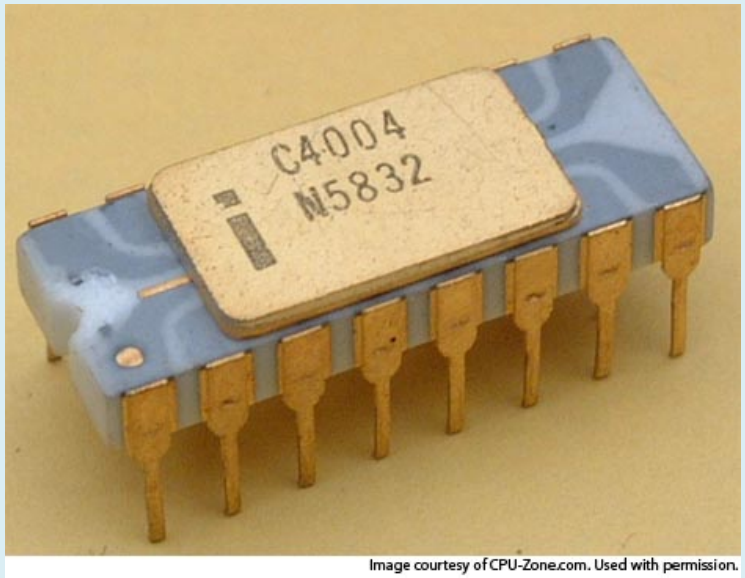

Image courtesy of CPU-Zone.com. Used with permission.

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x86 Architecture (+)

Key members

Chip	Date	MHz	Trans.	Memory	Notes
4004	4/1971	0.108	2300	640	First microprocessor on a chip
8008	4/1972	0.108	3500	16 KB	First 8-bit microprocessor
8080	4/1974	2	6000	64 KB	First general-purpose CPU on a chip
8086	6/1978	5–10	29,000	1 MB	First 16-bit CPU on a chip
8088	6/1979	5–8	29,000	1 MB	Used in IBM PC
80286	2/1982	8–12	134,000	16 MB	Memory protection present
80386	10/1985	16–33	275,000	4 GB	First 32-bit CPU
80486	4/1989	25–100	1.2M	4 GB	Built-in 8-KB cache memory
Pentium	3/1993	60–233	3.1M	4 GB	Two pipelines; later models had MMX
Pentium Pro	3/1995	150–200	5.5M	4 GB	Two levels of cache built in
Pentium II	5/1997	233–450	7.5M	4 GB	Pentium Pro plus MMX instructions
Pentium III	2/1999	650–1400	9.5M	4 GB	SSE Instructions for 3D graphics
Pentium 4	11/2000	1300–3800	42M	4 GB	Hyperthreading; more SSE instructions
Core Duo	1/2006	1600–3200	152M	2 GB	Dual cores on a single die
Core	7/2006	1200–3200	410M	64 GB	64-bit quad core architecture
Core i7	1/2011	1100–3300	1160M	24 GB	Integrated graphics processor

- MMX (MultiMedia
- SSE (Streaming SIMD Extensions)

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x86 Architecture (+)

- 1978, a genuine 16-bit CPU on a chip, 8086
- After 8086 → 8088, 80286, 80386, 80486
- After 80486, numbers cannot be trademarked, Pentium
- Intel chips are backward compatible as far back as 8086
- PC, Server, more

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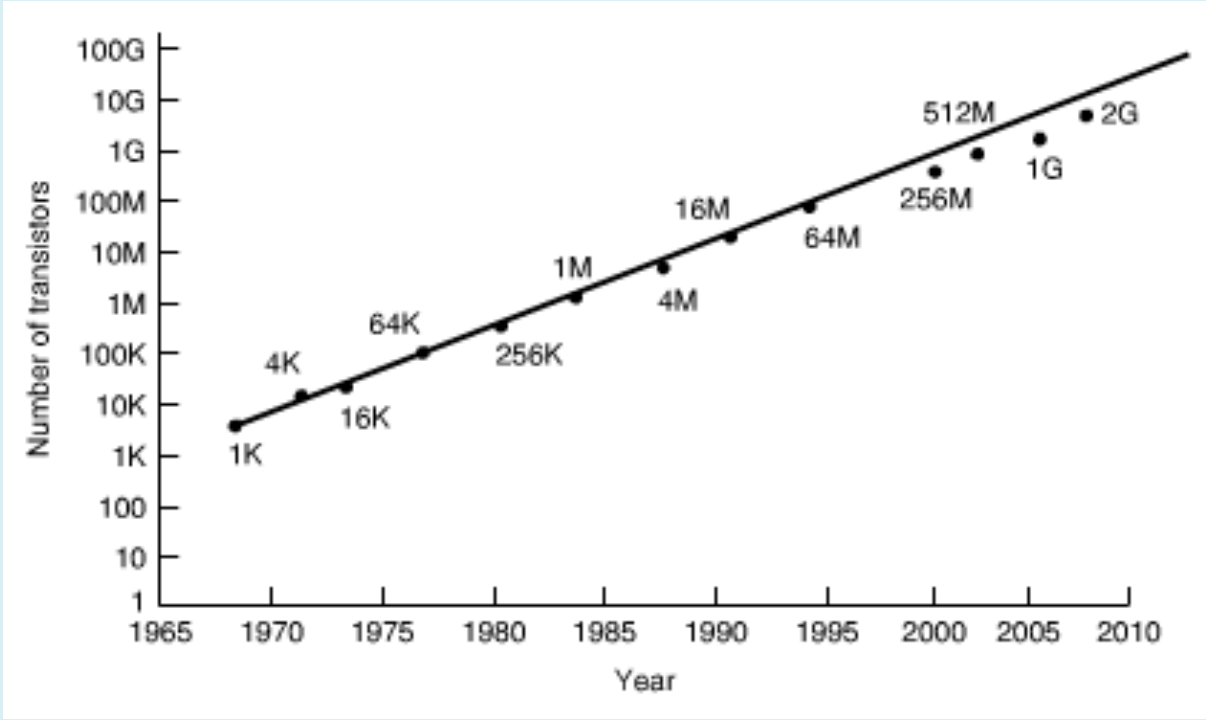
Moore's law and processor design

Textbook Ed. 6

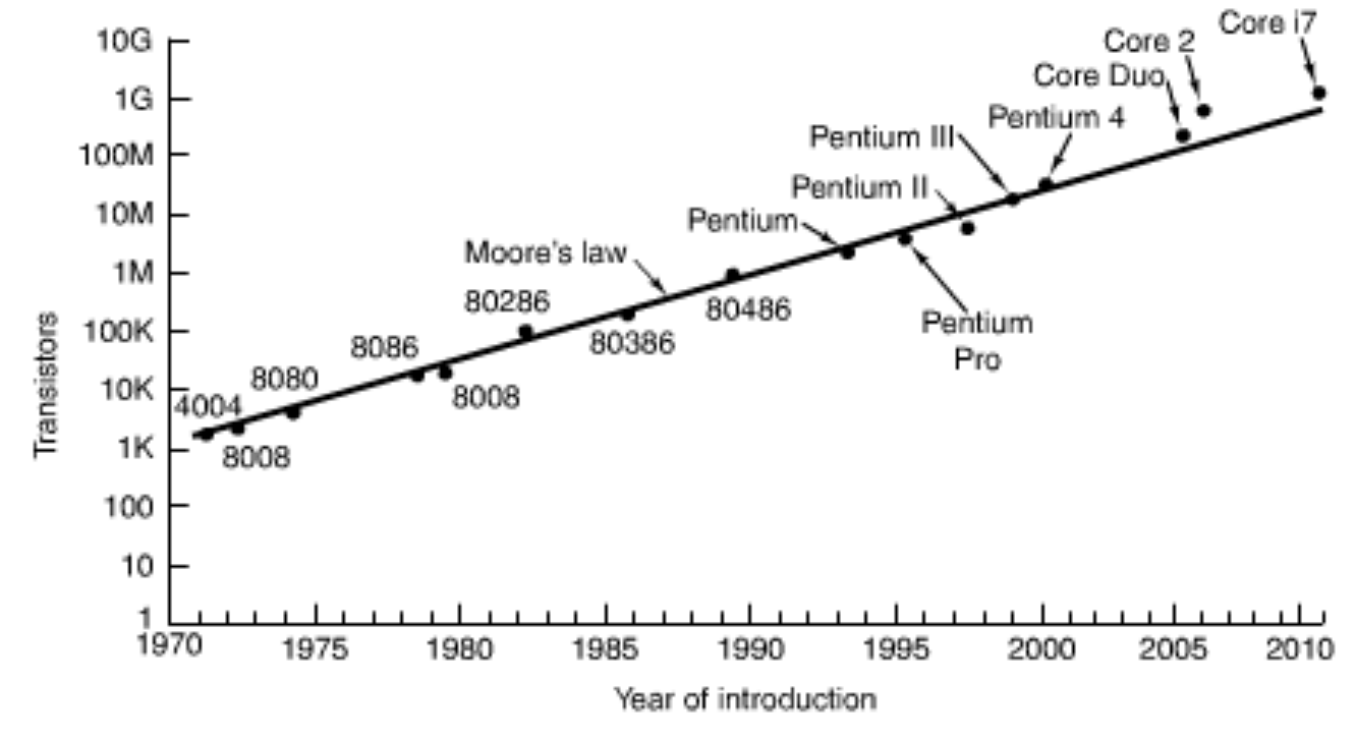
- **Moore's Law** predicts a 60-percent annual increase in the number of transistors that can be put on a chip.



Intro to Computer Architecture

Moore's law and Intel CPU chips

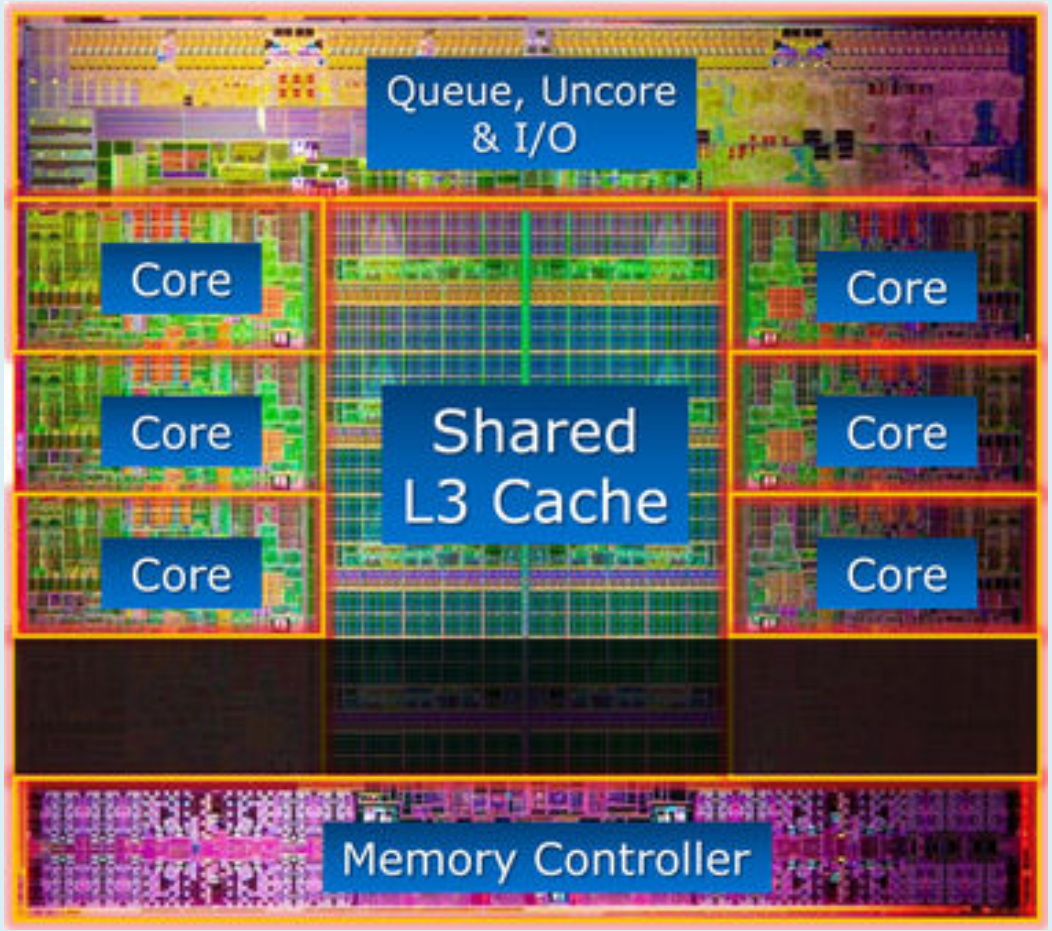
- **Moore's Law** predicts a 60-percent annual increase in the number of transistors that can be put on a chip. Different chips.



Intro to Computer Architecture

Intel Core i7-3960x die (21x21 mm, 2.27 BT)

- Cache?



Intro to Computer Architecture

Computer System

(Remember the diagram on left?)

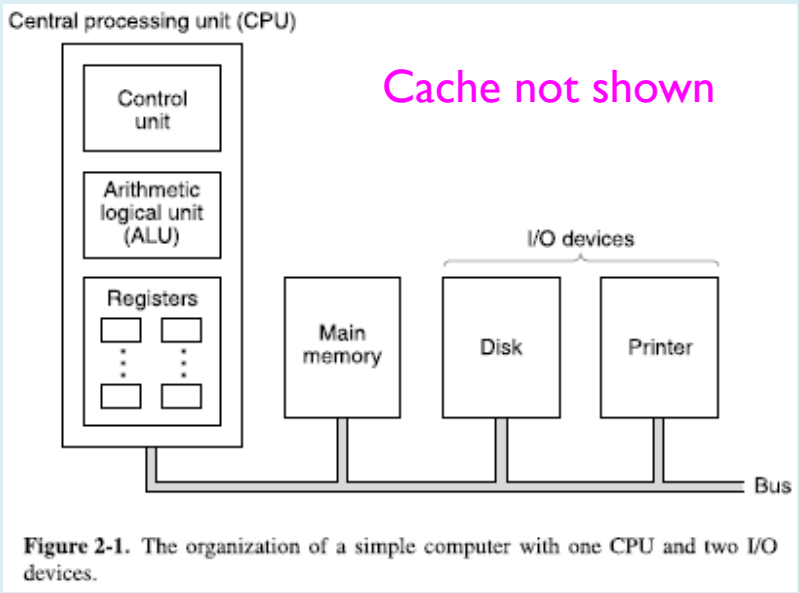


Figure 2-1. The organization of a simple computer with one CPU and two I/O devices.

Cache

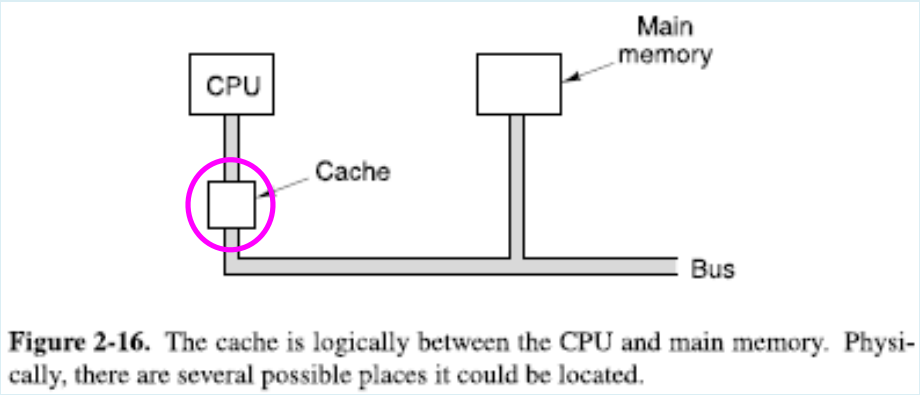
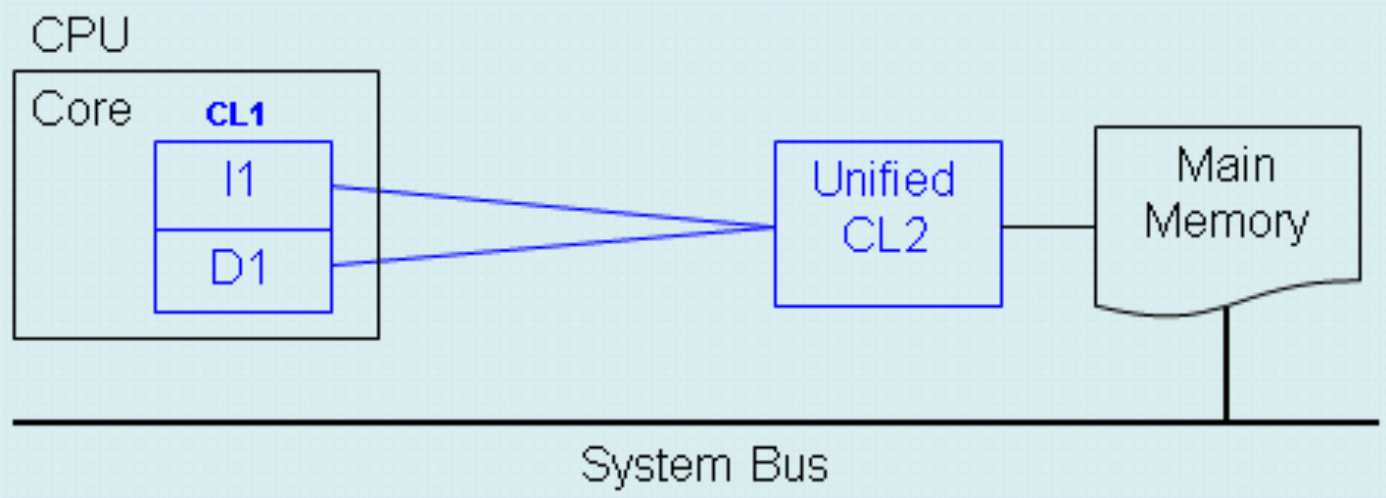


Figure 2-16. The cache is logically between the CPU and main memory. Physically, there are several possible places it could be located.

Intro to Computer Architecture

Computer System with Cache

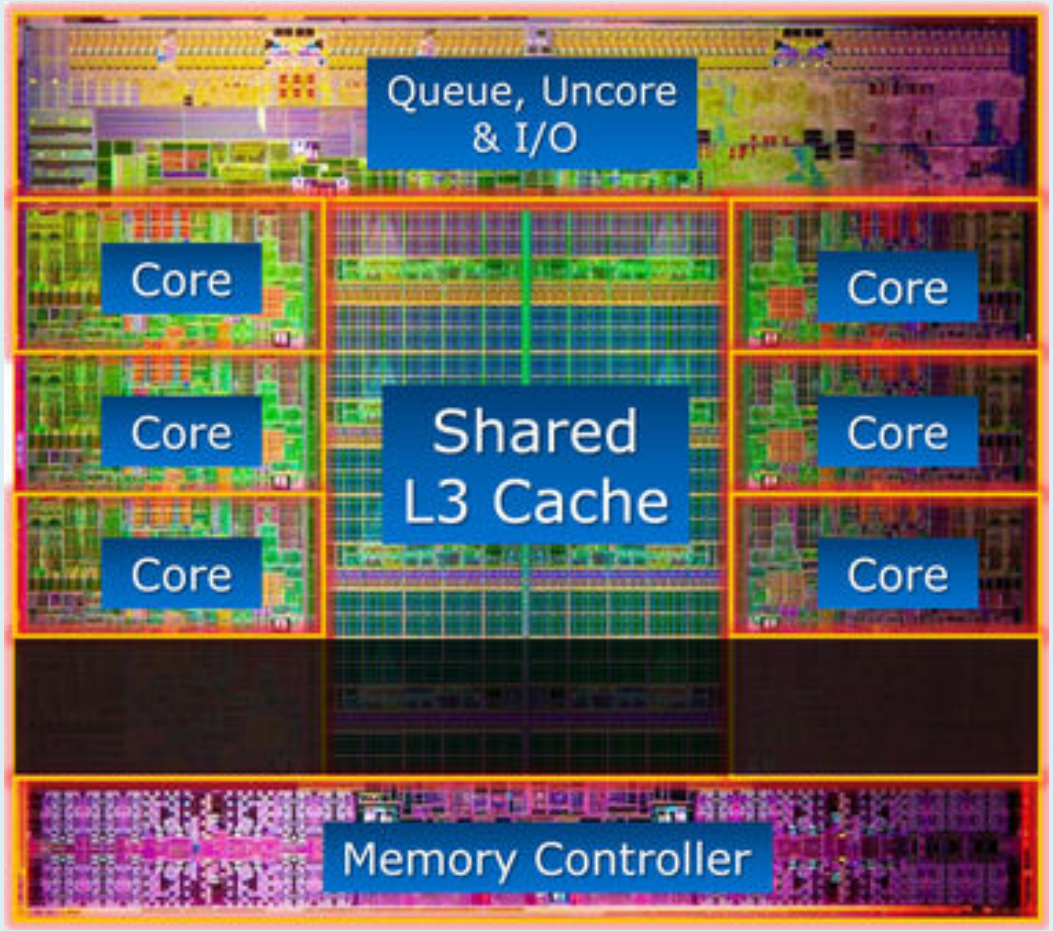
- **CL1 – Level-1 Cache or First Level Cache**
  - ➢ **Private, split into instruction cache (I1) and data cache (D1)**
- **CL2 – Level-2 Cache or Second Level Cache**
  - ➢ **Shared, unified (instructions and data)**
- **CL3 – Level-3 Cache or Third Level Cache (not shown)**



Intro to Computer Architecture

Intel Core i7-3960x die (21x21 mm, 2.27 BT) (+)

- 8/6 cores
- Private CL1, CL2
- Shared CL3



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ARM Architecture

- ISA Level (remember?)
  - ➢ Complex Instruction Set Computer (CISC), Intel
  - ➢ Reduced Instruction Set Computer (RISC), Berkeley, SPARC
- 1980s, Acorn Computer (UK), 8-bit CPU 6502, BBC Micro PC
- Acorn RISC Machine (ARM) processor, 6502, RISC, ARM2
- Apple, 1990s, ARM processor
- Advanced RISC Machine (ARM) processor, ARM 610, ARM7
- ARM (Mobile, Tablet, Smartphone)

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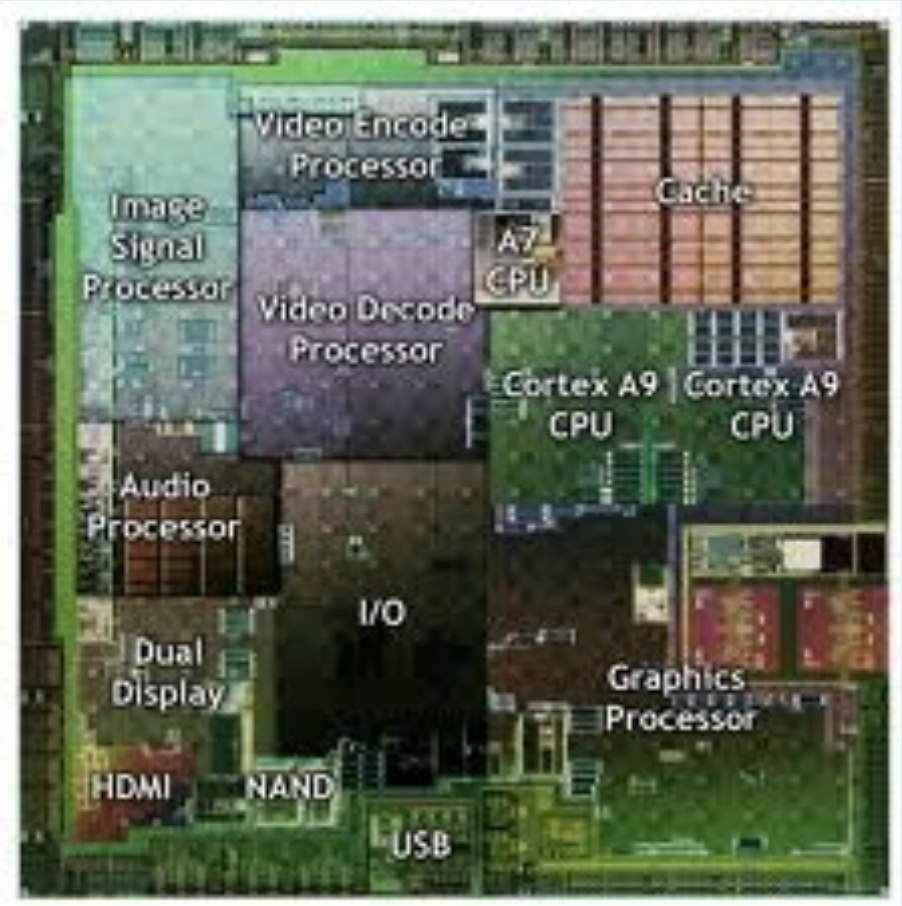
NVIDIA Tegra-2 SOC

- Samsung Galaxy Tab
- Android based Tablet
- Tegra-2 processor

- Nvidia Tegra-2 SOC
- System-on-a-chip
- 2 ARM Cortex-A9 CPUs



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AVR Architecture

- **1996, Norwegian Institute of Technology**
- **A**lf (Egil Bogen) and **V**egard (Wollan)'s **R**ISC processor – AVR
- Atmel, 1997, AT90S1200 microcontroller (8051-like pinout)
- tinyAVR, megaAVR, AVR XMEGA

Chip	Flash	EEPROM	RAM	Pins	Features
tinyAVR	0.5–16 KB	0–512 B	32–512 B	6–32	Tiny, digital I/O, analog input
megaAVR	8–256 KB	0.5–4 KB	0.25–8 KB	28-100	Many peripherals, analog out
AVR XMEGA	16–256 KB	1–4 KB	2–16 KB	44–100	Crypto acceleration, USB I/O

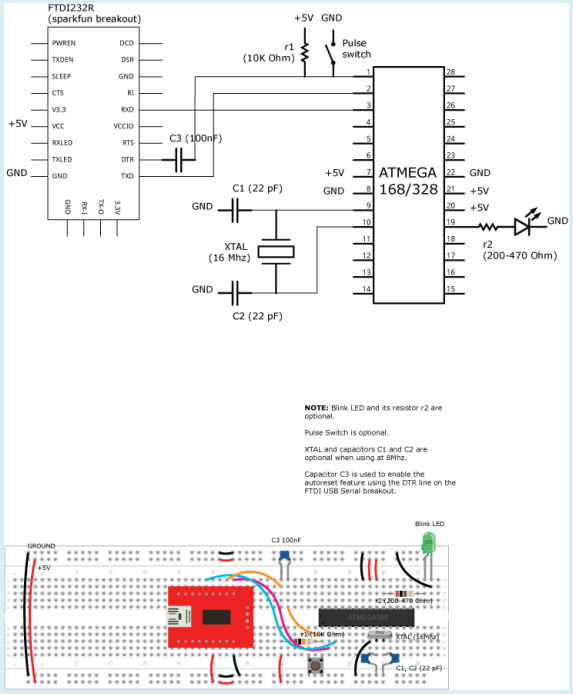
- Embedded systems, Microcontroller, Low-Power and Invisible Computers

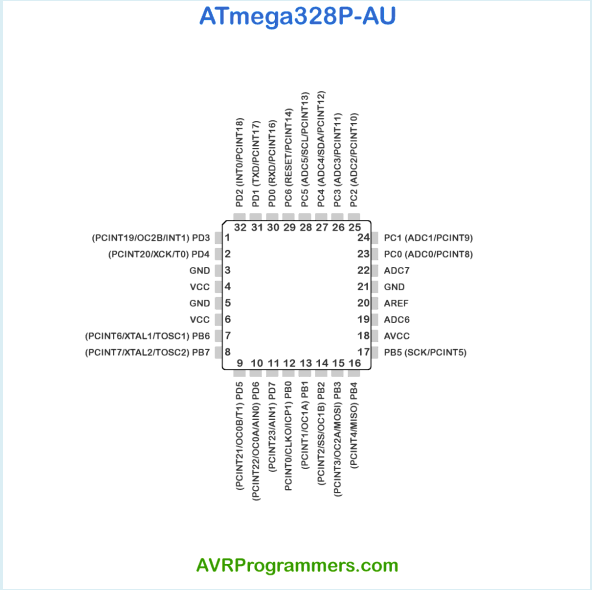
Intro to Computer Architecture

Arduino ATMEGA 168/328 (Diagram)

Atmel megaAVR-168

- 3 Hardware Timers
- 6 PWMs (control light)
- 8 ATDs (read voltage)
- Univ. serial rcv/trans
- Sensor interface
- Watchdog timer
- Real-Time clock
- Others





ECE 394

Introduction to Computer Architecture

Tentative Schedule

Week Tue	Note	Important topics/readings, assignments, due dates, and reminders are listed here so that you can organize your time and academic work.
1 08/20		ECE 394: Intro to Computer Architecture, Syllabus; K-probe; zyBook 1.1 (Intro to Computers); Homework, Quiz, and Exam;
2 08/27	HW-1	HW-1 Discussion; zyBook 1.2-1.5 (eight ideas, processors); HW-1 (due on Blackboard); zyBook 1.6 (performance);
3 09/03	HW-2	9/02 (Labor Day) No Class/Lab; HW-2 (Bb); zyBook 1.7-1.9 (… uni- and multiprocessors, Core i7);
4 09/10	Quiz-1	Quiz-1 Discussion; Handout: Multilevel Computers; Quiz-1 (class test, 30-min / 30-pts, closed book);
5 09/17	Exam-1	Exam-1 Discussion; Handout: Computer Generations; Exam-1 (class test, 65-min / 65-pts, closed book);
6 09/24	Update	zyBook: 3.1 (The Processor: Introduction); zyBook: 3.2-3.3 (The Processor: Datapath, Pipelining);
7 10/01	HW-3	zyBook 3.4-3.5 (Data hazards: Forwarding versus stalling); HW-3 (Bb); zyBook 3.6 (Data hazards and Control hazards);
8 10/08	Mid-Pt HW-4	zyBook 3.7 (Parallelism via instructions); HW-4 (Bb); zyBook 3.8 (Going faster: ILP and matrix multiply);
9 10/15	Fal-Brk Quiz-2	10/12 (Sat) to 10/15 (Tue) (Fall Break) No Class; Quiz-2 (class test, 30-min / 30-pts, closed book);
10 10/22	Exam-2	Exam-2 Discussion; zyBook 4.1 (Memory Hierarchy: Introduction); Exam-2 (class test, 65-min / 65-pts, closed book);
11 10/29	Update	zyBook 4.2-4.3 (Memory Hierarchy: Caches); zyBook 4.4-4.5 (Memory Hierarchy: Virtual memory);
12 11/05	HW-5	zyBook 5.1 (Parallel Processors: Introduction); HW-5 (Bb); zyBook 5.2 (Difficulty of Parallel Processing);
13 11/12	HW-6	zyBook 5.3 (SISD, MIMD, SIMD, SPMD, and vector); HW-6 (Bb); zyBook 5.4 (Hardware multithreading);
14 11/19	Quiz-3	zyBook 5.5-5.6 (Multicore processors, graphics processing units); Quiz-3 (class test, 30-min / 30-pts, closed book);
15 11/26	Thx-Brk	Future of Computers (selected materials); 11/27 (Wed) to 12/01 (Sun) (Thanksgiving Break) No Class;
16 12/03	Exam-3	Exam-3 Discussion; Exam-3 (class test, 65-min / 65-pts, closed book);
Finals		None!
Note: A date in Column 1 indicates the Tuesday of that week. Here, 12/03 is Tueday of Week 16.		