1. Description

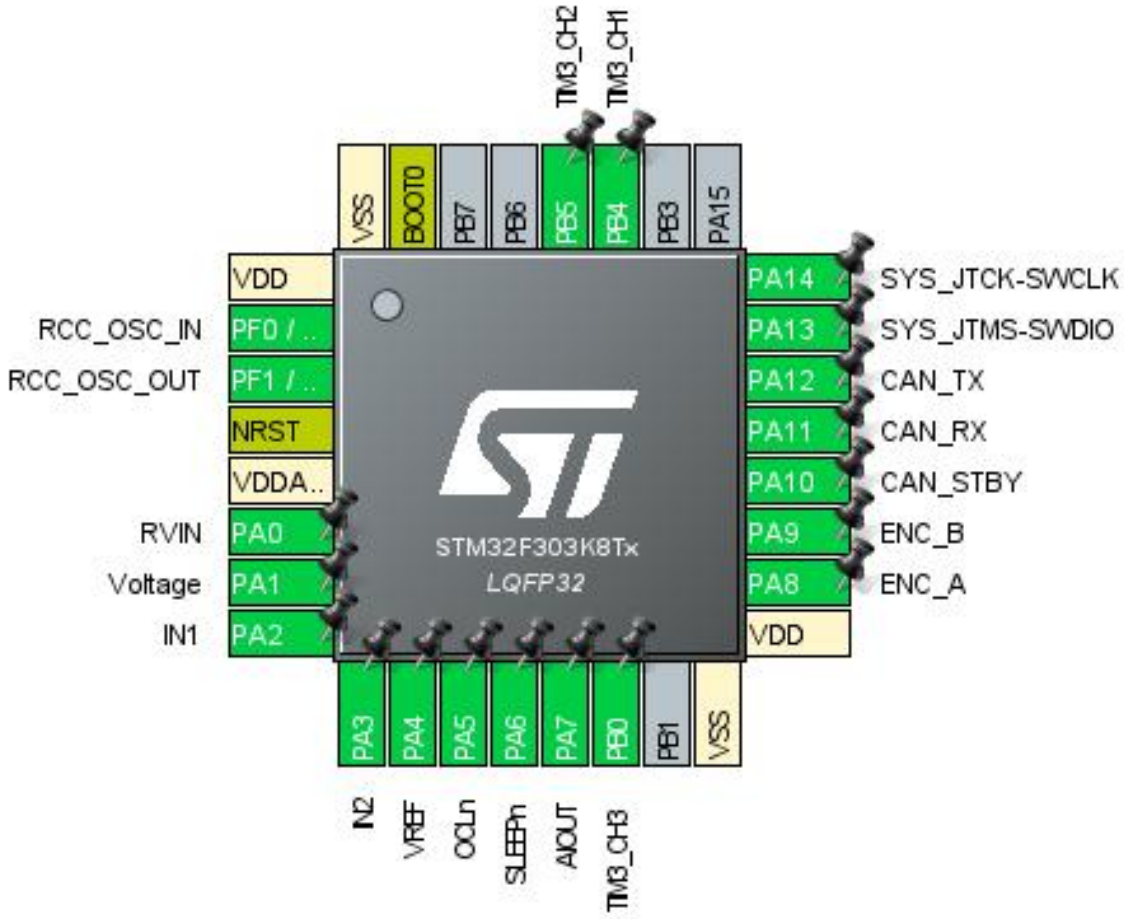
1.1. Project

Project Name	MD_Rev_November
Board Name	custom
Generated with:	STM32CubeMX 5.5.0
Date	02/18/2020

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

2. Pinout Configuration

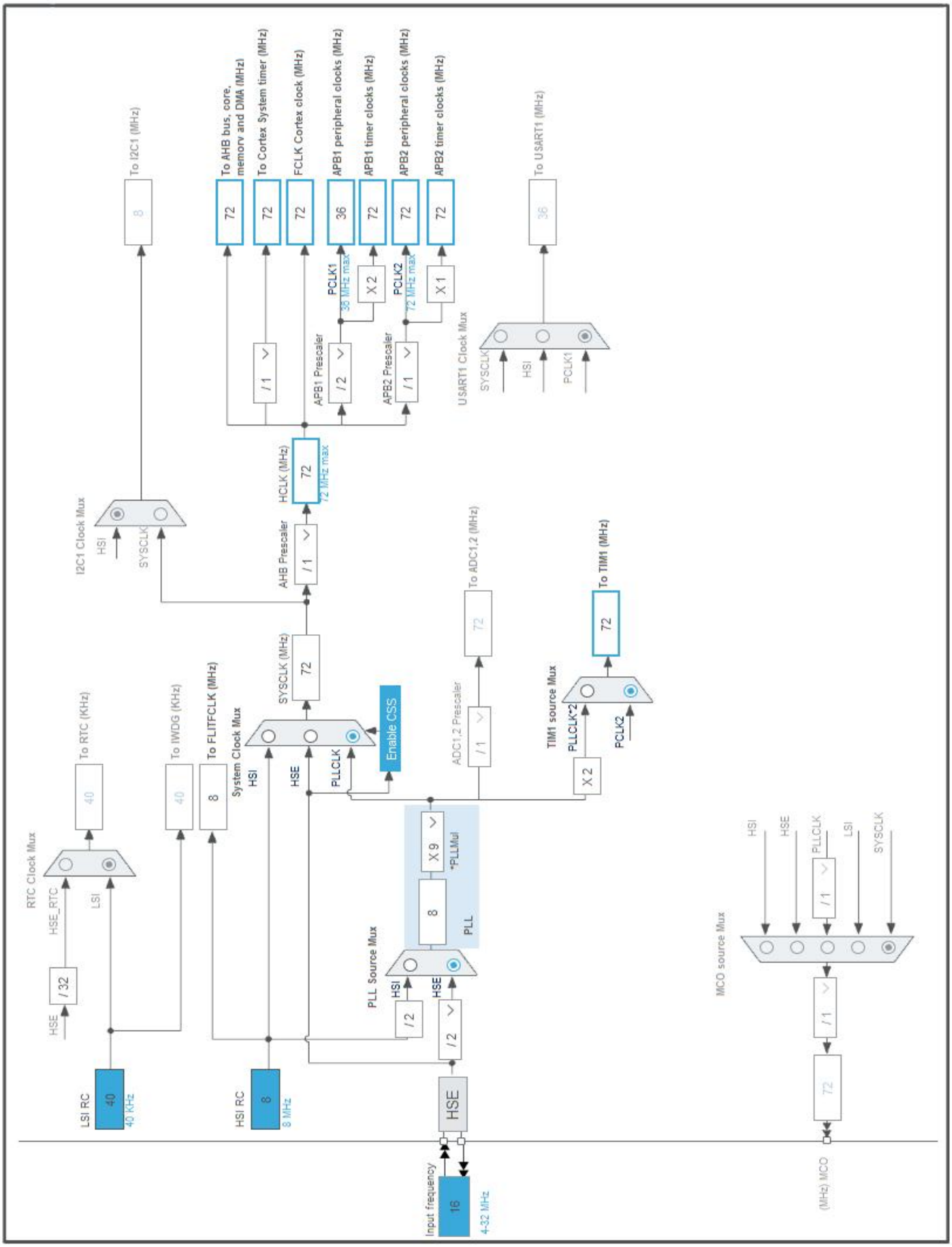


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0 / OSC_IN	I/O	RCC_OSC_IN	
3	PF1 / OSC_OUT	I/O	RCC_OSC_OUT	
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	ADC1_IN1	RVIN
7	PA1	I/O	ADC1_IN2	Voltage
8	PA2	I/O	TIM15_CH1	IN1
9	PA3	I/O	TIM15_CH2	IN2
10	PA4	I/O	DAC1_OUT1	VREF
11	PA5 *	I/O	GPIO_Input	OCLn
12	PA6 *	I/O	GPIO_Output	SLEEPn
13	PA7	I/O	ADC2_IN4	AIOUT
14	PB0	I/O	TIM3_CH3	
16	VSS	Power		
17	VDD	Power		
18	PA8	I/O	TIM1_CH1	ENC_A
19	PA9	I/O	TIM1_CH2	ENC_B
20	PA10 *	I/O	GPIO_Output	CAN_STBY
21	PA11	I/O	CAN_RX	
22	PA12	I/O	CAN_TX	
23	PA13	I/O	SYS_JTMS-SWDIO	
24	PA14	I/O	SYS_JTCK-SWCLK	
27	PB4	I/O	TIM3_CH1	
28	PB5	I/O	TIM3_CH2	
31	BOOT0	Boot		
32	VSS	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	MD_Rev_November
Project Folder	D:\Git\RS555_MD\MD_Rev_November
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	025083_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Sequence

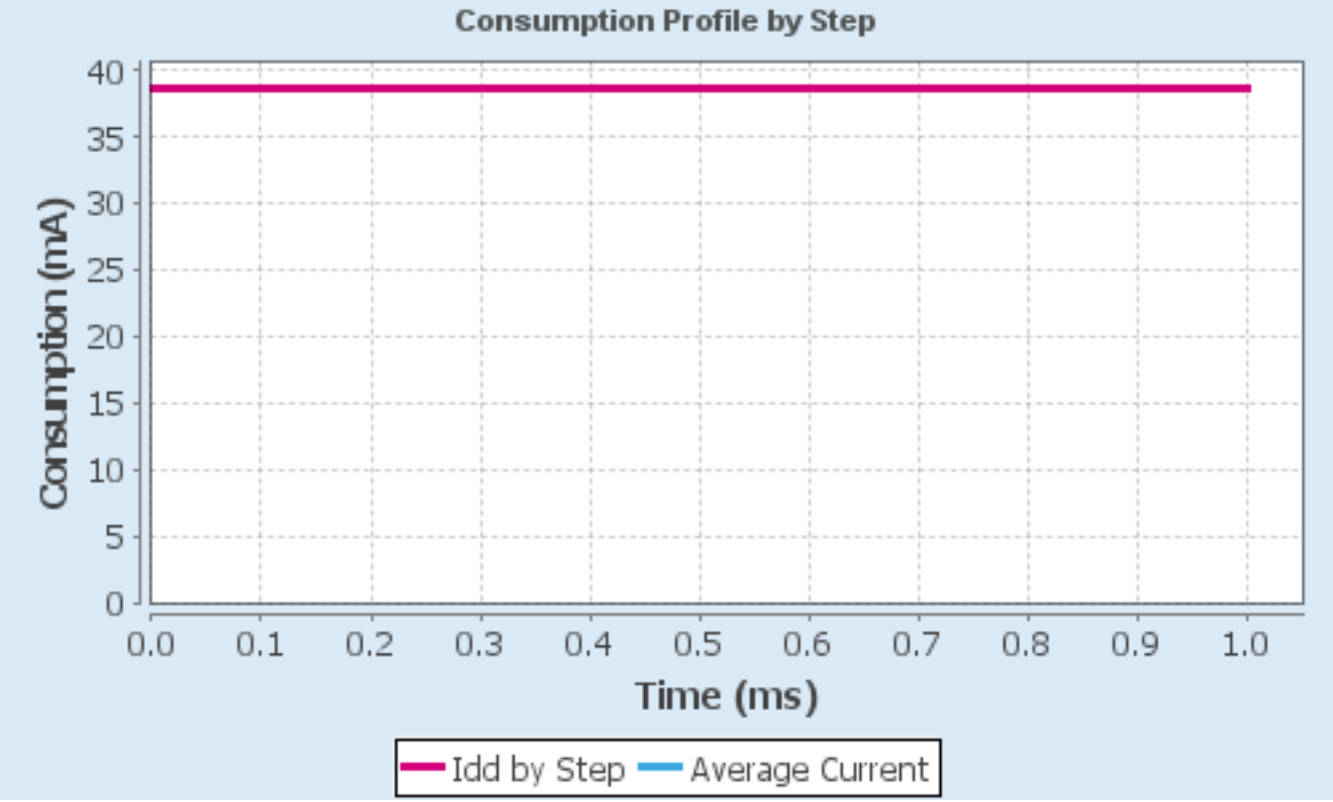
Step	Step1
Mode	RUN
Vdd	3.6
Voltage Source	Battery
Range	No Scale
Fetch Type	FLASH
CPU Frequency	72 MHz
Clock Configuration	HSEBYP PLL
Clock Source Frequency	8 MHz
Peripherals	ADC1:Single-ended_5MSPS ADC2:Single-ended_5MSPS CAN DAC1:OUT1 GPIOA GPIOB GPIOF TIM1 TIM3 TIM15
Additional Cons.	0 mA
Average Current	38.68 mA
Duration	1 ms
DMIPS	63.0
Ta Max	96.65
Category	In DS Table

6.4. RESULTS

Sequence Time	1 ms	Average Current	38.68 mA

Battery Life	0	Average DMIPS	63.0 DMIPS

6.5. Chart



7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data preserved ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**19.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**19.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

mode: IN4

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 4 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data preserved ***
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	**19.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. CAN

mode: Mode

7.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**9 ***
Time Quantum	**250.0 ***
Time Quanta in Bit Segment 1	**6 Times ***
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

7.4. DAC1

mode: OUT1 Configuration

7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

7.5. GPIO

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.7. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.8. TIM1

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***

____ Parameters for Channel 1

____

Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**3 ***

____ Parameters for Channel 2

____

Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**3 ***

7.9. TIM3

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1023 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1

Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. TIM15

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1023 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1

Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	RVIN
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	Voltage
ADC2	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	AIOUT
CAN	PA11	CAN_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA12	CAN_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
DAC1	PA4	DAC1_OUT1	Analog mode	No pull up pull down	n/a	VREF
RCC	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1 / OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	ENC_A
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	ENC_B
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull up pull down	Low	
	PB4	TIM3_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull up pull down	Low	
TIM15	PA2	TIM15_CH1	Alternate Function Push Pull	No pull up pull down	Low	IN1
	PA3	TIM15_CH2	Alternate Function Push Pull	No pull up pull down	Low	IN2
GPIO	PA5	GPIO_Input	Input mode	No pull up pull down	n/a	OCLn
	PA6	GPIO_Output	Output Push Pull	No pull up pull down	Low	SLEEPn
	PA10	GPIO_Output	Output Push Pull	No pull up pull down	Low	CAN_STBY

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**Medium ***
ADC2	DMA1_Channel2	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC2: DMA1_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
CAN TX interrupt	true	0	0
CAN RX0 interrupt	true	0	0
CAN RX1 interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
CAN SCE interrupt	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger and commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM6 global and DAC1 underrun error interrupts	unused		
Floating point unit interrupt	unused		

*** User modified value**

9. Software Pack Report