

Digital Transmission Laboratory

RX FFT

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- Avalon Streaming Interface
- Timing Diagramm
- Blockdiagramm
- Abschätzung des HW Aufwandes
- Testbench

FFT IP Cores

- Variable Streaming FFT
 - Single-precision floating-point und fixed-point
 - Input und output Reihenfolgen
 - natural
 - digit-reversed
 - DC-centered
 - 8 bis 32-bit Daten und Twiddle Bitbreiten
- Fixed Transform Size FFT
 - Block floating-point
 - Streaming, Buffered Burst oder Burst Modus
 - Single-output oder Quad-Output (auch mehrere parallel)

FFT IP Cores

Niedrigste Ressourcen

	Modus	Output	In/Out Reihenfolgen	Calculation Latency	Throughput Latency	ALMs	DSP	M10K	Registers
Gewählte Version	Burst	Single	natural	223	653.9	2	3	1228	
	Burst	Single	natural	423	166	639	2	3	1382
	Burst	Quad	natural	423	166	1534	6	8	3617
	Bufferd Burst	Quad	natural	171	160	1528	6	16	3713
	Streaming	Quad	natural	128	128	1651	6	20	3878
	Variable Streaming	Quad	natural	128	256	8611	36	62	15156
					Nicht relevant für Burst				

Matlab Modell

FFT IP Cores

Reicht die Latenz?

		Taktrate/Hz	Zeit/s	Zeit/ns	Takte
sys_clk_i	80 MHz	8.00E+07	1.25E-08	12.50	1
Baudrate	1.6 MS/s	2.00E+06	5.00E-07	500.00	40
Calculation Latency				5287.5	423
Zeit für 128 Chips				64000	5120
Zeit zum Ein- und Auslesen				3200	256
Benötigte / Verfügbare Zeit	0.132617				

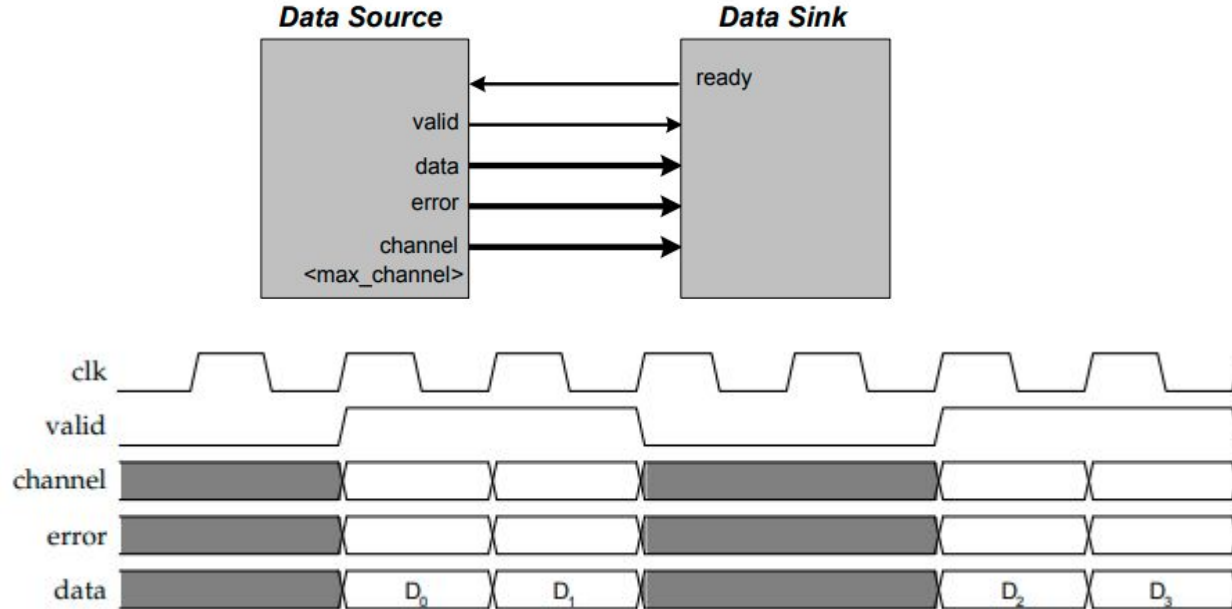
FFT IP Cores

Benötigen wir einen Eingangsbuffer?

		Taktrate/Hz	Zeit/s	Zeit/ns	Takte
sys_clk_i	80 MHz	8.00E+07	1.25E-08	12.50	1
Baudrate	1.6 MS/s	2.00E+06	5.00E-07	500.00	40
Calculation Latency				5287.5	423
Zeit für 128 Chips				64000	5120
Zeit zum Ein- und Auslesen				3200	256
Benötigte / Verfügbare Zeit	0.132617				
Zeit für 32 Chips				16000	1280
Benötigte / Verfügbare Zeit	0.530469				

Avalon Streaming Interface

- Interface for unidirectional data streams from source to sink



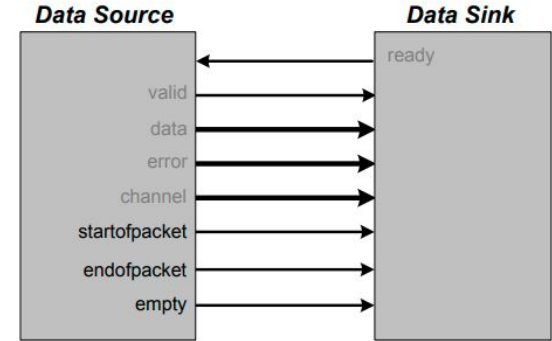
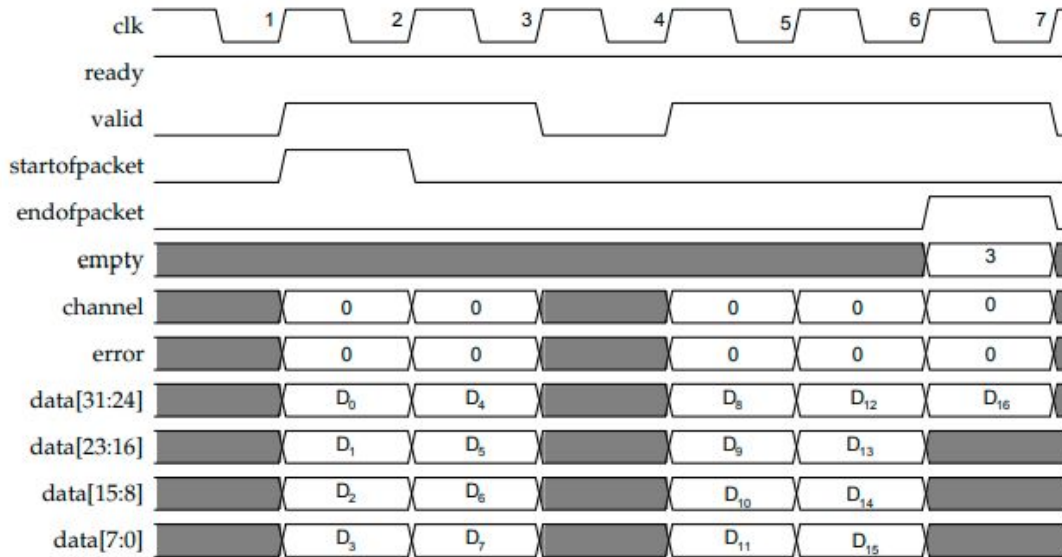
Avalon Streaming Interface

- Handshaking and flow control



Avalon Streaming Interface

- Packet Data Transfers



FFT IP Cores

- FFT Length: 128
- reduzierte Ressourcen: Burst
- Order I/O: natural
- Datenrepräsentation: Block Floating Point
- Datenbreite I/O: 12 bit
- Twiddle-Breite (sin/cos): 8 bit

The screenshot shows the 'Parameters' window for the 'altera_fft_ii' IP core. The window has a title bar with a close button and a 'Parameters' label. Below the title bar, it shows 'System: fft_ofdm' and 'Path: fft_ii_0'. There are two buttons: 'Details' and 'Generate Example Design...'. The main area has two tabs: 'Basic' and 'Advanced'. The 'Advanced' tab is selected. It contains several expandable sections: 'Transform', 'I/O', 'Data and Twiddle', and 'Latency Estimates'. The 'Transform' section shows 'Length: 128' and 'Direction: Bi-directional'. The 'I/O' section shows 'Data Flow: Burst', 'Input Order: Natural', and 'Output Order: Natural'. The 'Data and Twiddle' section shows 'Representation: Block Floating Point', 'Data Input Width: 12 bits', 'Twiddle Width: 8 bits', and 'Data Output Width: 12 bits'. The 'Latency Estimates' section shows 'Calculation Latency: 423 cycles' and 'Throughput Latency: 166 cycles'.

Parameters

System: fft_ofdm Path: fft_ii_0

FFT
altera_fft_ii

Details
Generate Example Design...

Basic Advanced

Transform

Length: 128
Direction: Bi-directional

I/O

Data Flow: Burst
Input Order: Natural
Output Order: Natural

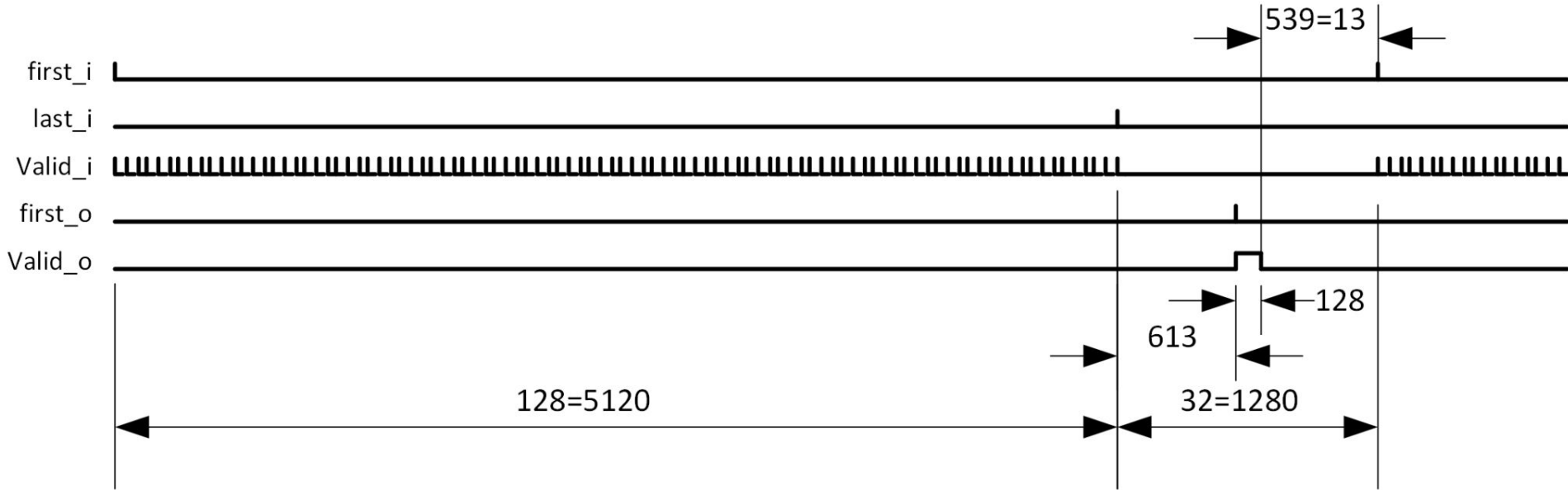
Data and Twiddle

Representation: Block Floating Point
Data Input Width: 12 bits
Twiddle Width: 8 bits
Data Output Width: 12 bits

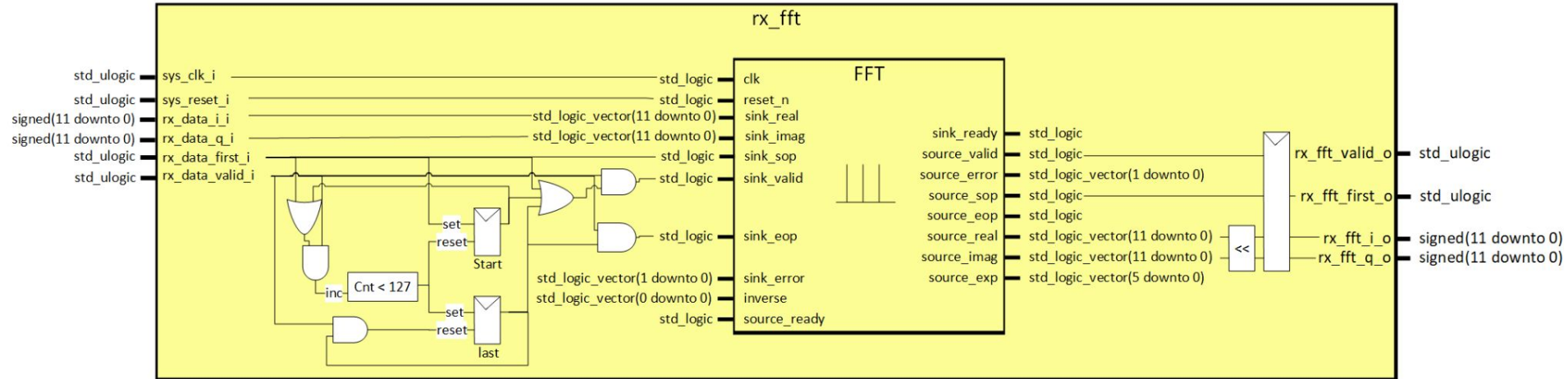
Latency Estimates

Calculation Latency: 423 cycles
Throughput Latency: 166 cycles

Timing Diagramm



Blockdiagramm



Abschätzung des HW Aufwandes

- Register = 1425 (Output Register = $22+2$; Control = $7+2$)
- ALMs: 600
- Blockram = 3520 bits
- DSP = 2 (4 Fixed Point Signed Multiplier)

Testbench