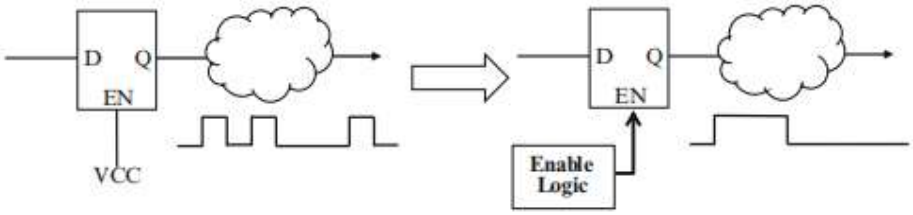
Project Title: **Optimization of FPGA Designs for Power Consumption**

Project Overview:
The increasing demand for energy efficiency in electronic devices has made power consumption a critical factor in the design of digital systems, including those implemented on Field-Programmable Gate Arrays (FPGAs). This project aims to explore, implement, and compare various optimization techniques to minimize power consumption in FPGA designs, enhancing their suitability for power-constrained applications such as mobile, IoT, and edge computing devices.



Objectives:

- Choose and implement a representative digital system to serve as the base design for optimization. Ensure the selected design is complex enough to demonstrate optimization benefits but simple enough for thorough analysis.
- Analyze and investigate existing methodologies and tools for optimizing FPGA designs with a focus on power reduction by using representative design. It could be
    - **Hardware-Level Optimizations**:
        1. Resource sharing and minimization.
        2. Clock gating and dynamic voltage scaling.
        3. Pipelining for reduced capacitance.
    - **Design-Level Optimizations**:
        1. Algorithmic optimizations (e.g., using more power-efficient algorithms).
        2. Use of power-optimized IP cores.
    - **Tool-Based Optimizations**:
        1. Utilizing FPGA vendor tools for power optimization.
        2. Exploring third-party tools for additional power reduction strategies.
- Measure and compare the power consumption for each technique using appropriate measurement approach and tools

Equipment available at Rohde and Schwarz:

- FPGA development board and FPGA Tools for implementation and testing.
- Appropriate power measurement tools e.g., oscilloscopes and power analyzers

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