Yuri Fioretti

Curriculum Vitae

General Information

Name	Yuri Fioretti
Birth date	07/02/1991
Citizenship	Italian

Education and Master Thesis

2011–2014 **Bachelor degree**, *Universita' degli studi Roma Tre*, Rome, .
Electronic engineering. 99/110

2014–2016 **Master degree**, *Politecnico di Torino*, Torino, *Electronic engineering 110/110*.

Thesis title *Control software acceleration through Application Specific Instruction Set Processors (ASIPs) exploration*

Supervisors Professor Luciano Lavagno & Ing. Alberto Ferrari

Description Simulink modeling of a Field Oriented Controller based on Space Vector Pulse Width Modulation; Manual design of an Application Specific Instruction set Processor, generation of multiple processors through design space exploration; Processors Pareto set extraction.

Professional Experience

01/2017–Present **FPGA hardware designer**, Virtual Open Systems, Grenoble.
Hardware and Software implementations for Virtex-ultrascale FPGA for virtualization environments with the scope of exposing hardware accelerators.

04/2016–12/2016 **Intern**, A.L.E.S, Rome.
Research on Application Specific Instruction Set Processor design environments and development of a Pareto set of processors for a Field Oriented Control and Space Vector Pulse Width Modulation driving system for Permanent Magnet Synchronous Motors.

Projects

PCB design Development of a high performance A/D acquisition board. (Bill of materials, PCB)

Integrated Architecture Design of a custom DLX RISC processor through VHDL code development, simulation, synthesis and layout Design.

Synthesis optimizations Developing of a tcl script for Synopsys Design Vision to perform a custom dual Vth replacement and cell re-sizing on a given design

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ASIP design	Development of an ASIP processor with TTA architecture for computing the discrete cosine transform over a given number of samples. Synthesis and layout design for ASIC production.
Multithread C	Development of the C code of a Blowfish cipher employing POSIX multithreading
ISO-26262 standard	Development of the model, and generation of a C code through Simulink, for developing an ISO-26262 compliant firmware for an ASIL D application (ultrasonic overtaking sensor)
Microwave circuits design	Design of a 2.4 GHz edge-fed rectangular single patch radiator. Insertion of impedance transformer, frequency response simulation, production of the device and frequency response measurement
IoT	Design of an IoT data acquisition board in greenhouse environment sensing air humidity, temperature, light, ground humidity. Development of a prototype and the PCB

Hardware skills

PCB Design	Altium designer, Orcad, Eagle
IC Design	VHDL, Verilog, IP-block Assembly, High level synthesis
Simulation	Mentor Graphics Modelsim
FPGA	Xilinx Vivado, Vivado HLS, Altera Quartus
ASIC	(Synthesis) Synopsys Design Compiler, (Layout) Cadence Encounter, (Verification) Synopsys Tetramax

Software skills

Programming and scripting	C, C++, Matlab (Simulink), tcl, bash
Miscellaneous	Microsoft and Unix-based OSs, Microsoft office suite, LaTeX, OpenOffice suite

General Skills

Projects management	Experienced in team work, project planning (Gantt), project revisioning systems (Git), hiring
Human Relations	Integration capability in any environment. High capability of make new acquaintances. High attitude to link informations.
General skills	Several instruments musician. Guitar teacher for children. Sport and Cooking passionate.

Languages

Italian	**Mothertongue**	
English	**Upper-intermediate**	*Conversationally fluent*
Spanish	**Basic**	*Basic words and phrases only*
French	**Basic**	*Basic words and phrases only*

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