
```

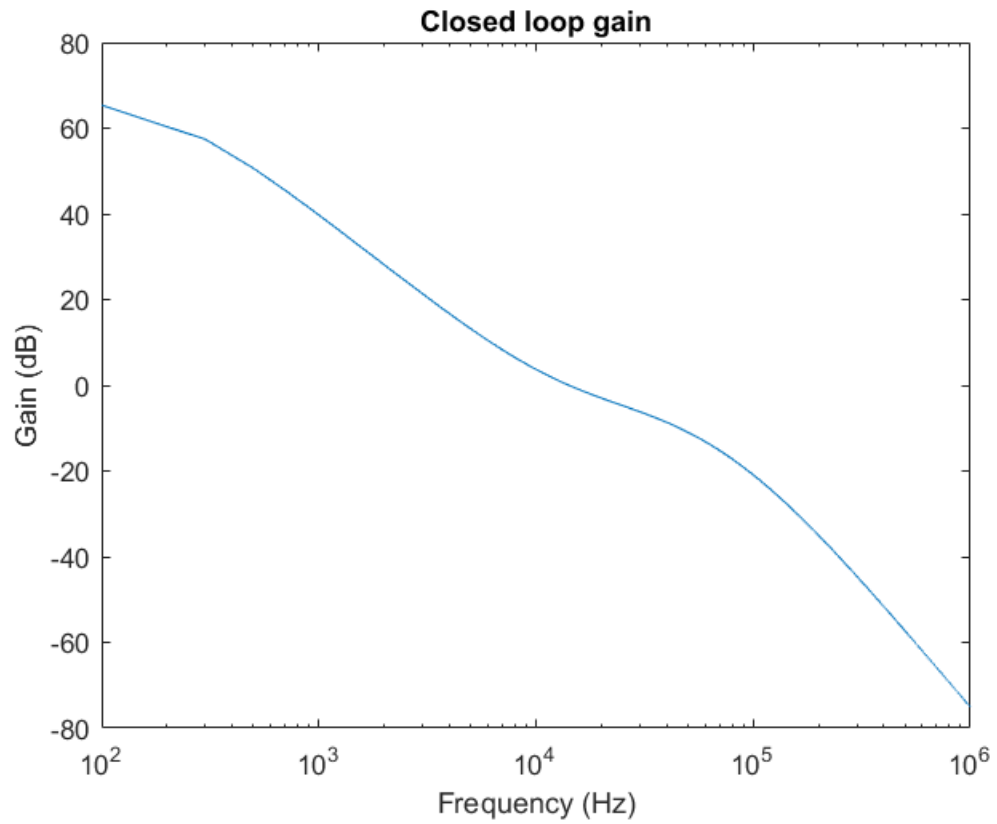
% Dylan Doucette & Corbin Study
% ECE 402
% Loop Compensation Network Design

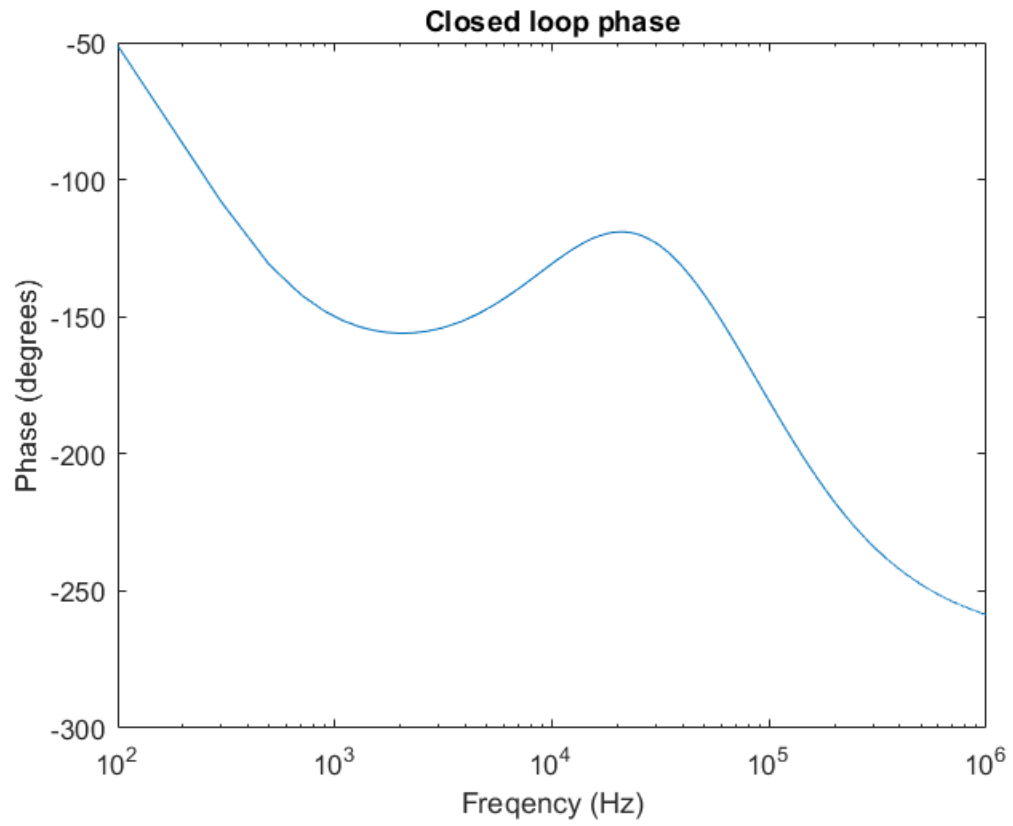
s=linspace(100*2*pi,1e6*2*pi,5000);
n=2; % Number of phases
Vin=36;
Vo=28;
Ls=0.00001; % Inductor
Ri=0.004*22.856; % Resistance of sense resistor multiplied by
    error amplifier gain
Tsw=1./150000;
RCo=0.014; % ESR of output capacitor
Co=3.*0.000330; % Output capacitance
RL=0.875; % Max load resistance
D=Vin/Vo; % Ideal duty cycle
Toff=(1-D).*Tsw; % Off time of high-side MOSFETs
w2=pi./(Tsw);
sn=Ri.*(Vin-Vo)./Ls; % Inductor current slopes
sf=Ri.*Vo./Ls;
se=Vin.*Ri./Ls; % Slope of internal compensation ramp
Q2=1./(pi.*((sn+se)./(sn+sf)-0.5));
k2=-Ri./(Ls.*Q2.*w2);
Gcv=n.*(1./(1+((li.*s)./(Q2.*w2))+((li.*s).^2)/(w2.^2))).*(RL./
    (Ri.*(1-(k2.*RL./Ri)))).*((RCo.*Co.*li.*s+1)./(((RL+RCo).*Co-
    (RL.*RCo.*Co.*k2./Ri))./(1-(RL.*k2./Ri))).*s.*li+1)); % Transfer
    function for current mode buck converter
Kref=0.02857;
gm=n.*0.002; % Gain of voltage feedback amplifier
Ro=1.5e6; % Output resistance of internal voltage
    feedback amplifier
Rth=16900; % Component values in compensation network
Cth=620.*1e-12;
Cthp=240.*1e-12;
sthp=1./(Rth.*(Cth.*Cthp)./(Cth+Cthp)); % Pole 1 generated by loop
    compensation network
sthz=1./(Rth.*Cth); % Zero generated by loop
    coompensation network
spo=1./(Ro.*Cth); % Pole 2 generated by loop
    compensation network
As=gm.*Ro.*(((1+(li.*s)./sthz))./((1+(li.*s)./spo).*(1+(li.*s)./
    sthp))); % Transfer function of compensation network
Ts=Gcv.*Kref.*As; % Closed loop transfer function of current
    mode buck converter
f=s./(2.*pi);
figure;
semilogx(f, 20*log10(Ts));
title('Closed loop gain');
xlabel('Frequency (Hz)');
ylabel('Gain (dB)');
figure;
semilogx(f, rad2deg(phase(Ts)));

```

```
title('Closed loop phase');  
xlabel('Frequency (Hz)');  
ylabel('Phase (degrees)');
```

Warning: Imaginary parts of complex X and/or Y arguments ignored





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