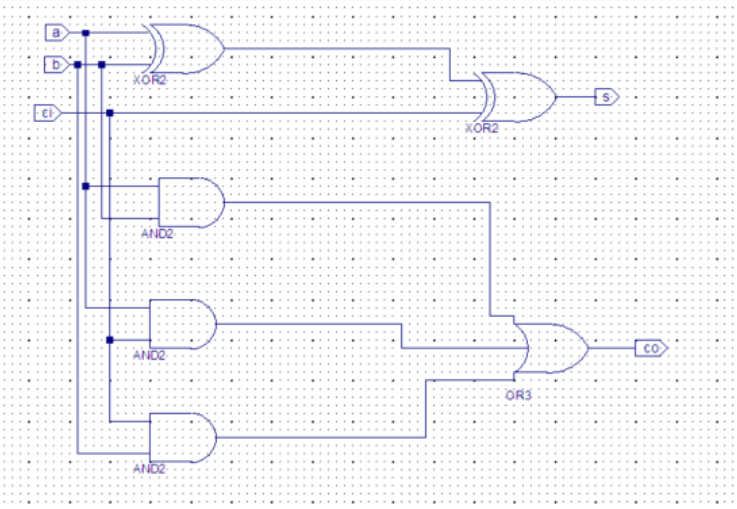
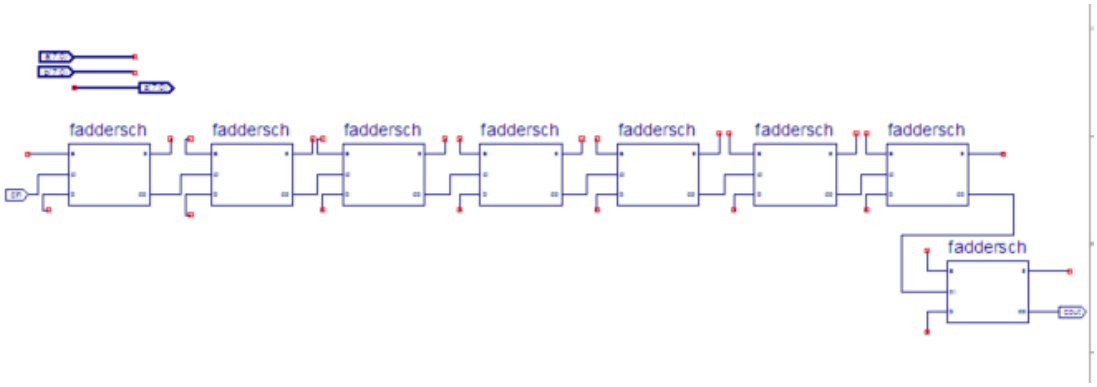
EE533 Lab2

1. Designing and Simulating Synchronous 8-bit adder

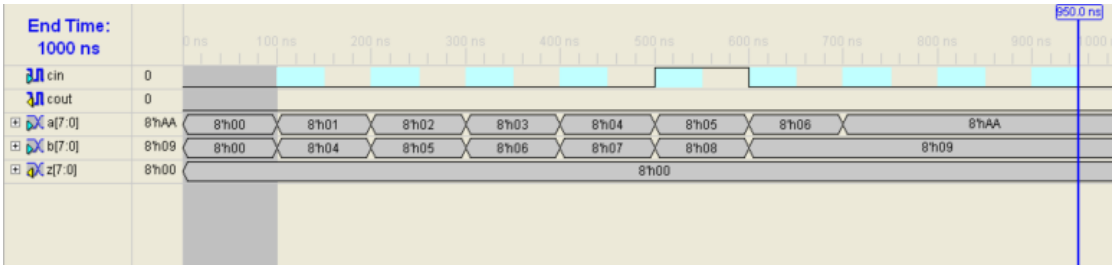
1-bit adder schematic:



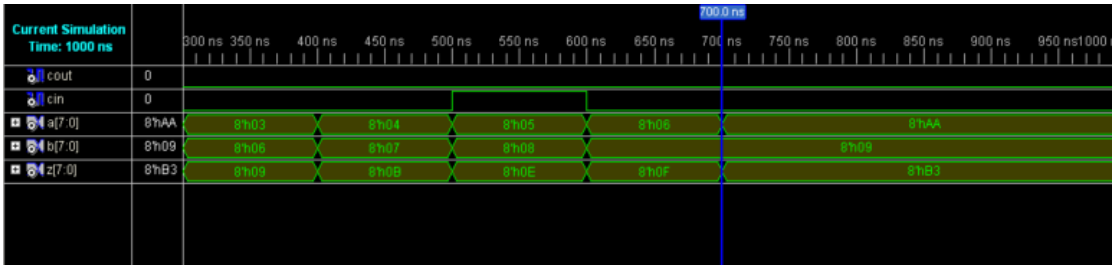
8-bits adder schematic:



8-bits adder testbench:

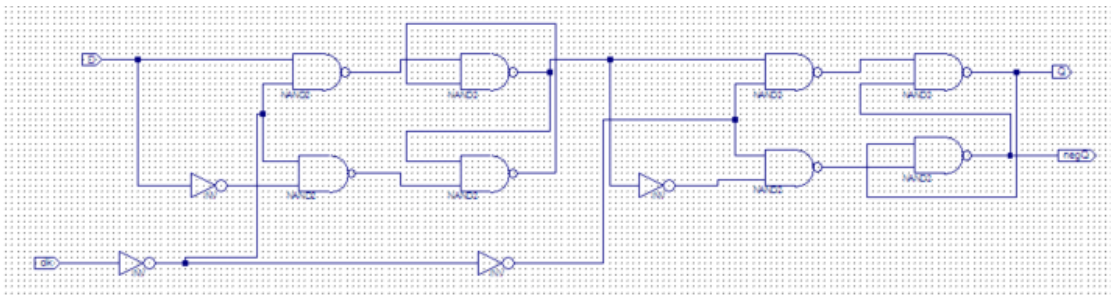


8-bits adder simulation result:

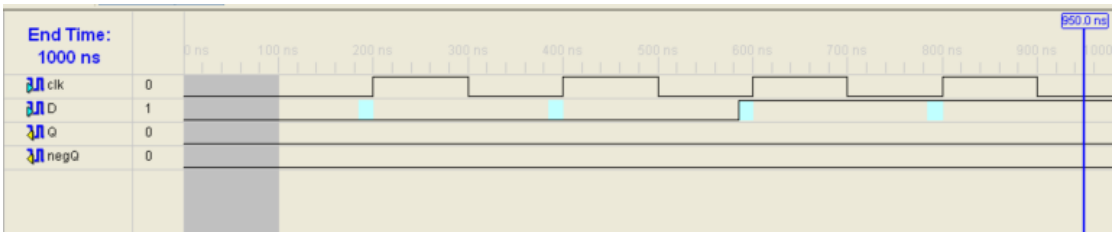


DFF for synchronous

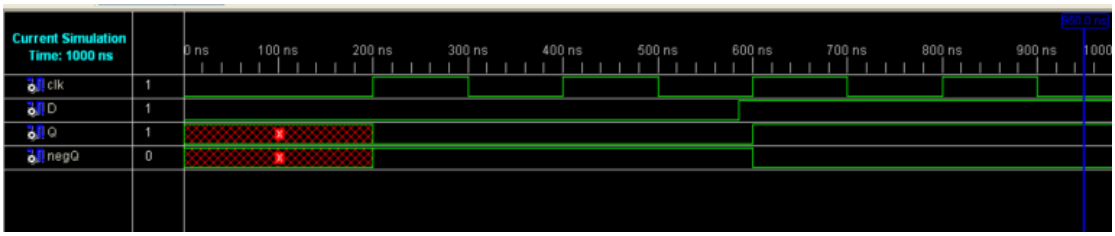
Schematic:



Testbench:

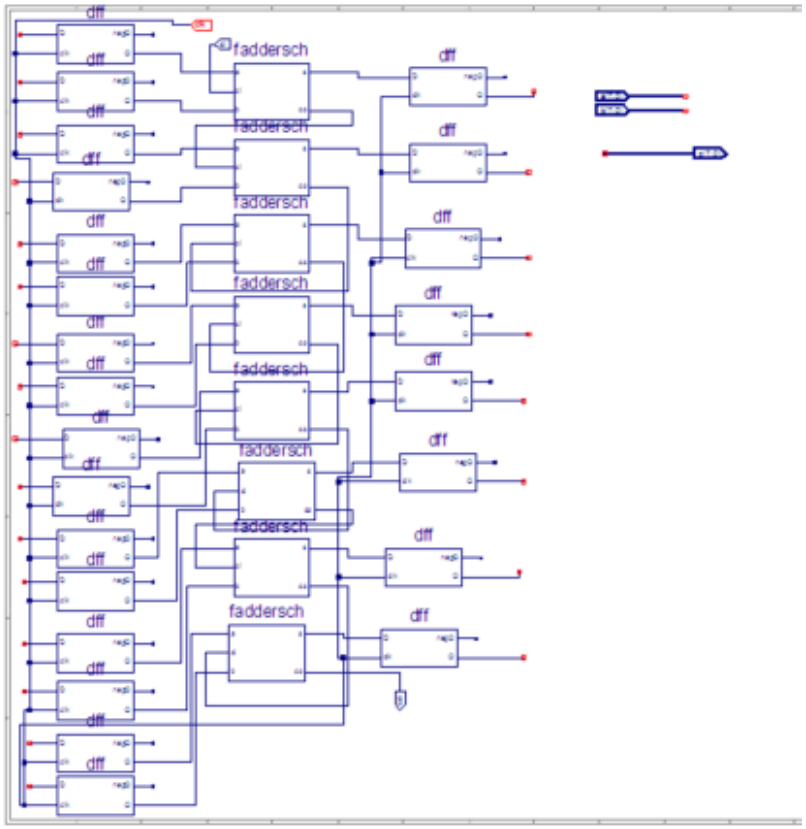


Simulation result:

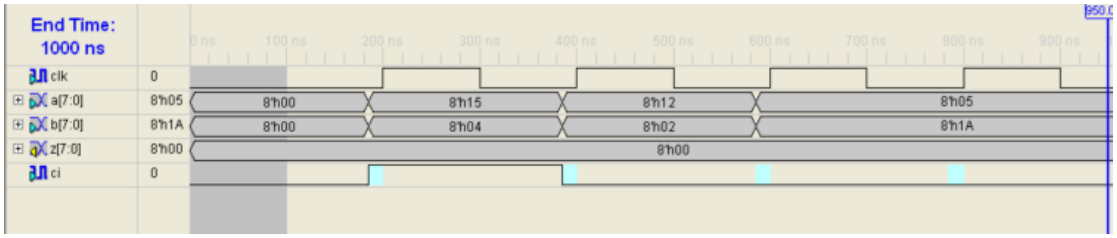


8bit fulladder with dff

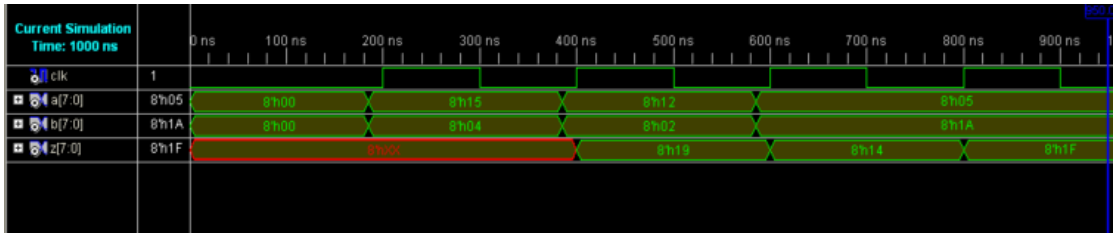
Schematic:



Testbench:

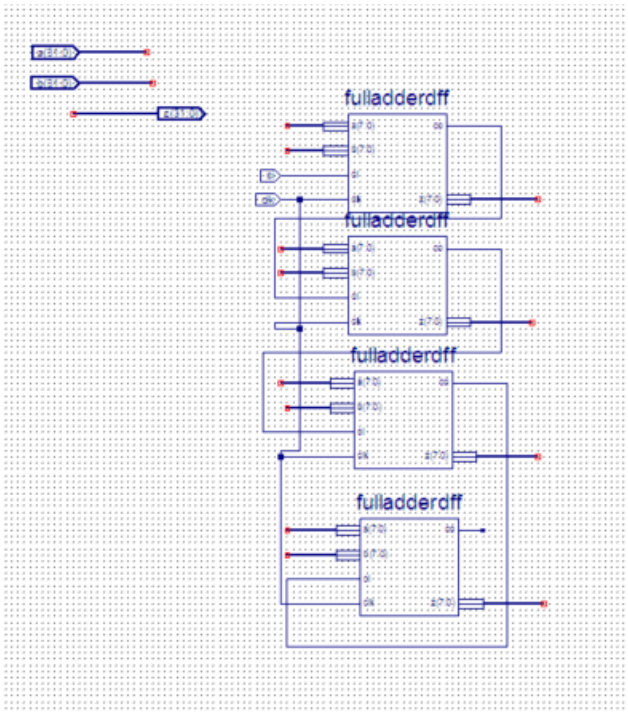


Simulation result:

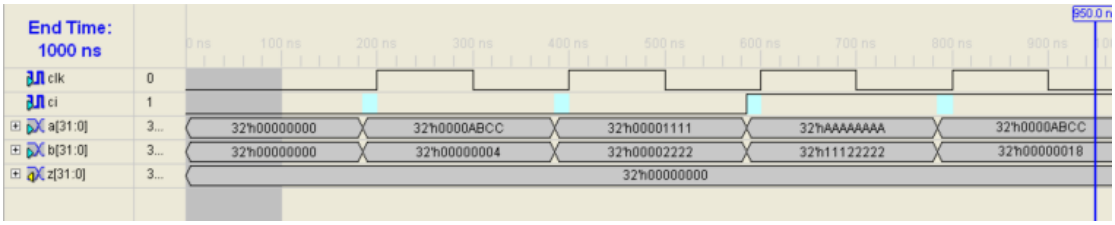


32bit fulladder with dff

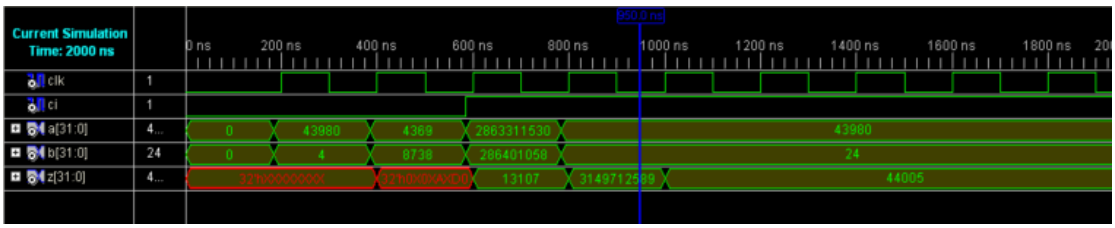
Schematic:



Testbench:



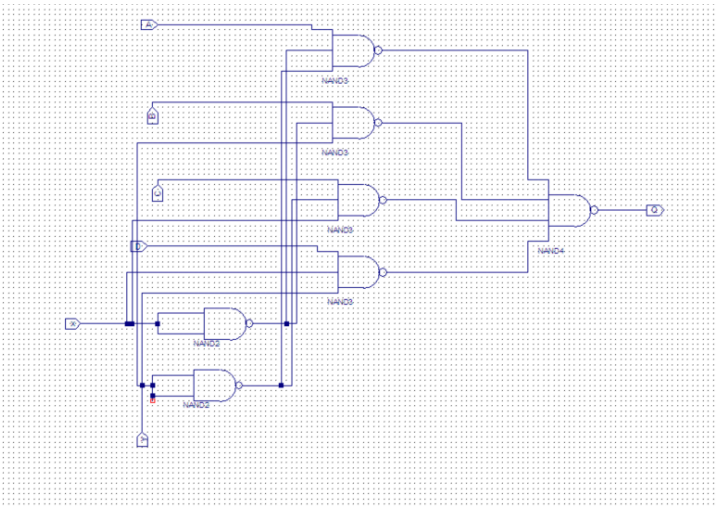
Simulation result:



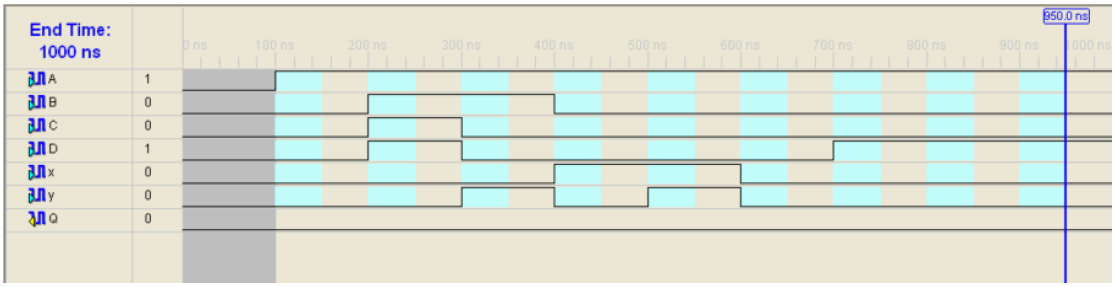
2. Extending Adder into 32-bit ALU

Mux for ALU's sel

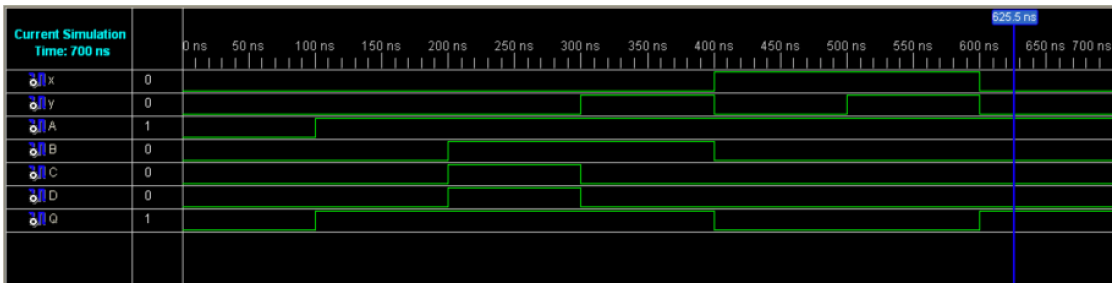
Schemaitic:



Testbench:

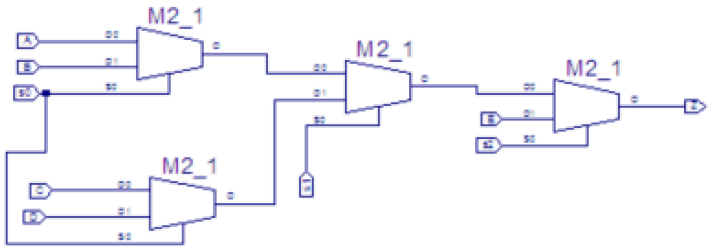


Simulation result:

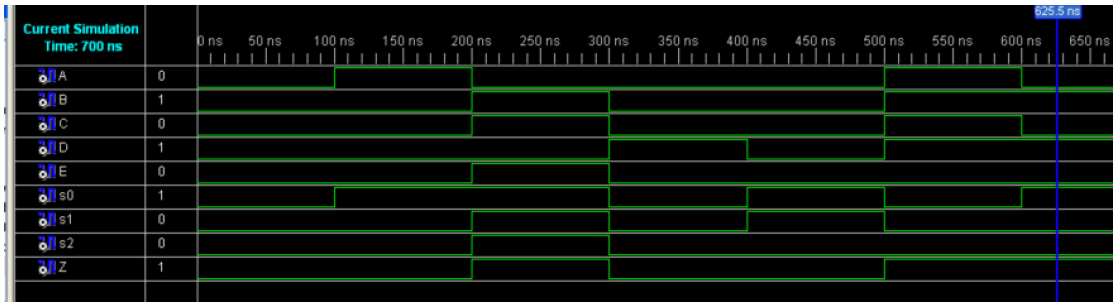


5 input mux for sel

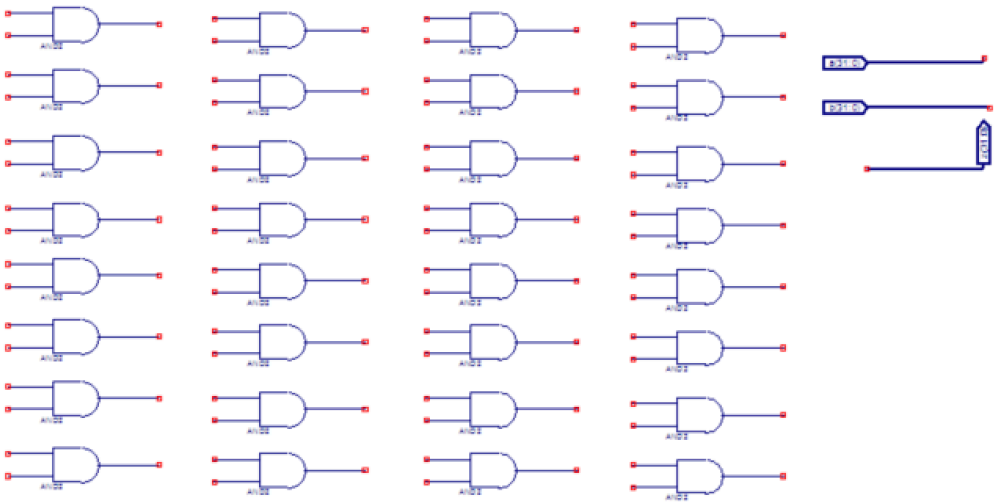
Schematic:

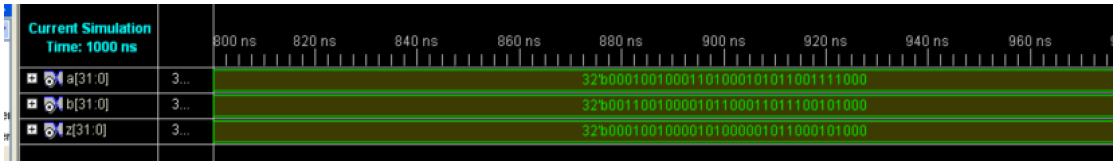


Simulation result:

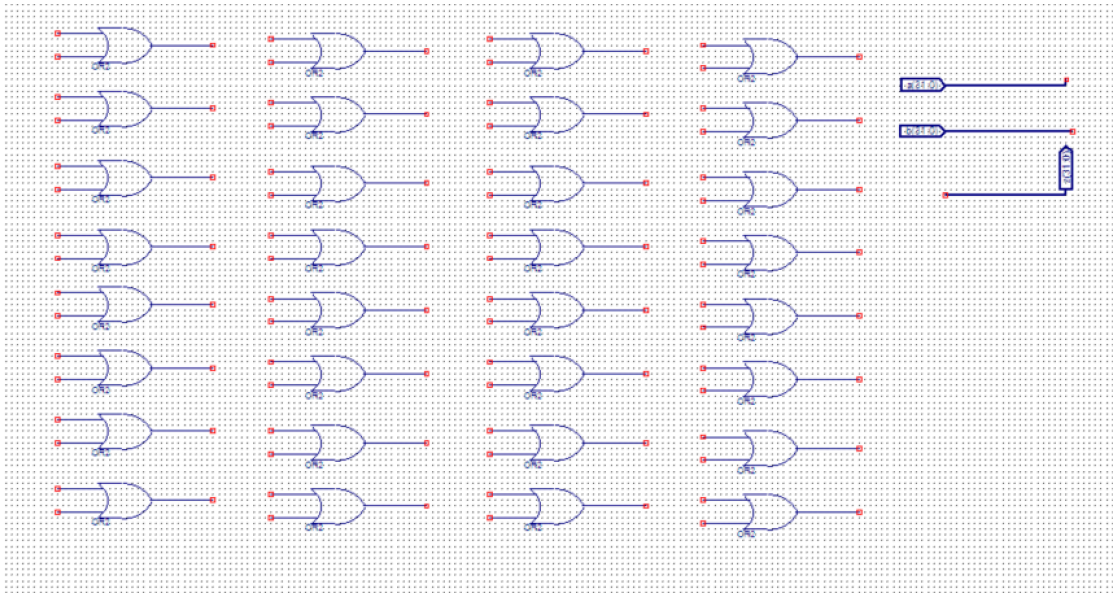


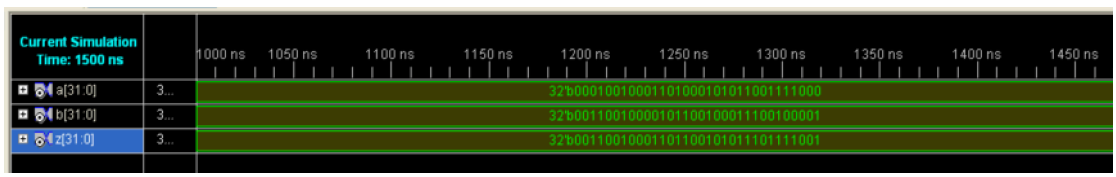
AND function





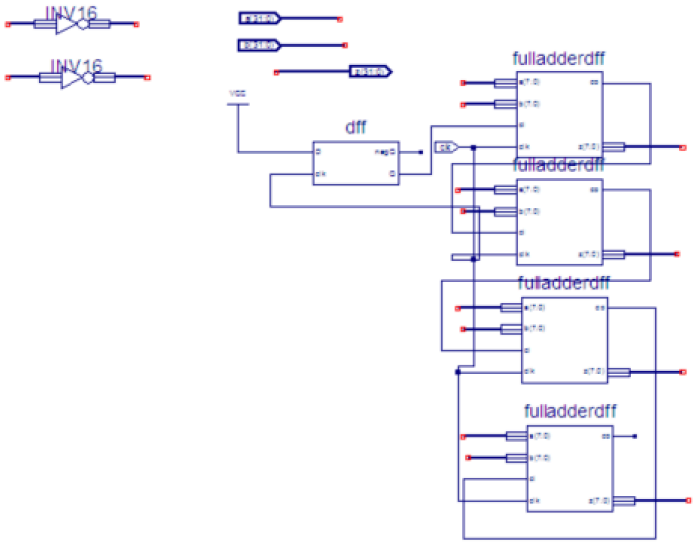
OR function



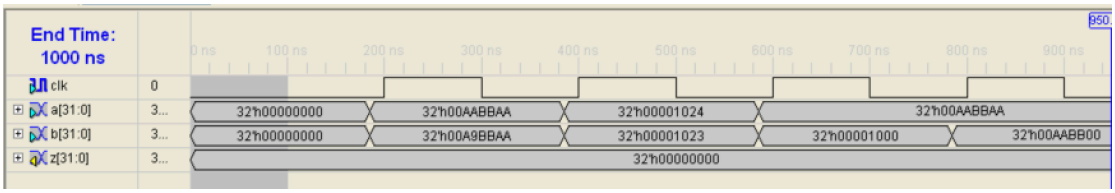


Subtractor

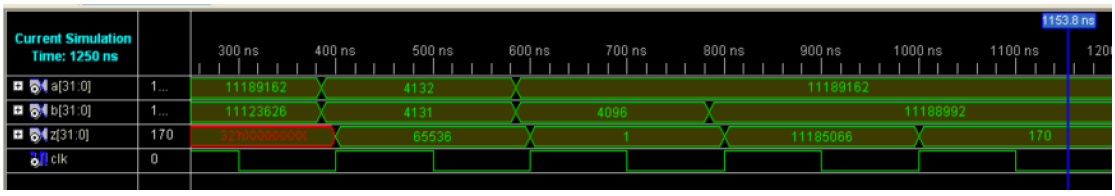
Schematic:



Testbench:

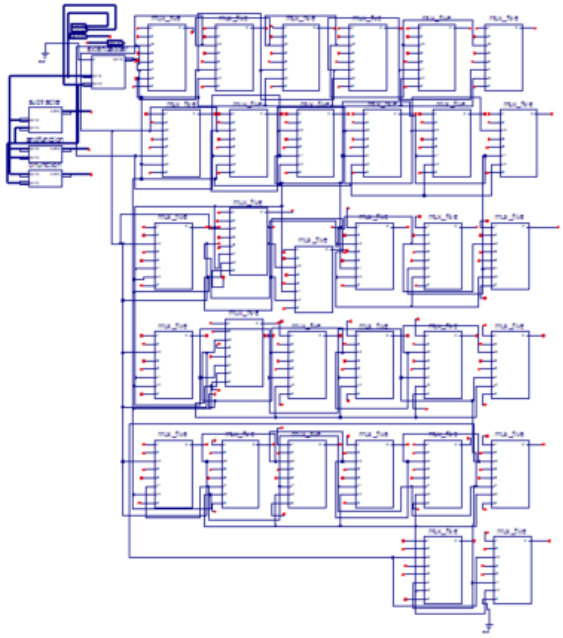


Simulation result:

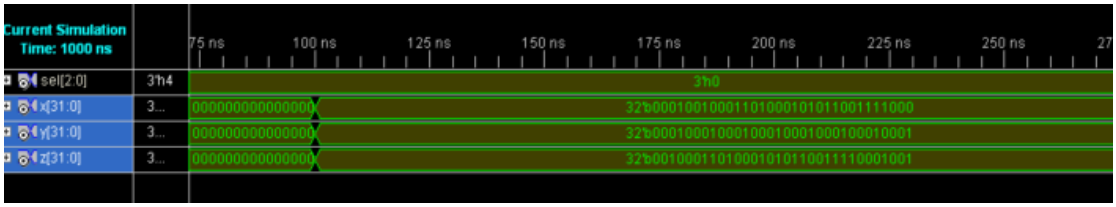


ALU

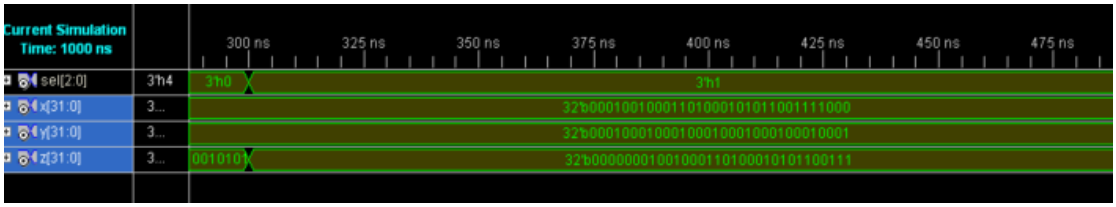
Schematic:



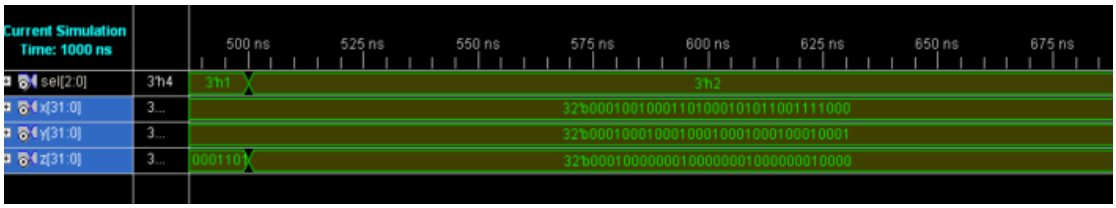
Add: sel=0



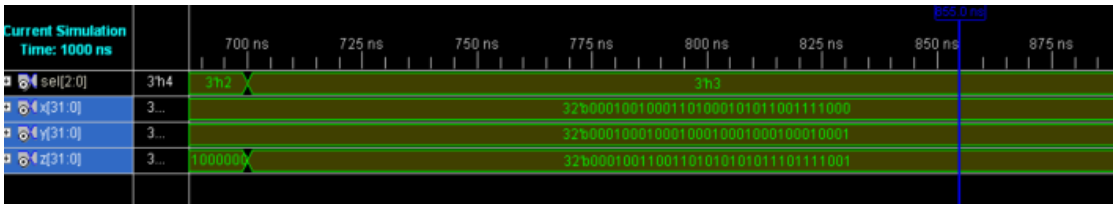
Sub: sel=1



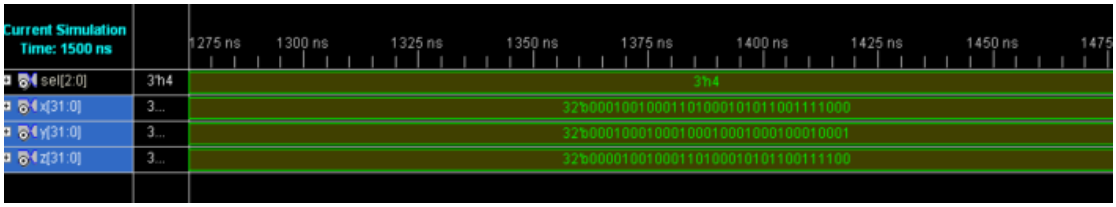
And: sel=2



Or: sel=3



Shift right: sel=4



Log file of the mapper:

```
   mapped into FPGA logic resources.  It can also be used to analyze
   preliminary, logic-level (pre-route) timing with one of the Xilinx static
   timing analysis tools (TRCE or Timing Analyzer).

Design Summary
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Design Summary:
Number of errors:      1
Number of warnings:    0
Logic Utilization:
  Number of 4 input LUTs:           219 out of  1,536   14%
Logic Distribution:
    Number of occupied Slices:                        114 out of    768   14%
    Number of Slices containing only related logic:   114 out of    114  100%
    Number of Slices containing unrelated logic:        0 out of    114    0%
       *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:       219 out of  1,536   14%
   Number of bonded IOBs:            99 out of     98  101% (OVERMAPPED)

Peak Memory Usage:  130 MB
Total REAL time to MAP completion:  1 secs
Total CPU time to MAP completion:   1 secs

NOTES:

   Related logic is defined as being logic that shares connectivity - e.g. two
   LUTs are "related" if they share common inputs.  When assembling slices,
```
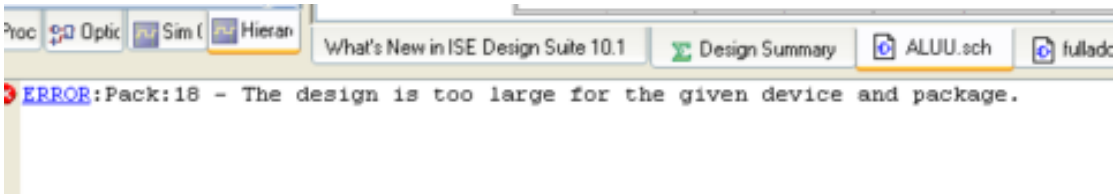

Total LUTs = 219

Number of occupied Slices: 114

Error: number of bonded IOBs 99 out of 98 101% (overmapped)

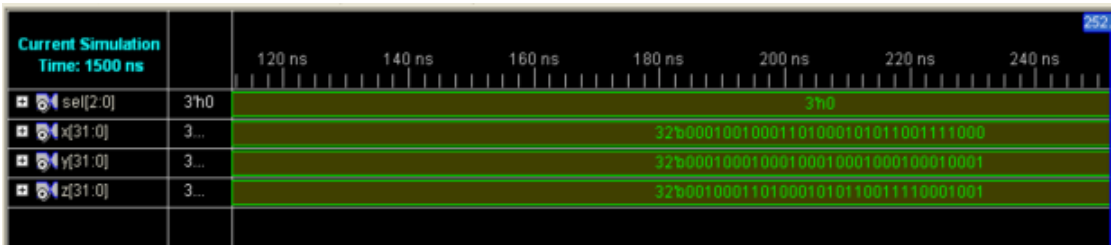


3. Verilog equivalent of 32-bit ALU Verilog

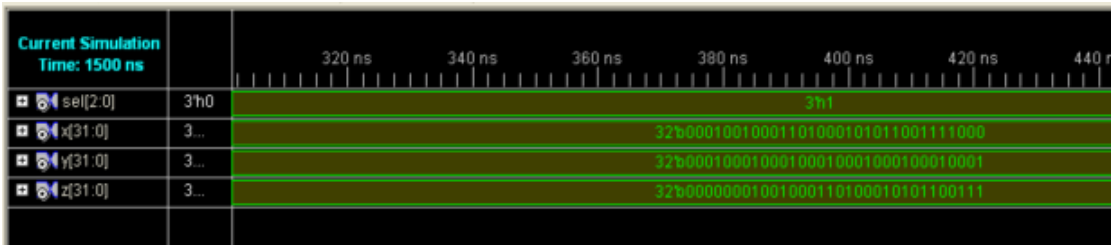
Verilog:

```
module ALUverilog(
    input [31:0] x,
    input [31:0] y,
    input [2:0] sel,
    output reg [31:0] z
    );

always @(*) begin
   case (sel)
      3'd0: z= x+y;
      3'd1: z= x-y;
      3'd2: z= x&y;
      3'd3: z= x|y;
      3'd4: z= x>>1;
      default: z= 32'd0;
   endcase
end

endmodule
```

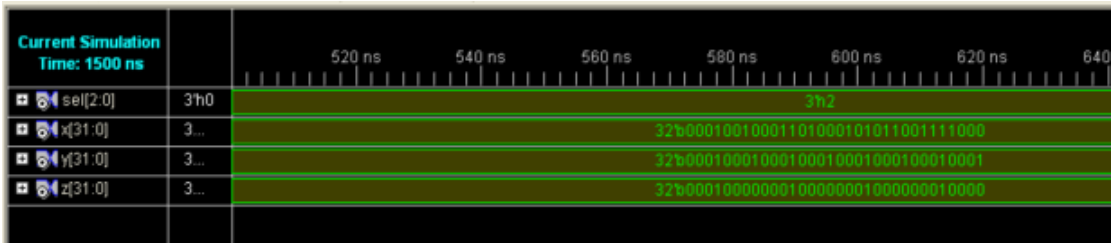
Add sel=0



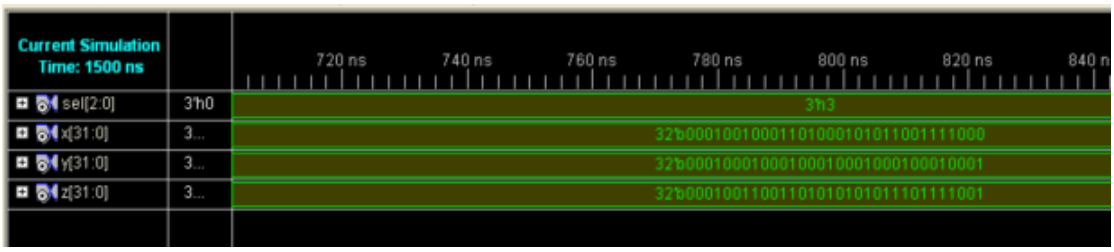
Sub sel=1



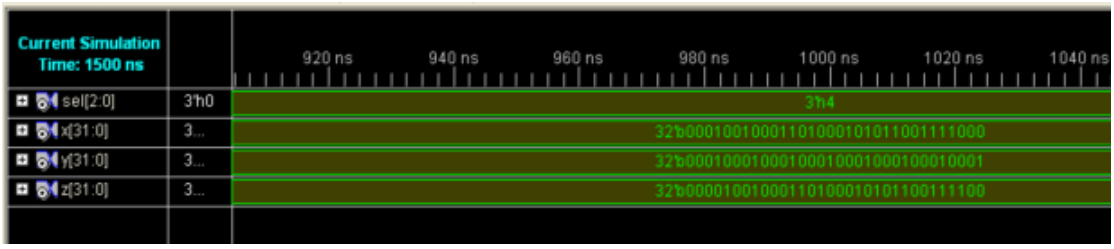
And sel=2



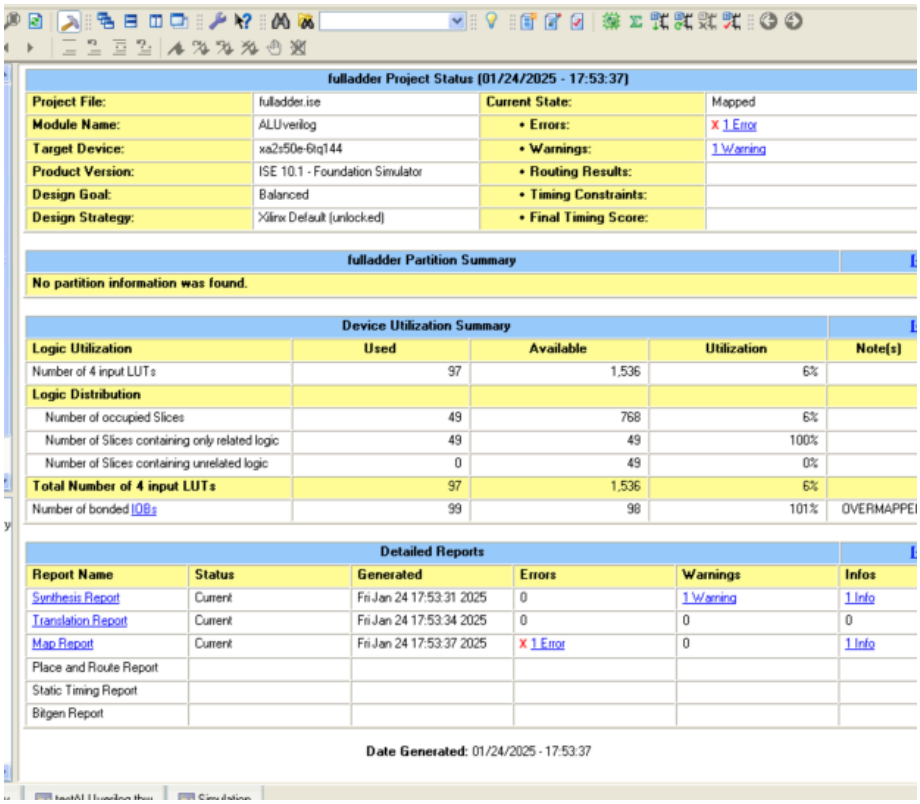
Or sel=3



Shift right sel=4



Log file of the mapper:



fulladder Project Status (01/24/2025 - 17:53:37)

Project File:	fulladder.ise	Current State:	Mapped
Module Name:	ALUverilog	• Errors:	x 1 Error
Target Device:	xa2s50e-6tq144	• Warnings:	1 Warning
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

fulladder Partition Summary

No partition information was found.

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	97	1,536	6%	
Logic Distribution				
Number of occupied Slices	49	768	6%	
Number of Slices containing only related logic	49	49	100%	
Number of Slices containing unrelated logic	0	49	0%	
Total Number of 4 input LUTs	97	1,536	6%	
Number of bonded IOBs	99	98	101%	OVERMAPPE

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	Fri Jan 24 17:53:31 2025	0	1 Warning	1 Info
Translation Report	Current	Fri Jan 24 17:53:34 2025	0	0	0
Map Report	Current	Fri Jan 24 17:53:37 2025	x 1 Error	0	1 Info
Place and Route Report					
Static Timing Report					
Bitgen Report					

Date Generated: 01/24/2025 - 17:53:37

Total LUTs = 97

Number of occupied Slices: 49

Brief comment on the number of gates as compared to the schematic version

1. Separate Paths for ADD and SUB

In a typical Verilog or RTL ALU, addition and subtraction can be implemented using one single 32-bit adder, combined with a 2's complement approach. This only requires one arithmetic circuit.

In a schematic-based design, I create a separate 32-bit adder for ADD and another 32-bit subtractor for SUB, the synthesis tool will see two distinct circuits and will not automatically merge them. Thus, more LUTs will be needed.

2. Multiple 5-to-1 MUX Instances (Multiplied by 32 Bits)

I use 32 instances of a 5-to-1 multiplexer to handle multiple ALU operations. Each 1-bit 5-to-1 MUX is constructed from multiple smaller logic gates or 2-input MUXes, so get a lot of replicated logic.

In contrast, when written in in Verilog, the synthesis tool can generate an efficient LUT-based multiplexer or share logic to reduce resource usage.