ELEC 3300

HOMEWORK 2

Please complete the following and submit your worksheet electronically before the deadline

Name : _	Mn-Rues,	1seng	Student number:	20472512	
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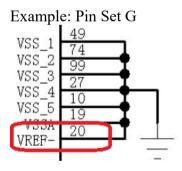
Question 1:

Part 1.a

With reference to your LAB2, based on your student ID, you have Pin Set from A to G Please fill in the following table based on your student ID. If the two digits are 00, then Pin number = 100 Pin Set G is filled as an example.

Pin Set	Actual Pin Number on STM32	Default Function of the pin on 100pin STM32F103VET6
A	22	V DODA
В	52	PB13
С	25	PAZ
D	92	J7MS-SWD10
Е	47	PBIO
F	04	PES
G	20	VREF-

Part 1.b With reference to the updated MINI V3 schematic dated 20210304, for Pin Set A, B and D, locate where do the pin connected. Cut and Paste the detailed schematic, highlight it and attached below.



Pin Set A	Pin Set B	Pin Set D	
SYS STI	LED_G	PB3 90 TD0 PB4 72 TMS PA14 76 TCK PA15 8 OSC32_IN PC14 9 OSC32_OUT	

Part 1.c With the Pin Set A, B and D you have, fill out the following table

	Pin Set A	Pin Set B	Pin Set D
Following the connection on the schematic, if I want to set that Pin to GPIO input, what mode I can program the pin into? Please circle all the possible options. If the pin cannot be programmed to	GPIO_PULLUP	GPIO_PULLUP) GPIO_PULLDOWN GPIO_NOPULL N/A	GPIO_PULLUP
input, please circle N/A		17/21	11/11

Question 2:

Part 2.b

Part 2.a

Assume a 3-minute stereo sound is being sampled at 48 kHz with 24-bit per channel, what would be the data size of the sound file in bytes? Show your calculation.

With the sampling rate at 48 kHz, what is the time between each sample? Show your calculation.

Part 2.c

With the sample time that you calculate in *Part 2.b* if we want to implement the sampling from the ADC of STM32 with different settings below. What is the total number of cycles needed? Hence, calculate the conversion time (Tconv) for the different settings

14x 1/ 2x106 = 7x106 = 7Ms

Total conversion time, Tcycle = sample cycles + 12.5 (conversion cycles)

	CLK (MHz) at the input at ADC Prescaler	ADC Prescaler (2/4/6/8)	ADCCLK (MHz) Max 14 MHz	ADC sample time register (cycles) (1.5 – 239.5)	Total conversion time, Tcycle Sample time (cycles)	Tconv (μsec)
Setting 1	12	6	Q	1.5	14	\ \
Setting 2	24	4	6	28.5	41	6.83
Setting 3	36	4	9	55.5	68	7.55
Setting 4	72	8	ġ	239.5	252	28

Part 2.d Can sampling in Part 2.b be achieved with the conversion time (Tconv) you calculated in Part 2.c for Setting 1 to 4? Please circle the correct answer and calculate the additional delay needed for different settings to achieve the goal.

	Can sampling be achieved	Additional Delay needed (μsec)
Setting 1	YE8/NO	20.833 - 7= 13.833
Setting 2	(YES) NO	20.833 - 6.83 = 14
Setting 3	YES/NO	70.833 - 7.55 = 13.278
Setting 4	YES/NO	NIA