

1	A	B	C	D
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	2			2
	3			3
4	<div><div>Note Table</div><div><div>3</div><div>Found error in the Arduino power connector: +3.3V and +5V pins were swapped on the symbol. Corrected the symbol by swapping the pins for these two power pins, but also renamed the second +5V pin to IOREF as generally shown on Arduino schematics. Created separate net for this signal from the power connector to the 10–pin I/O connector. This allows the IOREF to be independently defined by the Arudino master. The jumper on the Chameleon allows the I/O voltage to be set as either the IOREF voltage or +3.3V. Applied corrections to the PCB file as well.</div></div><div><div>2</div><div>Found that the 32–pin TSOP I SRAM shown on the schematic and BOM is incorrect: operating voltage is +5V instead of the required +3.3V. Corrected the schematic part number for the ISSI SRAM and added an alternate part from Cypress.</div></div><div><div>1</div><div>Changed default part number for the Arduino connectors to use the version with longer pin lengths. Location and height of the Arduino UNO USB Type B connector touches the pins of the serial port connectors if normal stacking connector pin lengths are used. The standard stacking connector part numbers still shown on the schematic</div></div></div>			
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Revision Note Table  
Revision A – Notes 1 through 3

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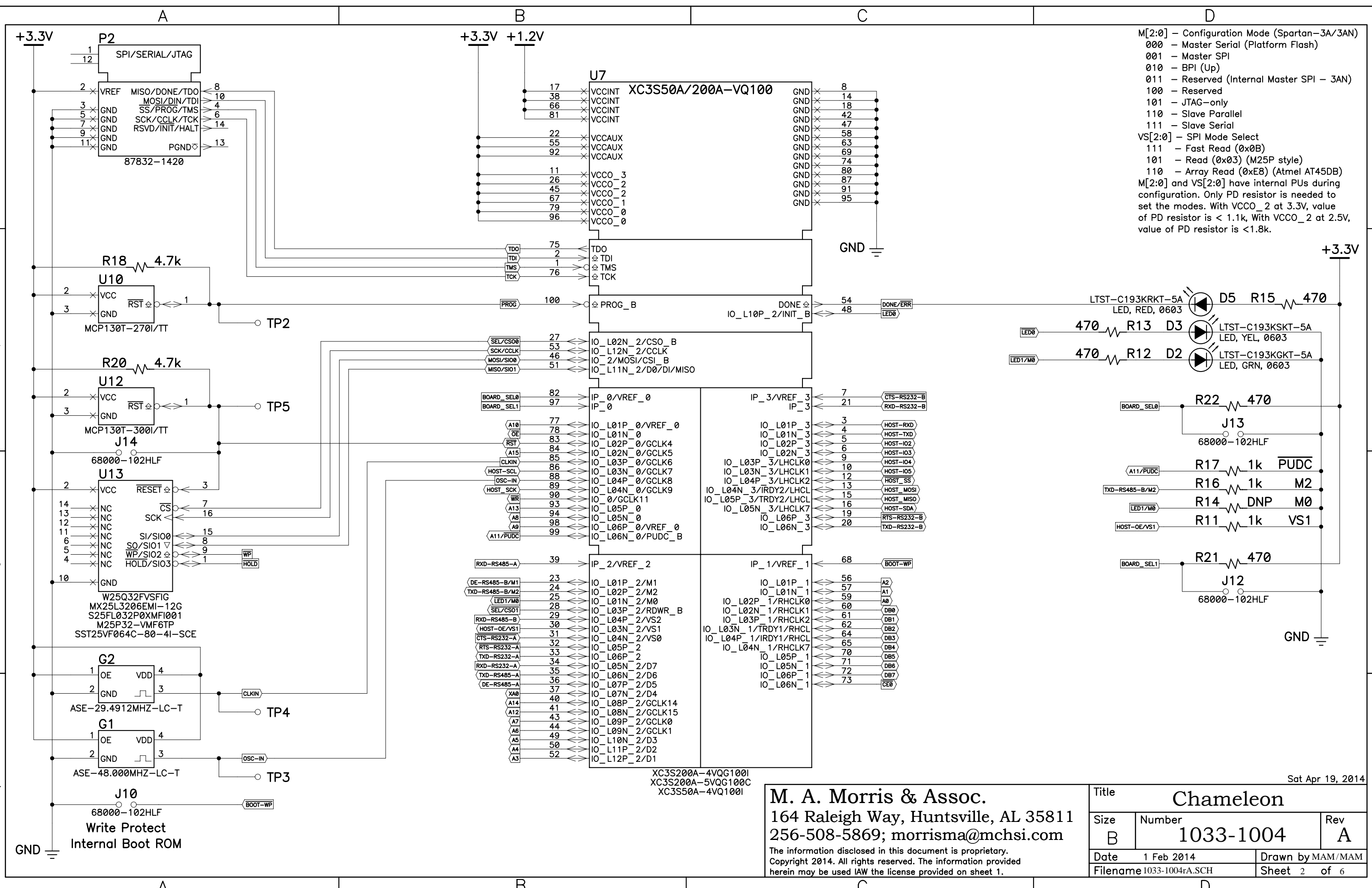
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Title Chameleon		
Size B	Number 1033-1004	Rev A
Date 1 Feb 2014	Drawn by MAM/MAM	
Filename 1033-1004rA.SCH	Sheet 1	of 6

Sat Apr 19, 2014



M[2:0] – Configuration Mode (Spartan–3A/3AN)  
000 – Master Serial (Platform Flash)  
001 – Master SPI  
010 – BPI (Up)  
011 – Reserved (Internal Master SPI – 3AN)  
100 – Reserved  
101 – JTAG–only  
110 – Slave Parallel  
111 – Slave Serial  
VS[2:0] – SPI Mode Select  
111 – Fast Read (0x0B)  
101 – Read (0x03) (M25P style)  
110 – Array Read (0xE8) (Atmel AT45DB)  
M[2:0] and VS[2:0] have internal PUs during configuration. Only PD resistor is needed to set the modes. With VCCO\_2 at 3.3V, value of PD resistor is < 1.1k, With VCCO\_2 at 2.5V, value of PD resistor is <1.8k.

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Size <b>B</b>	Number <b>1033-1004</b>	Rev <b>A</b>
Date 1 Feb 2014	Drawn by MAM/MAM	
Filename 1033-1004rA.SCH	Sheet 2	of 6

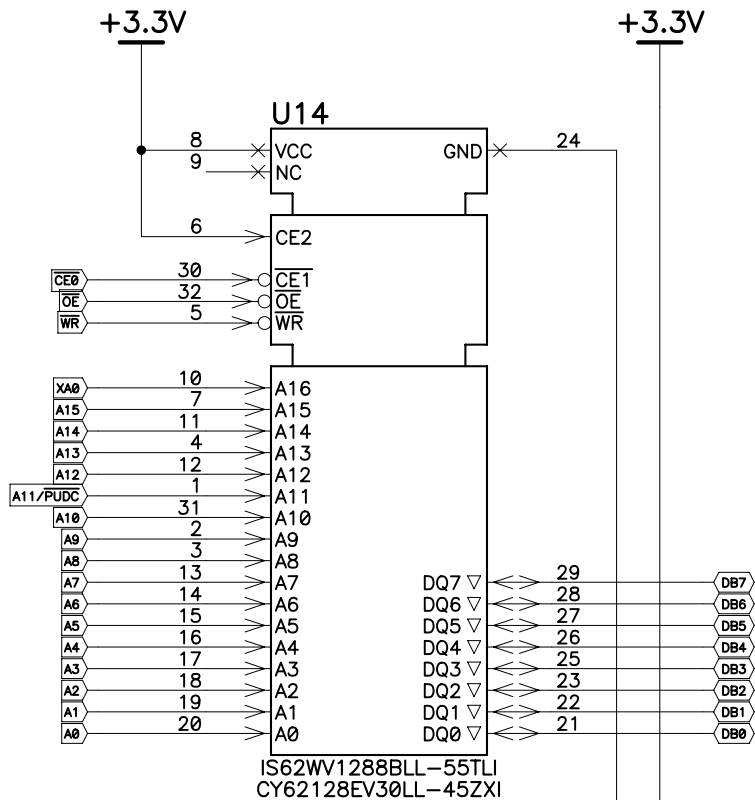
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A

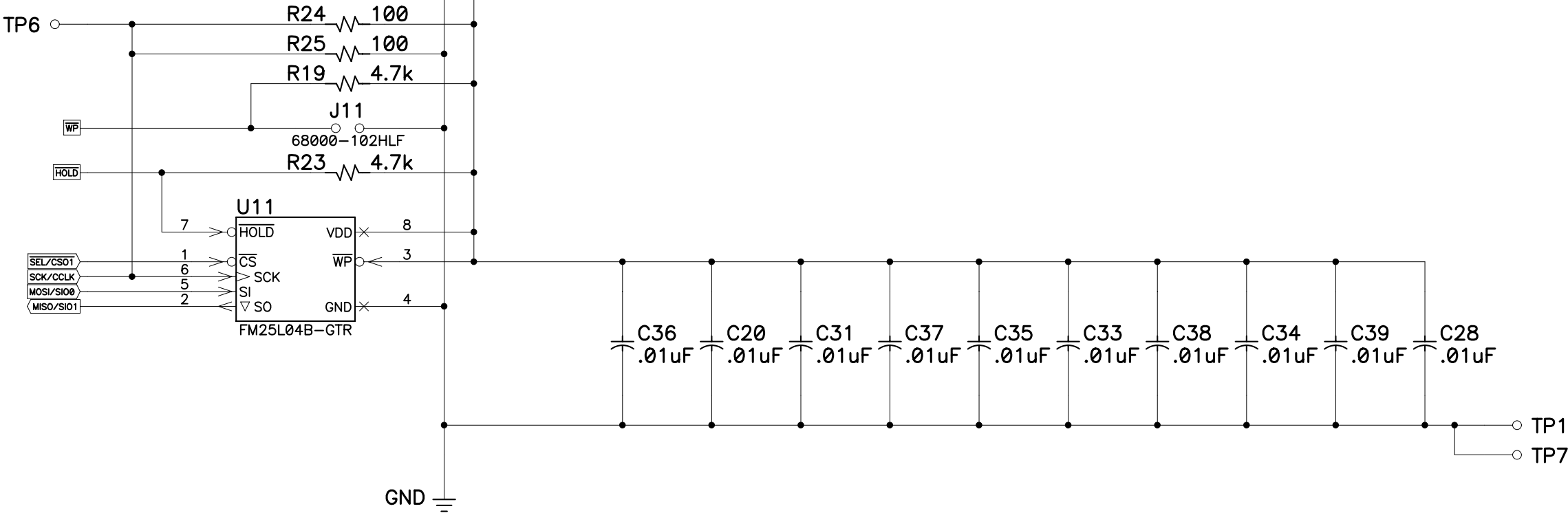
B

C

D



Terminate at end of net.  
Route from FPGA to last  
device in SCK/CCLK chain  
without stubs.



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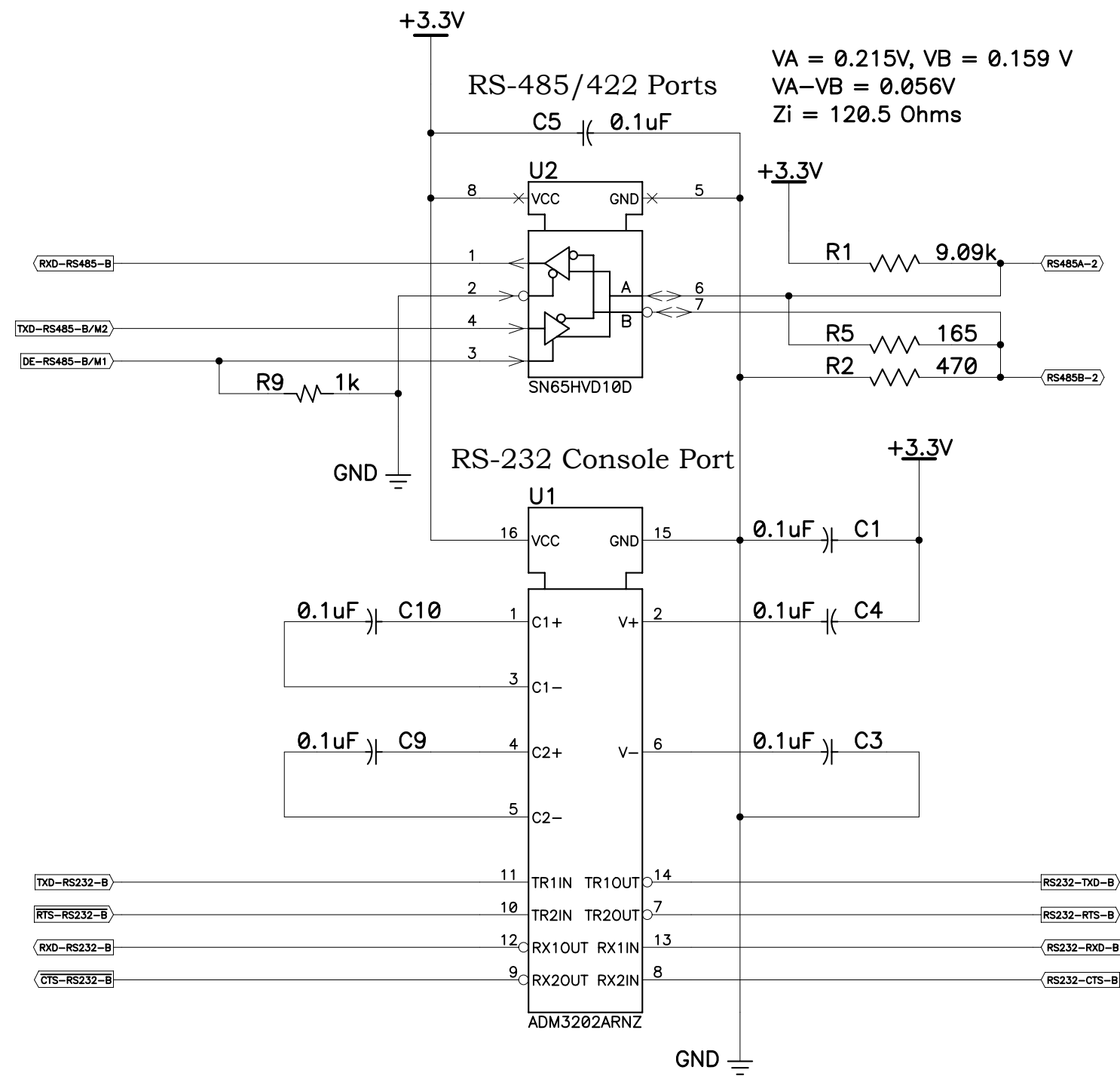
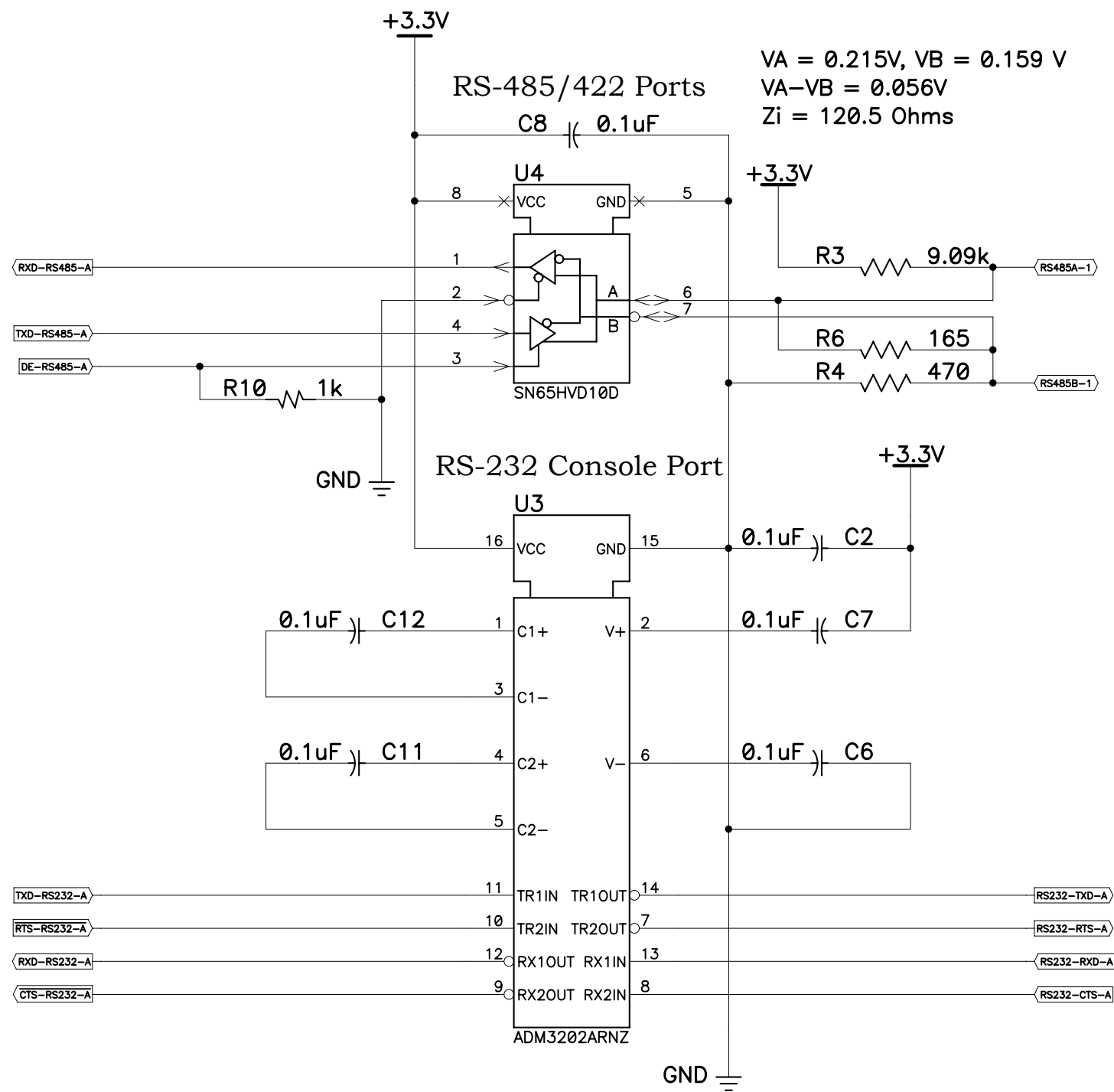
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Size		Number		Rev	
B		1033-1004		A	
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			Drawn by MAM/MAM		
Filename			1033-1004rA.SCH		
			Sheet 3 of 6		

A

B

C

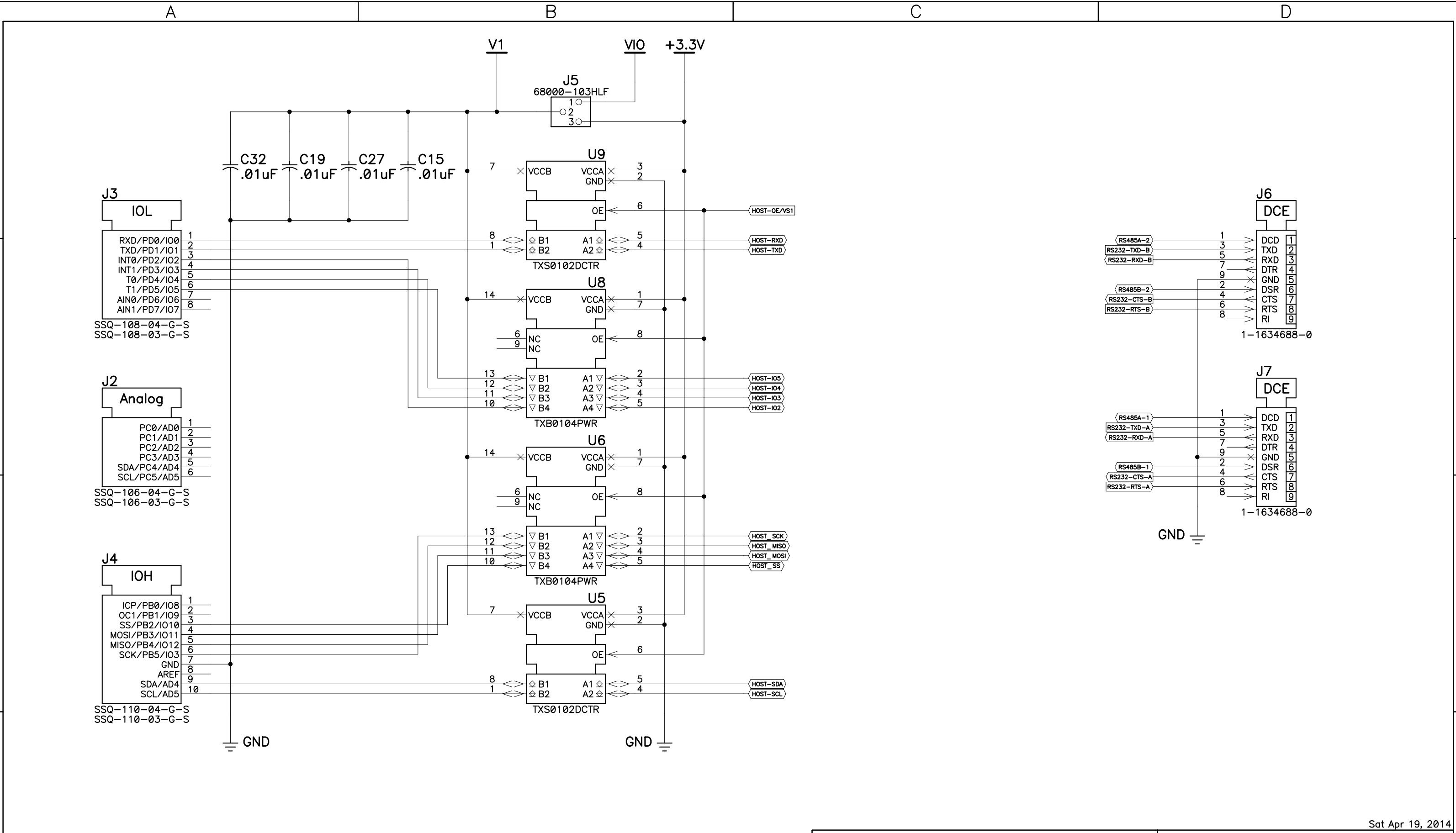
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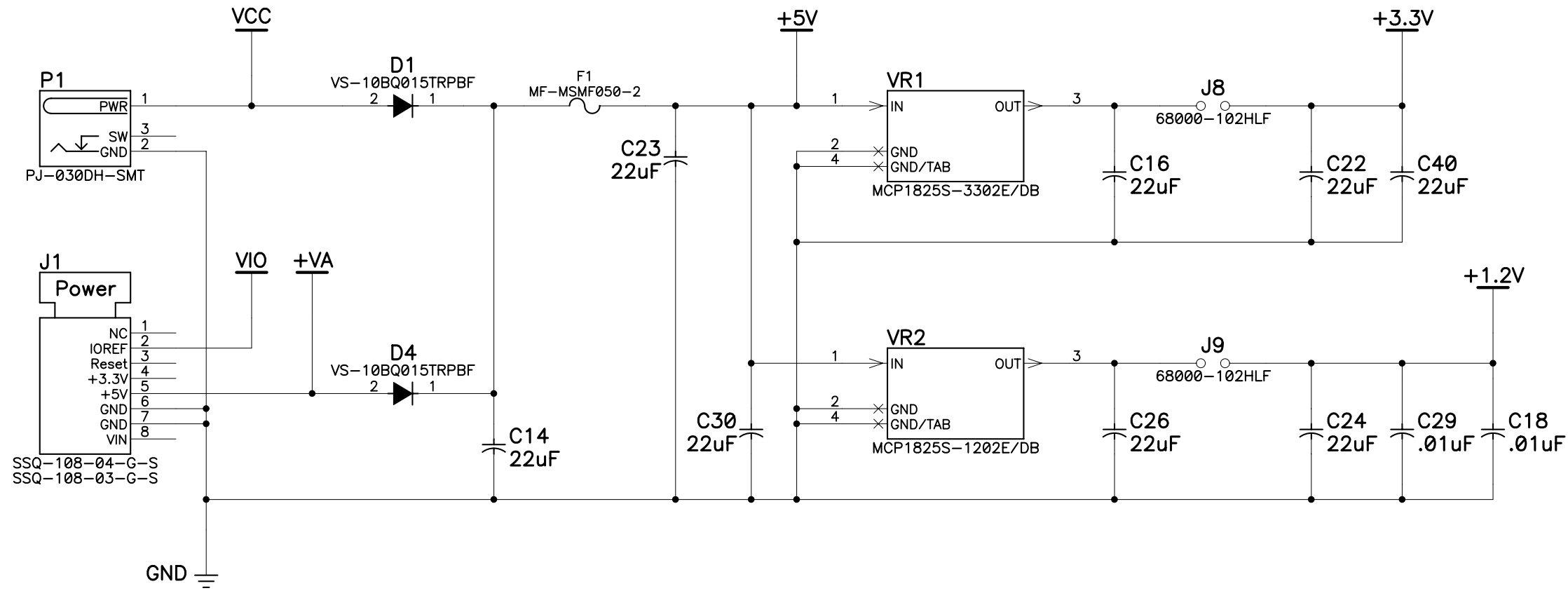


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Filename 1033-1004rA.SCH	Sheet 4	of 6

Sat Apr 19, 2014





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Filename 1033-1004rA.SCH	Sheet 6	of 6