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Sat Mar 29, 2014

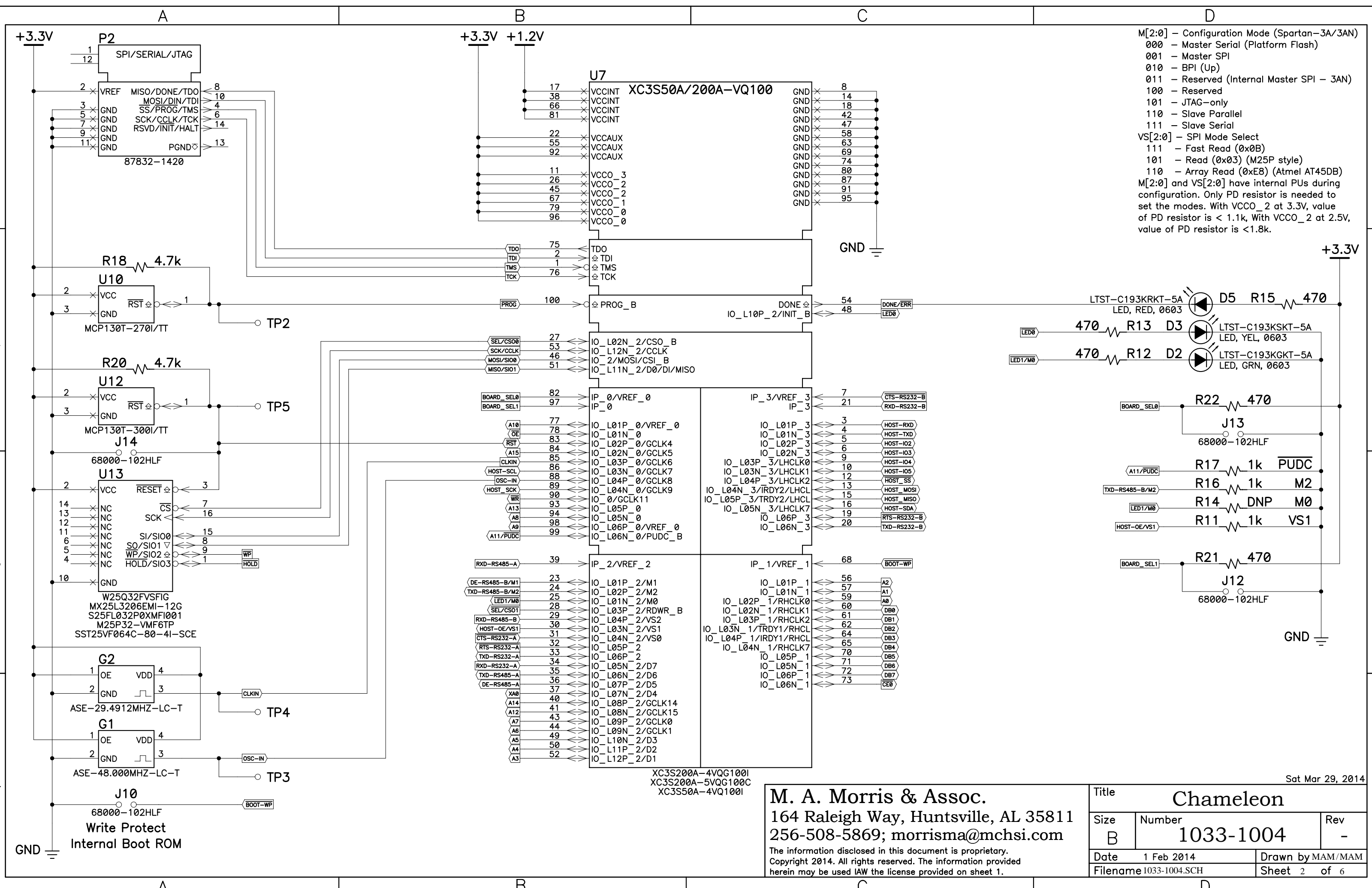
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Title	Chameleon
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Size B	Number 1033-1004	Rev -
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Date	1 Feb 2014	Drawn by	MAM/MAM
Filename	1033-1004.SCH	Sheet	1 of 6



M[2:0] – Configuration Mode (Spartan–3A/3AN)
000 – Master Serial (Platform Flash)
001 – Master SPI
010 – BPI (Up)
011 – Reserved (Internal Master SPI – 3AN)
100 – Reserved
101 – JTAG–only
110 – Slave Parallel
111 – Slave Serial
VS[2:0] – SPI Mode Select
111 – Fast Read (0x0B)
101 – Read (0x03) (M25P style)
110 – Array Read (0xE8) (Atmel AT45DB)
M[2:0] and VS[2:0] have internal PUs during configuration. Only PD resistor is needed to set the modes. With VCCO_2 at 3.3V, value of PD resistor is < 1.1k, With VCCO_2 at 2.5V, value of PD resistor is <1.8k.

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Title Chameleon		
Size B	Number 1033-1004	Rev -
Date 1 Feb 2014	Drawn by MAM/MAM	
Filename 1033-1004.SCH	Sheet 2	of 6

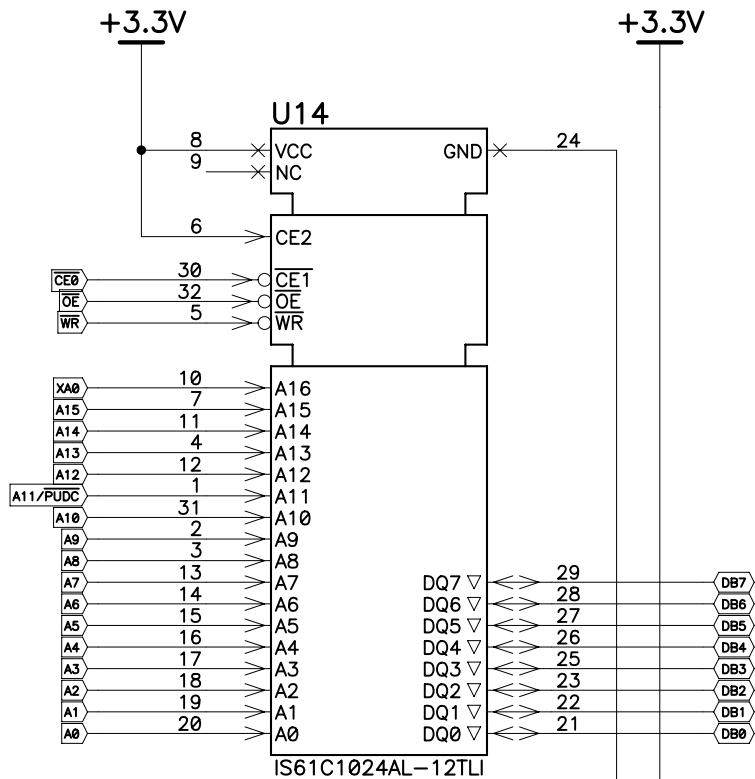
Sat Mar 29, 2014

A

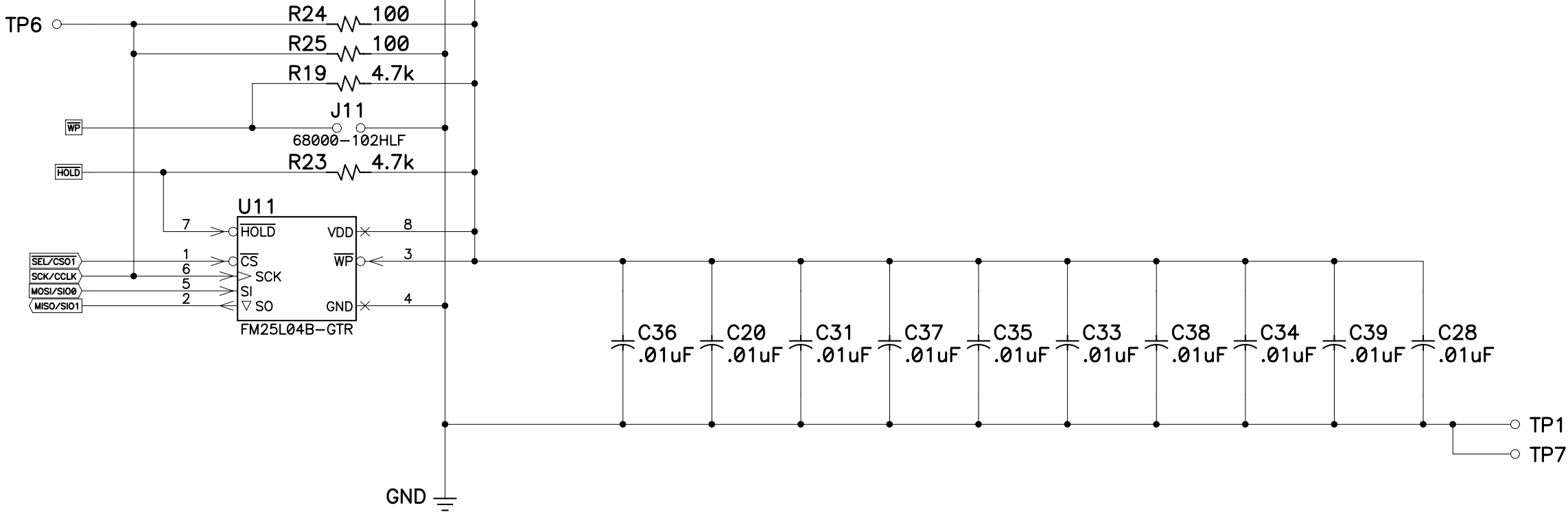
B

C

D



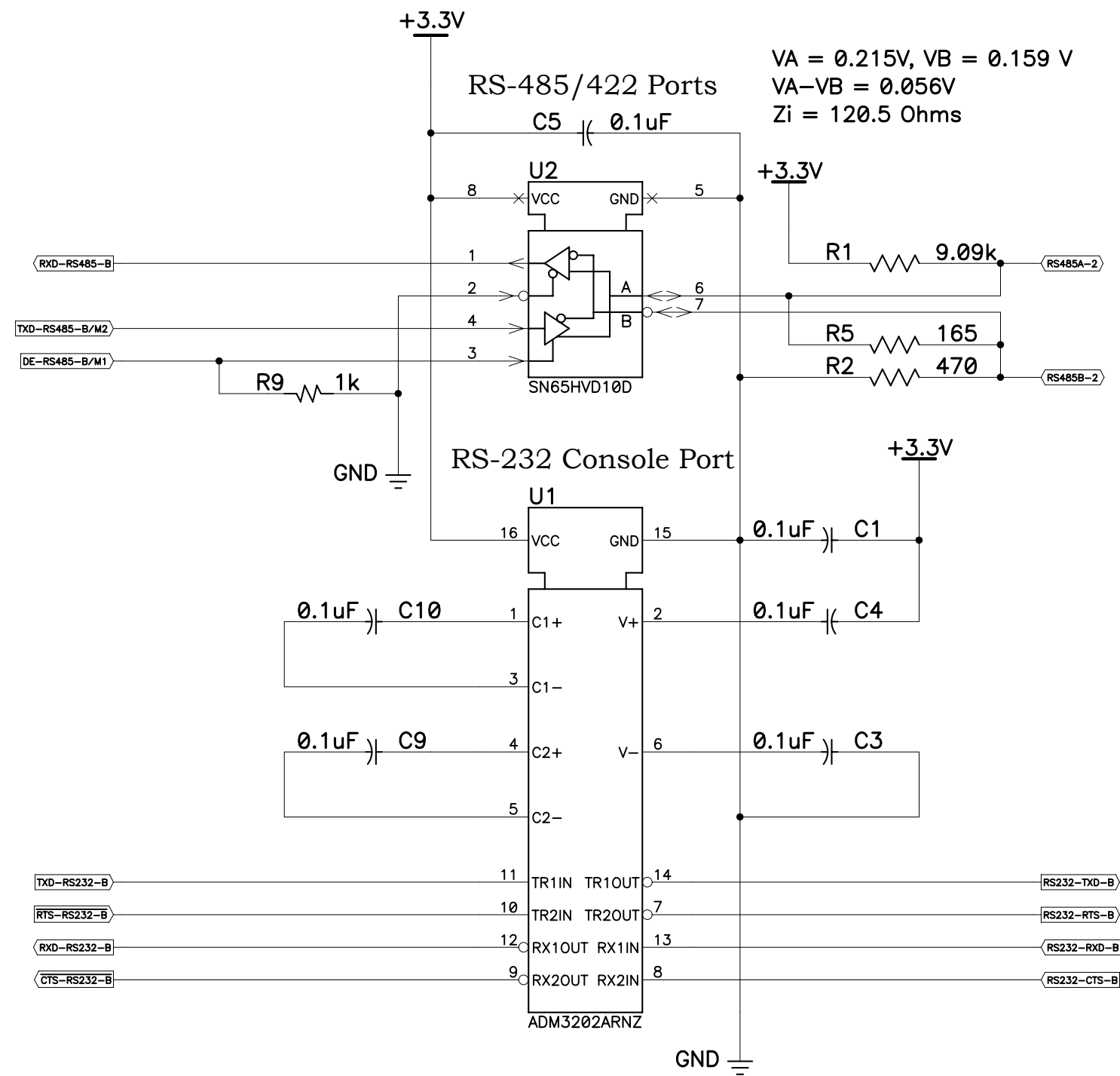
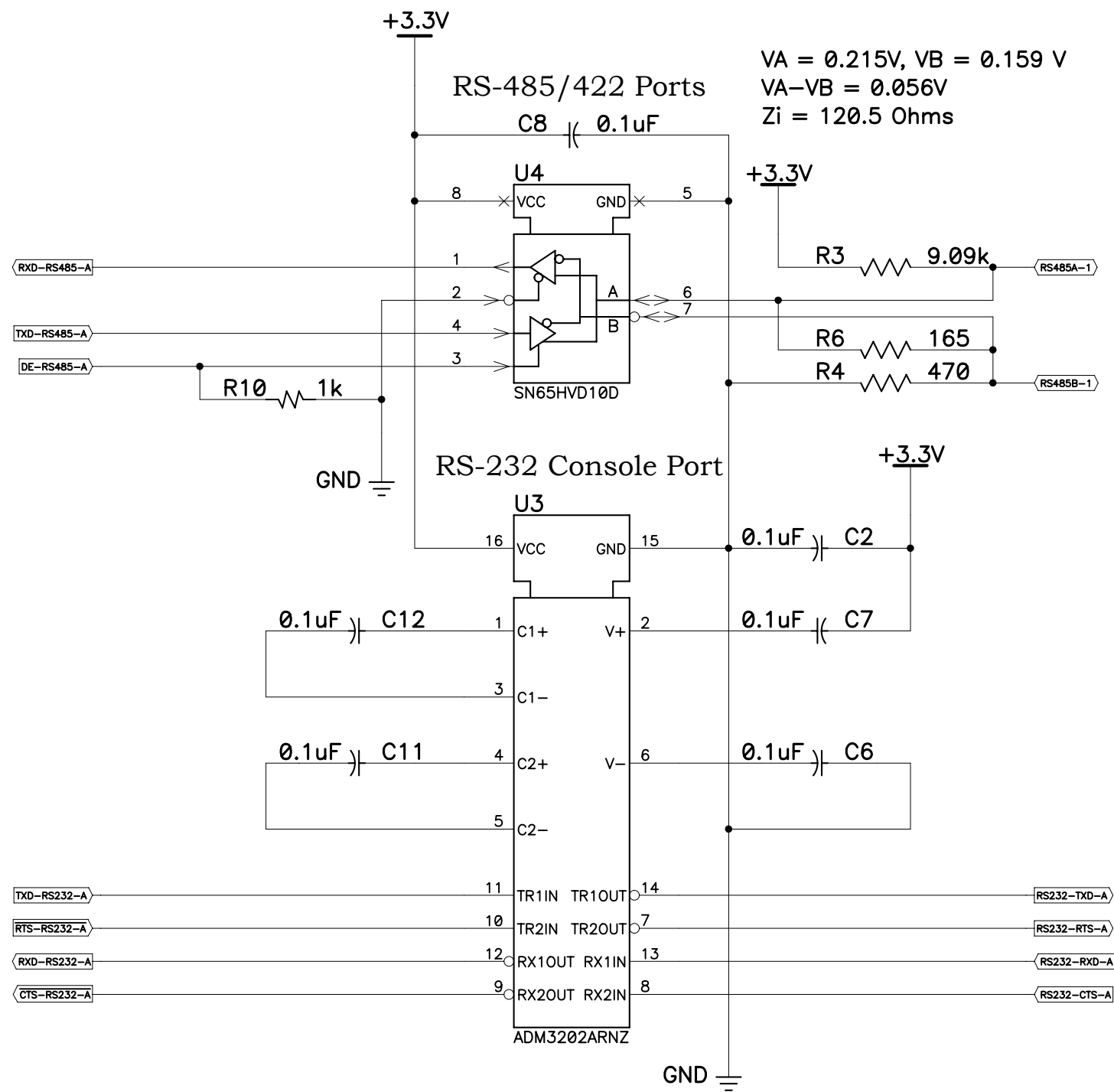
Terminate at end of net.
Route from FPGA to last
device in SCK/CCLK chain
without stubs.



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