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INCREMENTER AND DECREMENTER OF AN N-BIT INPUT, BY A VALUE 'M' CIRCUIT DESIGN AND ANALYSIS FOR VARIOUS PARAMETERS

Mr. Manjunath K. M[1], Dr. K. N. Muralidhara[2], Dr. H. V. Ravish Aradhya [3]

[1] Assistant Professor,Dept. of ECE, RVITM, Bengaluru, Karnataka, India.

[2] Professor,Dept. of ECE,BGSIT, Mandya, Karnataka, India.

[3] Professor,Dept. of ECE, RVCE, Bengaluru, Karnataka, India.

[1]manjunathkm.rvitm@rvei.edu.in, [2]knm08@rediffmail.com, [3]ravisharadhya@rvce.edu.in

ABSTRACT: Incrementer and Decrementer for an N-bit operation is as usual as adding or subtracting by a value 'M' to the given N-bit Input respectively. For Example, if for a given N-bit input, added or subtracted by M=1 value to the given N-bit Input, it is called as Increment or Decrement by One Operation for a N-bit Input respectively and If added or subtracted by M=2 value to the given N-bit Input, then it is called as an Increment or Decrement by Two operation for a N-bit Input respectively. Here $M=2^X$ and is applicable for all 'X' Positive Integers varying from Zero to Infinity. (i.e. M=1, 2, 4, 8 and so on). Note that here if 'M' is 2^X or other than the 2^X values, then the logic can be slightly varied to arrive for General Expression as per the user Requirements. In this Paper, the work carried out to generalize the Minimal Possible Area Design Equations, for the N-bit Incrementer or Decrementer by a value 'M' Operation Circuit Design and its implementation in Cadence Platform for various parameter analysis is summarized. This helps for many VLSI Designs like ALU Design which involves Increment or Decrement Operation.

KEYWORDS: Binary-Incrementer, Binary-Decrementer, N-bit-Incrementer, N-bit-Decrementer, Increment/Decrement Operation.

I. INTRODUCTION

The final complex circuit design involves many components level circuits like adder, multiplier, Incrementer, Decrementer, complement and so on. Also, the final complex circuit design depends mainly on the fundamental optimized component level circuits. If the component level circuits are chosen to the best optimized way, then the final complex circuit will be optimized and in turn results with better area and power efficiency.

For performing the N-bit Incrementer and Decrementer operation, the operating principle of an N-bit Incrementer and Decrementer circuit should be understood thoroughly. In turn, truth table, that describes the operating principle is important and hence to start the circuit design and analyses, it is important to start with truth table. Later, input-output logical expression for each bit output is analyzed from truth table followed by the circuit design, implementation and simulation for functionality check.

For the N-bit Incrementer and Decrementer operation, the input-output logical expression for each bit output can be found using the K-Map technique. But this K-Map technique is flexible and easy for N-bit Incrementer and Decrementer operation, where N=1,2,3 and 4. If 'N' is greater than 4, then the technique becomes too complex for finding the input-output logical expression for each bit output. Hence the other way of manipulating the input-output logical expression for each bit output for the N-bit Incrementer and Decrementer operation is done by Generalizing the input-output Relation. The same is explained in this paper.

A new circuit using a decision module that implements the key operation of the Incrementer / Decrementer circuit showed better performance in terms of Power-Delay product [1]. The design of Decrement / Increment that is highly parallel and almost independent of the word size shown better results in terms of speed of operation [2]. The cascading architecture for building larger size Incrementer-cum-Decrementer based on the LSZB (Least Significant Zero Bit) Principle [3]. The 64-bit Incrementer / Decrementer can be designed well above 100MHZ in a 0.6-mCMOS process [4]. To obtain more prominent results, the sub-module D-Flipflop is implemented using the Transmission Gate CMOS methodology [5]. An improvement to the decision block of the existing Incrementer / Decrementer architectures using a new reconfigurable circuit, which can be configured to perform Increment, Decrement and other operations showed better performance [6]. The MUX-based Incrementer / Decrementer is more efficient in terms of speed and hardware complexity [7]. A high-Speed Programmable Incrementing / Decrementing Accumulator can be used inside any High-Speed High-Resolution Calibration loops [8]. An Incrementer / Decrementer is a common building block in many digital systems

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like address generation unit, which are used in Microcontrollers and Microprocessors [9]. Hence the Incrementer and Decrementer operations are very important and need for VLSI Component designs.

Incrementer Operation

Incrementer operation is adding by a value M to the given N-bit Input. For Example, If added by M=1 value to the given N-bit Input, it is called as Incrementer by One Operation for a N-bit Input and If added by M=2 value to the given N-bit Input, then it is called as an Incrementer by Two operation for a N-bit Input.

Here $M=2^X$ and is applicable for all 'X' Positive Integers varying from Zero to Infinity. (i.e. M=1, 2, 4, 8 and so on). Note that here if 'M' is other than the 2^X values, then the logic can be slightly varied to arrive for General Expression as per the user Requirements.

In this second part Paper, the work carried out to generalize the Minimal Possible Area Design Equations, for the N-bit Incrementer by a value M Operation Circuit Design and implementation of the same is done in Cadence Platform for various parameter analyses.

Initially to start the same, Truth Table and Exhaustive Analysis is written by considering the 1-bit, 2-bit, 3-bit and 4-bit Incrementer by M=1 value Circuit Design and further enhancing the same to arrive with the Generalized Expression for the N-bit Incrementer by M=1 value Operation Circuit Design.

A. 1-bit Incrementer by M=1

The 1-bit Incrementer by M=1 value Block Design is as shown in the "Fig. 1" below. It is used to add the given 1-bit Input by a value M=1.

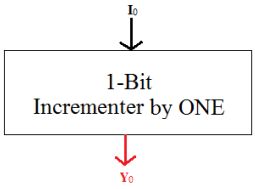

FIG. 1. 1-BIT INCREMENTER BY M=1 BLOCK

TABLE I. TRUTH TABLE FOR 1-BIT INCREMENTER BY M=1 VALUE

1-bit Input	1-bit Incrementer by ONE Output
I_0	Y_0
0	1
1	0

Initially, By K-Map, Realizing the Logical Expressions for 1-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 1-bit Input 'I' and 1-bit Input value M=1(i.e. 1 in binary) and considering Truth Table as shown in TABLE I, we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (1)}$$

B. 2-bit Incrementer by M=1

The 2-bit Incrementer by M=1 value Block Design is as shown in the "Fig. 2" below. It is used to add the given 2-bit Input by a value M=1.

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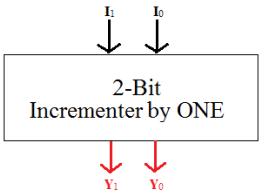

FIG. 2. 2-BIT INCREMENTER BY M=1 BLOCK

TABLE II (a). TRUTH TABLE FOR 2-BIT INCREMENTER BY M=1 VALUE

2-bit Input		2-bit Incrementer by ONE Output	
I_1	I_0	Y_1	Y_0
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

TABLE II (b). K-MAP IMPLEMENTATION FOR 2-BIT INCREMENTER OUTPUT Y_0 BY M=1 VALUE

Y_0	0 ($\overline{I_0}$)	1 (I_0)
0 ($\overline{I_1}$)	1	0
1 (I_1)	1	0

TABLE II (c). K-MAP IMPLEMENTATION FOR 2-BIT INCREMENTER OUTPUT Y_1 BY M=1 VALUE

Y_1	0 ($\overline{I_0}$)	1 (I_0)
0 ($\overline{I_1}$)	0	1
1 (I_1)	1	0

Initially, By K-Map, Realizing the Logical Expressions for 2-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 2-bit Input 'I' and 2-bit Input value M=1(i.e. 01 in binary) and considering Truth Table as shown in TABLE II (a), TABLE II (b) and TABLE II (c) we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (2)}$$

$$Y_1 = \overline{I_1}\ I_0 + I_1\ \overline{I_0} = I_1 \oplus I_0 \qquad \text{Eqn (3)}$$

C. 3-bit Incrementer by M=1

The 3-bit Incrementer by M=1 value Block Design is as shown in the "Fig. 3" below. It is used to add the given 3-bit Input by a value M=1.

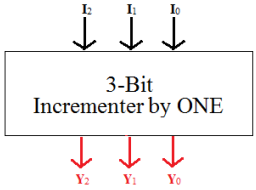

FIG. 3. 3-BIT INCREMENTER BY M=1 BLOCK

TABLE III (a). TRUTH TABLE FOR 3-BIT INCREMENTER BY M=1 VALUE

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3-bit Input			3-bit Incrementer by ONE Output		
I_2	I_1	I_0	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	0	0	0	0

TABLE III (b). K-MAP IMPLEMENTATION FOR 3-BIT INCREMENTER OUTPUT Y_0 BY M=1 VALUE

Y_0	00 ($\bar{I_1}$ $\bar{I_0}$)	01 ($\bar{I_1}$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I_0}$)
0 ($\bar{I_2}$)	1	0	0	1
1 (I_2)	1	0	0	1

TABLE III (c). K-MAP IMPLEMENTATION FOR 3-BIT INCREMENTER OUTPUT Y_1 BY M=1 VALUE

Y_1	00 ($\bar{I_1}$ $\bar{I_0}$)	01 ($\bar{I_1}$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I_0}$)
0 ($\bar{I_2}$)	0	1	0	1
1 (I_2)	0	1	0	1

TABLE III (d). K-MAP IMPLEMENTATION FOR 3-BIT INCREMENTER OUTPUT Y_2 BY M=1 VALUE

Y_2	00 ($\bar{I_1}$ $\bar{I_0}$)	01 ($\bar{I_1}$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I_0}$)
0 ($\bar{I_2}$)	0	0	1	0
1 (I_2)	1	1	0	1

Initially, By K-Map, Realizing the Logical Expressions for 3-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 3-bit Input 'I' and 3-bit Input value M=1(i.e. 001 in binary) and considering Truth Table as shown in TABLE III (a), TABLE III (b), TABLE III (c) and TABLE III (d), we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (4)}$$

$$Y_1 = \overline{I_1}\ I_0 + I_1\ \overline{I_0} = I_1 \oplus I_0 \qquad \text{Eqn (5)}$$

$$Y_2 = I_2\ \overline{I_1} + \overline{I_2}\ I_1 I_0 + I_2 I_1\ \overline{I_0} = I_2 \oplus I_1 I_0 \qquad \text{Eqn (6)}$$

D. 4-bit Incrementer by M=1

The 4-bit Incrementer by M=1 value Block Design is as shown in the "Fig. 4" below. It is used to add the given 4-bit Input by a value M=1.

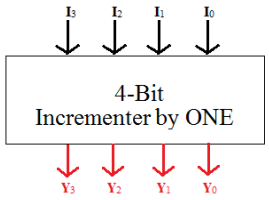

FIG. 4. 4-BIT INCREMENTER BY M=1 BLOCK

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TABLE IV (a). TRUTH TABLE FOR 4-BIT INCREMENTER BY M=1 VALUE

4-bit Input				4-bit Incrementer by ONE Output			
I_3	I_2	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

TABLE IV (b). K-MAP IMPLEMENTATION FOR 4-BIT INCREMENTER OUTPUT Y_0 BY M=1 VALUE

Y_0	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	1	0	0	1
01 ($\bar{I}_3$ I_2)	1	0	0	1
11 (I_3 I_2)	1	0	0	1
10 (I_3 $\bar{I}_2$)	1	0	0	1

TABLE IV (c). K-MAP IMPLEMENTATION FOR 4-BIT INCREMENTER OUTPUT Y_1 BY M=1 VALUE

Y_1	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	0	1	0	1
01 ($\bar{I}_3$ I_2)	0	1	0	1
11 (I_3 I_2)	0	1	0	1
10 (I_3 $\bar{I}_2$)	0	1	0	1

TABLE IV (d). K-MAP IMPLEMENTATION FOR 4-BIT INCREMENTER OUTPUT Y_2 BY M=1 VALUE

Y_2	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	0	0	1	0
01 ($\bar{I}_3$ I_2)	1	1	0	1
11 (I_3 I_2)	1	1	0	1
10 (I_3 $\bar{I}_2$)	0	0	1	0

TABLE IV (e). K-MAP IMPLEMENTATION FOR 4-BIT INCREMENTER OUTPUT Y_3 BY M=1 VALUE

Y_3	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	0	0	0	0
01 ($\bar{I}_3$ I_2)	0	0	1	0

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11 (I_3 I_2)	1	1	0	1
10 (I_3 $\overline{I_2}$)	1	1	1	1

Initially, By K-Map, Realizing the Logical Expressions for 4-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 4-bit Input 'I' and 4-bit Input value M=1(i.e. 0001 in binary) and considering Truth Table, as shown in TABLE IV (a), TABLE IV (b), TABLE IV (c), TABLE IV (d) and TABLE IV (e), we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (7)}$$

$$Y_1 = \overline{I_1}\ I_0 + I_1\ \overline{I_0} = I_1 \oplus I_0 \qquad \text{Eqn (8)}$$

$$Y_2 = I_2\ \overline{I_1} + \overline{I_2}\ I_1 I_0 + I_2 I_1\ \overline{I_0} = I_2 \oplus I_1 I_0 \qquad \text{Eqn (9)}$$

$$Y_3 = I_3\ \overline{I_1} + I_3\ \overline{I_2} + I_3 I_1\ \overline{I_0} + \overline{I_3}\ I_2 I_1 I_0 = I_3 \oplus I_2 I_1 I_0 \qquad \text{Eqn (10)}$$

E. N-bit Incrementer by M=1

The N-bit Incrementer by M=1 value Block Design is as shown in the "Fig. 5" below. It is used to add the given N-bit Input by a value M=1.

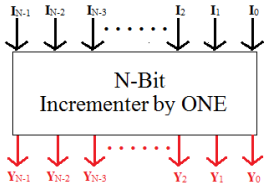

FIG. 5. N-BIT INCREMENTER BY M=1 BLOCK

TABLE V. TRUTH TABLE FOR N-BIT INCREMENTER BY M=1 VALUE

N-bit Input					**N-bit Incrementer by ONE Output**				
I_{N-1}	I_{N-2}	...	I_1	I_0	Y_{N-1}	Y_{N-2}	...	Y_1	Y_0
0	0		0	0	0	0		0	1
0	0	.	0	1	0	0	.	1	0
0	0	.	1	0	0	0	.	1	1
0	0	.	1	1	0	0	.	0	0
0	0	.	0	0	0	0	.	0	1
0	0		0	1	0	0		1	0
.		.		.	.		.		.
.		.		.	.		.		.
.		.		.	.		.		.
1	1		1	0	1	1		1	1
1	1	.	1	1	1	1	.	0	0
1	1	.	0	0	1	1	.	0	1
1	1	.	0	1	1	1	.	1	0
1	1	.	1	0	1	1	.	1	1
1	1		1	1	0	0		0	0

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Initially, By K-Map, Realizing the Logical Expressions for N-bit Input, it is found to be very complex process if N > 4, and the Later stage, Realizing the Logical Expressions by the Concept of Full Adder Addition between N-bit Input 'I' and N-bit Input value M=1(i.e. 000…..001 in binary) and considering Truth Table as shown in TABLE V, we have,

$$Y_P = \begin{cases} \overline{I_0}, & P = 0 \\ I_P \oplus [I_{(P-1)} I_{(P-2)} \ldots\ldots I_1 I_0], & 0 < P < N \end{cases} \qquad \text{Eqn (11)}$$

II. DECREMENTER OPERATION

Decrementer operation is Subtracting by a value M to the given N-bit Input. For Example, If Subtracted by M=1 value to the given N-bit Input, it is called as Decrementer by One Operation for a N-bit Input and If Subtracted by M=2 value to the given N-bit Input, then it is called as an Decrementer by Two operation for a N-bit Input.

Here $M=2^X$ and is applicable for all 'X' Positive Integers varying from Zero to Infinity. (i.e. M=1, 2, 4, 8 and so on). Note that here if 'M' is other than the 2^X values, then the logic can be slightly varied to arrive for General Expression as per the user Requirements.

In this third part of the Paper, the work carried out to generalize the Minimal Possible Area Design Equations, for the N-bit Decrementer by a value M Operation Circuit Design and implement the same in Cadence Platform for various parameter analyses.

Initially to start the same, Truth Table and Exhaustive Analysis is written by considering the 1-bit, 2-bit, 3-bit and 4-bit Decrementer by M=1 value Circuit Design and further enhancing the same to arrive with the Generalized Expression for the N-bit Decrementer by M=1 value Operation Circuit Design.

1-bit Decrementer by M=1

The 1-bit Decrementer by M=1 value Block Design is as shown in the "Fig. 6" below. It is used to subtract the given 1-bit Input by a value M=1.

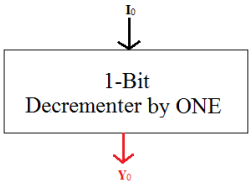

FIG. 6. 1-BIT DECREMENTER BY M=1 BLOCK

TABLE VI. TRUTH TABLE FOR 1-BIT DECREMENTER BY M=1 VALUE

1-bit Input	1-bit Decrementer by ONE Output
I_0	Y_0
0	1
1	0

Initially, By K-Map, Realizing the Logical Expressions for 1-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 1-bit Input 'I' and 1-bit Input value M=1 (i.e. 1 in binary) and considering Truth Table, as shown in TABLE VI, we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (12)}$$

A. 2-bit Decrementer by M=1

The 2-bit Decrementer by M=1 value Block Design is as shown in the "Fig. 7" below. It is used to subtract the given 2-bit Input by a value M=1.

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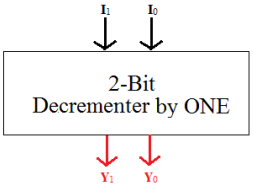

FIG. 7. 2-BIT DECREMENTER BY M=1 BLOCK

TABLE VII (a). TRUTH TABLE FOR 2-BIT DECREMENTER BY M=1 VALUE

2-bit Input		2-bit Decrementer by ONE Output	
I_1	I_0	Y_1	Y_0
0	0	1	1
0	1	0	0
1	0	0	1
1	1	1	0

TABLE VII (b). K-MAP IMPLEMENTATION FOR 2-BIT DECREMENTER OUTPUT Y_0 BY M=1 VALUE

Y_0	0 ($\bar{I}_0$)	1 (I_0)
0 ($\bar{I}_1$)	1	0
1 (I_1)	1	0

TABLE VII (c). K-MAP IMPLEMENTATION FOR 2-BIT DECREMENTER OUTPUT Y_1 BY M=1 VALUE

Y_1	0 ($\bar{I}_0$)	1 (I_0)
0 ($\bar{I}_1$)	1	0
1 (I_1)	0	1

Initially, By K-Map, Realizing the Logical Expressions for 2-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 2-bit Input 'I' and 2-bit Input value M=3 (i.e. 11 in binary) and considering Truth Table, as shown in TABLE VII (a), TABLE VII (b) and TABLE VII (c), we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (12)}$$

$$Y_1 = \overline{I_1}\ \overline{I_0} + I_1 I_0 = \overline{I_1 \oplus I_0} \qquad \text{Eqn (13)}$$

B. 3-bit Decrementer by M=1

The 3-bit Decrementer by M=1 value Block Design is as shown in the "Fig. 8" below. It is used to subtract the given 3-bit Input by a value M=1.

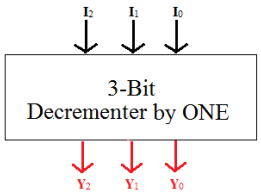

FIG. 8. 3-BIT DECREMENTER BY M=1 BLOCK

TABLE VIII (a). TRUTH TABLE FOR 3-BIT DECREMENTER BY M=1 VALUE

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3-bit Input			3-bit Decrementer by ONE Output		
I_2	I_1	I_0	Y_2	Y_1	Y_0
0	0	0	1	1	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

TABLE VIII (b). K-MAP IMPLEMENTATION FOR 3-BIT DECREMENTER OUTPUT Y_0 BY M=1 VALUE

Y_0	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
0 ($\bar{I}_2$)	1	0	0	1
1 (I_2)	1	0	0	1

TABLE VIII (c). K-MAP IMPLEMENTATION FOR 3-BIT DECREMENTER OUTPUT Y_1 BY M=1 VALUE

Y_1	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
0 ($\bar{I}_2$)	1	0	1	0
1 (I_2)	1	0	1	0

TABLE VIII (d). K-MAP IMPLEMENTATION FOR 3-BIT DECREMENTER OUTPUT Y_2 BY M=1 VALUE

Y_2	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
0 ($\bar{I}_2$)	1	0	0	0
1 (I_2)	0	1	1	1

Initially, By K-Map, Realizing the Logical Expressions for 3-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 3-bit Input 'I' and 3-bit Input value M=7 (i.e. 111 in binary) and considering Truth Table as shown in TABLE VIII (a), TABLE VIII (b), TABLE VIII (c) and TABLE VIII (d), we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (14)}$$

$$Y_1 = \overline{I_1}\ \overline{I_0} + I_1 I_0 = \overline{I_1 \oplus I_0} \qquad \text{Eqn (15)}$$

$$Y_2 = \overline{I_2}\ \overline{I_1}\ \overline{I_0} + I_2 I_0 + I_2 I_1 = \overline{I_2 \oplus [I_1 + I_0]} \qquad \text{Eqn (16)}$$

C. 4-bit Decrementer by M=1

The 4-bit Decrementer by M=1 value Block Design is as shown in the "Fig. 9" below. It is used to subtract the given 4-bit Input by a value M=1.

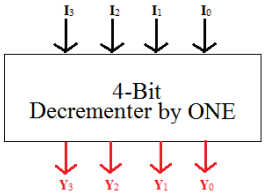

FIG. 9. 4-BIT DECREMENTER BY M=1 BLOCK

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TABLE IX (a). TRUTH TABLE FOR 4-BIT DECREMENTER BY M=1 VALUE

4-bit Input				4-bit Decrementer by ONE Output			
I_3	I_2	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	1	1	1	1
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	1
0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	1	1	1
1	0	0	1	1	0	0	0
1	0	1	0	1	0	0	1
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	1	0

TABLE IX (b). K-MAP IMPLEMENTATION FOR 4-BIT DECREMENTER OUTPUT Y_0 BY M=1 VALUE

Y_0	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	1	0	0	1
01 ($\bar{I}_3$ I_2)	1	0	0	1
11 (I_3 I_2)	1	0	0	1
10 (I_3 $\bar{I}_2$)	1	0	0	1

TABLE IX (c). K-MAP IMPLEMENTATION FOR 4-BIT DECREMENTER OUTPUT Y_1 BY M=1 VALUE

Y_1	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	1	0	1	0
01 ($\bar{I}_3$ I_2)	1	0	1	0
11 (I_3 I_2)	1	0	1	0
10 (I_3 $\bar{I}_2$)	1	0	1	0

TABLE IX (d). K-MAP IMPLEMENTATION FOR 4-BIT DECREMENTER OUTPUT Y_2 BY M=1 VALUE

Y_2	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	1	0	0	0
01 ($\bar{I}_3$ I_2)	0	1	1	1
11 (I_3 I_2)	0	1	1	1
10 (I_3 $\bar{I}_2$)	1	0	0	0

TABLE IX (e). K-MAP IMPLEMENTATION FOR 4-BIT DECREMENTER OUTPUT Y_3 BY M=1 VALUE

Y_3	00 ($\bar{I}_1$ $\bar{I}_0$)	01 ($\bar{I}_1$ I_0)	11 (I_1 I_0)	10 (I_1 $\bar{I}_0$)
00 ($\bar{I}_3$ $\bar{I}_2$)	1	0	0	0
01 ($\bar{I}_3$ I_2)	0	0	0	0
11 (I_3 I_2)	1	1	1	1

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10 (I_3 $\overline{I_2}$)	0	1	1		1

Initially, By K-Map, Realizing the Logical Expressions for 4-bit Input and Later, Realizing the Logical Expressions by the Concept of Full Adder Addition between 4-bit Input 'I' and 4-bit Input value M=15 (i.e. 1111 in binary) and considering Truth Table as shown in TABLE IX (a), TABLE IX (b), TABLE IX (c), TABLE IX (d) and TABLE IX (e), we have,

$$Y_0 = \overline{I_0} \qquad \text{Eqn (17)}$$

$$Y_1 = \overline{I_1}\ \overline{I_0} + I_1\, I_0 = \overline{I_1 \oplus I_0} \qquad \text{Eqn (18)}$$

$$Y_2 = \overline{I_2}\ \overline{I_1}\ \overline{I_0} + I_2\, I_0 + I_2\, I_1 = \overline{I_2 \oplus [I_1 + I_0]} \qquad \text{Eqn (19)}$$

$$Y_3 = \overline{I_3}\ \overline{I_2}\ \overline{I_1}\ \overline{I_0} + I_3\, I_2 + I_3\, I_1 + I_3\, I_0 = \overline{I_3 \oplus [I_2 + I_1 + I_0]} \qquad \text{Eqn (20)}$$

D. N-bit Decrementer by M=1

The N-bit Decrementer by M=1 value Block Design is as shown in the "Fig. 10" below. It is used to subtract the given N-bit Input by a value M=1.

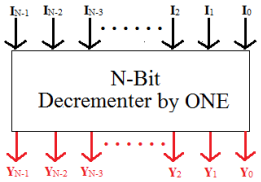

FIG. 10. N-BIT DECREMENTER BY M=1 BLOCK

TABLE X. TRUTH TABLE FOR N-BIT DECREMENTER BY M=1 VALUE

N-bit Input					**N-bit Decrementer by ONE Output**				
I_{N-1}	I_{N-2}	. . .	I_1	I_0	Y_{N-1}	Y_{N-2}	. . .	Y_1	Y_0
0	0		0	0	1	1		1	1
0	0	.	0	1	0	0	.	0	0
0	0	.	1	0	0	0	.	0	1
0	0	.	1	1	0	0	.	1	0
0	0	.	0	0	0	0	.	1	1
0	0		0	1	0	0		0	0
.		.		.	.		.		.
.		.		.	.		.		.
		.					.		
1	1		1	0	1	1		0	1
1	1	.	1	1	1	1	.	1	0
1	1	.	0	0	1	1	.	1	1
1	1	.	0	1	1	1	.	0	0
1	1	.	1	0	1	1	.	0	1
1	1		1	1	1	1		1	0

Initially, By K-Map, Realizing the Logical Expressions for N-bit Input, it is found to be very complex process if N > 4, and the Later stage, Realizing the Logical Expressions by the Concept of Full Adder Addition between N-bit Input 'I' and

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N-bit Input value M=Maximum Value of the Bit Capacity i.e. 1, 3, 7, 15, $(2^N - 1)$ and so on for 1-bit, 2-bit, 3-bit, 4-bit and N-bit Respectively and considering Truth Table as shown in TABLE X, we have,

$$Y_P = \begin{cases} \overline{I_0}, & P = 0 \\ I_P \oplus \left[I_{(P-1)} + I_{(P-2)} + \ldots + I_1 + I_0\right], & 0 < P < N \end{cases} \qquad \text{Eqn (21)}$$

III. RESULTS AND DISCUSSION

The 4-bit Incrementer and Decrementer by M=1 value Circuit Design is implemented in cadence virtuoso environment and the waveforms for the same are obtained and found that it verifies the logic functional Truth Table perfectly for all the combination of inputs of a 4-bit Incrementer and Decrementer operation. The same is verified for 8, 16, 32 and 64-bit input Incrementer and Decrementer circuits also. N-bit Incrementer Circuit and N-bit Decrementer Circuit, Cadence Virtuoso Implementation of 4-bit Incrementer Circuit, 4-bit Incrementer Input-Output Waveform, Cadence Virtuoso Implementation of 4-bit Decrementer Circuit and 4-bit Decrementer Input-Output Waveform are as shown in the "Fig. 11", "Fig. 12", "Fig. 13", "Fig. 14", "Fig. 15" and "Fig. 16" below respectively.

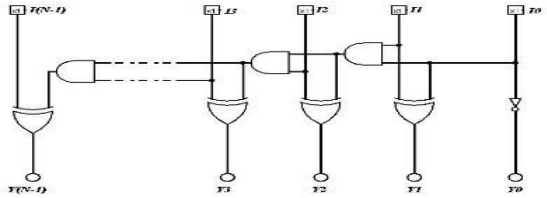

FIG. 11. N-BIT INCREMENTER CIRCUIT

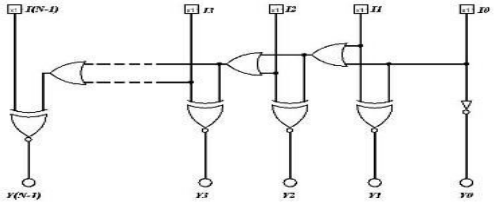

FIG. 12. N-BIT DECREMENTER CIRCUIT

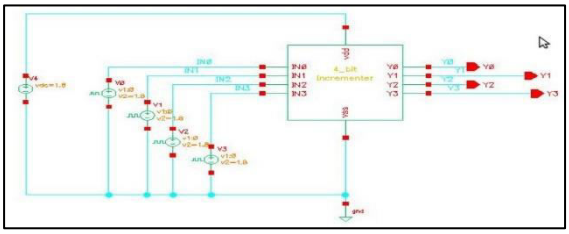

FIG. 13. CADENCE VIRTUOSO IMPLEMENTATION OF 4-BIT INCREMENTER CIRCUIT

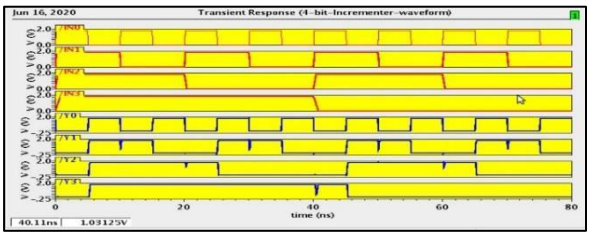

FIG. 14. 4-BIT INCREMENTER INPUT-OUTPUT WAVEFORM

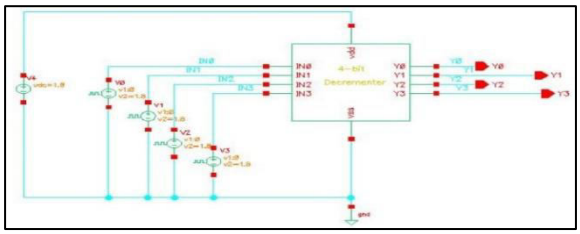

FIG. 15. CADENCE VIRTUOSO IMPLEMENTATION OF 4-BIT DECREMENTER CIRCUIT

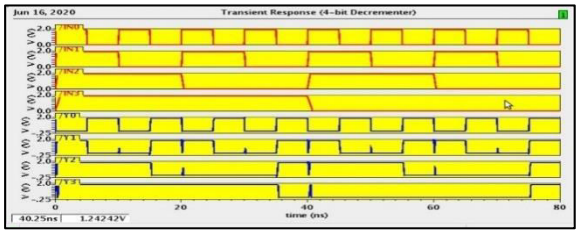

FIG. 16. 4-BIT DECREMENTER INPUT-OUTPUT WAVEFORM

IV. CONCLUSION

The Generalized Expression for N-bit Incrementer and Decrementer operation is obtained for M=1 value. The same logic can be enhanced for generalizing the input-output relation expressions and further to implement the same for various applications on demand can be very easily done for $M=2^X$ values. If 'M' is other than the 2^X values, then the logic can be slightly varied to arrive for General Expression as per the user applications and requirements. The same concepts can also be used to Generalize the input-output relation expressions for various components of an ALU and other VLSI Digital design components.

V. REFERENCES

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VI. AUTHOR DETAILS

Manjunath K M is an Assistant Professor at RVITM, Bengaluru and a research scholar pursuing his Ph.D in PET Research Centre, (PESCE), Mandya, under VTU Part Time Ph.D from 2014 in the VLSI domain. His area of research interests is VLSI, Analog Mixed Signal Circuits, Low Power Low Voltage Circuit techniques, VLSI Design Automation, etc. He has completed his Bachelor of Engineering degree in Jnana Vikasa Institute of Technology in 2011 in the specialization of Electronics and Communication Engineering and Master of Technology in P.E.S. College of Engineering, Mandya in 2013 in the specialization of VLSI Design and Embedded Systems and worked in various institutes like PESCE Mandya, BITM Bellary, RYMEC Bellary and presently working in RVITM, Bengaluru as an Assistant Professor in Electronics and Communication Engineering Department. He has an experience of 7 Years.

Dr. K N Muralidhara, is a Professor in the Electronics and Communication Engineering Department, BGSIT, Mandya. He has completed his Bachelor of Engineering Degree in P.E.S. College of Engineering, Mandya in 1981 in the specialization of Electronics and Communication Engineering and Master of Engineering and Doctor of Philosophy in Indian Institute of Technology Roorkee in 1990 and 1998 respectively. He has working experience of almost 37 years. His areas of research interests are Electronic devices, VLSI Design, Wireless communication, Mobile Communication. He has guided 4 Ph.D scholars and presently guiding 6 Ph.D scholars.

Dr. H. V. Ravish Aradhya is a professor at RV College of Engineering, Bengaluru. He has completed his Bachelor of Engineering Degree **in** Electronics and M.E. in Electronics and Ph.D in Low Power VLSI Design. He has more than of 27 Years of Teaching Experience. He has filed many patents and published many research papers and has authored many Engineering Text Books. He has also taken up various R & D Projects. He is guiding many Ph.D Scholars and His areas of Interest is VLSI and Embedded Systems.