HW3 Report

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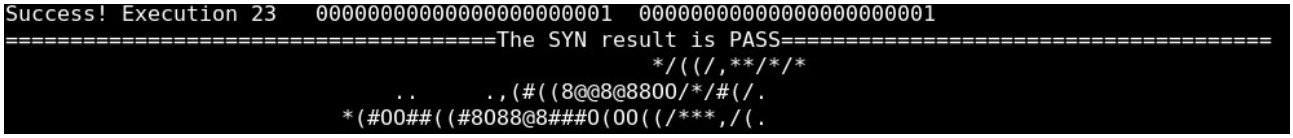
1. Snapshots

a. RTL(Pass)

b. SYN(Pass)



c. no latch

```
Inferred memory devices in process
        in routine CHIP line 169 in file
                '/home/raid7_2/userb07/b07069/Desktop/hw3/CHIP.v'.
===============================================================================
|     Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  instruction_type_reg  | Flip-flop |  23   |  Y  | N  | Y  | N  | N  | N  | N  |
| instruction_format_reg | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|     mem_addr_I_reg     | Flip-flop |  30   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb07/b07069/Desktop/hw3/CHIP.db:CHIP'
Loaded 1 design.
Current design is 'CHIP'.
Current design is 'CHIP'.
```

d. Timing report

```
CHIP               tsmc13_wl10           slow

Point                                    Incr       Path
-----------------------------------------------------------
clock CLK (rise edge)                    0.00       0.00
clock network delay (ideal)              0.50       0.50
mem_addr_I_reg_3_/CK (DFFRX2)            0.00       0.50 r
mem_addr_I_reg_3_/Q (DFFRX2)             0.26       0.76 r
add_53/A[1] (CHIP_DW01_inc_0)            0.00       0.76 r
add_53/U1_1_1/CO (ADDHX1)                0.17       0.93 r
add_53/U1_1_2/CO (ADDHX2)                0.13       1.07 r
add_53/U1_1_3/CO (ADDHX2)                0.14       1.20 r
add_53/U1_1_4/CO (ADDHX4)                0.10       1.31 r
add_53/U1_1_5/CO (ADDHX2)                0.13       1.44 r
add_53/U1_1_6/CO (ADDHX4)                0.10       1.54 r
add_53/U1_1_7/CO (ADDHX2)                0.13       1.67 r
add_53/U1_1_8/CO (ADDHX4)                0.10       1.77 r
add_53/U1_1_9/CO (ADDHX2)                0.13       1.90 r
add_53/U1_1_10/CO (ADDHX4)               0.10       2.01 r
add_53/U1_1_11/CO (ADDHX2)               0.13       2.13 r
add_53/U1_1_12/CO (ADDHX4)               0.10       2.24 r
add_53/U1_1_13/CO (ADDHX2)               0.10       2.34 r
add_53/U1_1_14/CO (ADDHXL)               0.20       2.54 r
add_53/U1_1_15/CO (ADDHXL)               0.21       2.75 r
add_53/U1_1_16/CO (ADDHXL)               0.21       2.97 r
add_53/U1_1_17/CO (ADDHXL)               0.21       3.18 r
add_53/U1_1_18/CO (ADDHXL)               0.21       3.40 r
add_53/U1_1_19/CO (ADDHXL)               0.21       3.61 r
add_53/U1_1_20/CO (ADDHXL)               0.21       3.83 r
add_53/U1_1_21/CO (ADDHXL)               0.21       4.04 r
add_53/U1_1_22/CO (ADDHXL)               0.21       4.26 r
add_53/U1_1_23/CO (ADDHXL)               0.23       4.49 r
add_53/U1_1_24/CO (ADDHX1)               0.19       4.68 r
add_53/U1_1_25/CO (CMPR22X2)             0.14       4.82 r
add_53/U1_1_26/CO (CMPR22X2)             0.12       4.94 r
add_53/U1_1_27/CO (ADDHX2)               0.12       5.06 r
add_53/U1_1_28/CO (ADDHX2)               0.11       5.17 r
add_53/U1/Y (XOR2X2)                     0.09       5.26 r
add_53/SUM[29] (CHIP_DW01_inc_0)         0.00       5.26 r
mem_addr_I_reg_31_/D (DFFRX2)            0.00       5.26 r
data arrival time                                   5.26

clock CLK (rise edge)                    5.00       5.00
clock network delay (ideal)              0.50       5.50
clock uncertainty                       -0.10       5.40
mem_addr_I_reg_31_/CK (DFFRX2)           0.00       5.40 r
library setup time                      -0.10       5.30
data required time                                  5.30
-----------------------------------------------------------
data required time                                  5.30
data arrival time                                  -5.26
-----------------------------------------------------------
slack (MET)                                         0.03
```

e. Area report

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Tue Dec  1 01:27:52 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                          153
Number of nets:                           395
Number of cells:                          239
Number of combinational cells:            180
Number of sequential cells:                58
Number of macros/black boxes:               0
Number of buf/inv:                         78
Number of references:                      32

Combinational area:               2359.385976
Buf/Inv area:                      899.621994
Noncombinational area:            1904.482742
Macro/Black Box area:                0.000000
Net Interconnect area:           28186.808014

Total cell area:                  4263.868719
Total area:                      32450.676733
```

2. Circuit Design & Experience

我把 output 全部設成 reg type，對於每個 output reg 設一個 reg next_XXX 的變數，並且把所有要輸出的內容設成 constants。Combinational logic 的部份就是每次都把 mem_addr_I 加 1，之後取 mem_rdata_I 的相應位置（opcode, func7, funct3...）寫一堆 if else 去輸出。而 sequential logic 的部份就是 rst_n 時就把 output reg 全部設成 0，否則就把 next_XXX assign 到相對應的 output reg。

在這次作業上遇到的困難大概就是因為是第一次寫 Verilog 所以語法不太熟，還有查表查得很累，除此之外應該沒有什麼困難。

經過這次作業後對 Verilog 和相關的工具有了粗淺的認識，希望接下來的作業和期末的 project 能順利。