HW4 Report

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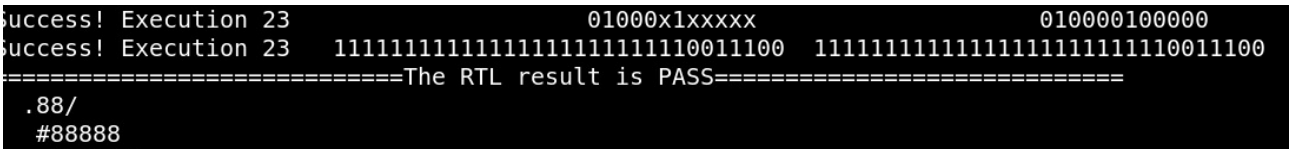
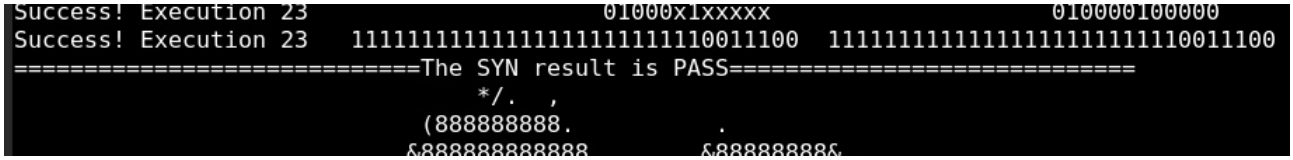
Snapshots

a. RTL(Pass)



b. SYN(Pass)



c. no latch

```
Inferred memory devices in process
        in routine HW4 line 247 in file
                '/home/raid7_2/userb07/b07069/Desktop/HW4/HW4.v'.
===============================================================================
|      Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
| delayed_mem_rdata_I_reg | Flip-flop |  25   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb07/b07069/Desktop/HW4/HW4.db:HW4'
Loaded 1 design.
Current design is 'HW4'.
Loading verilog file '/home/raid7_2/userb07/b07069/Desktop/HW4/HW3.v'
Detecting input file type automatically (-rtl or -netlist).
Reading with Presto HDL Compiler (equivalent to -rtl option).
Running PRESTO HDLC
Compiling source file /home/raid7_2/userb07/b07069/Desktop/HW4/HW3.v
Warning:  /home/raid7_2/userb07/b07069/Desktop/HW4/HW3.v:9: Empty port in module declara
Warning:  /home/raid7_2/userb07/b07069/Desktop/HW4/HW3.v:1: Port number 7 of 'HW3' was n

Inferred memory devices in process
        in routine HW3 line 169 in file
                '/home/raid7_2/userb07/b07069/Desktop/HW4/HW3.v'.
===============================================================================
|     Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  instruction_type_reg  | Flip-flop |  23   |  Y  | N  | Y  | N  | N  | N  | N  |
| instruction_format_reg | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|     mem_addr_I_reg     | Flip-flop |  30   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb07/b07069/Desktop/HW4/HW3.db:HW3'
Loaded 1 design.
```

d. Timing report

```
HW4                tsmc13_wl10           slow

Point                                                  Incr       Path
-----------------------------------------------------------------------------
clock CLK (rise edge)                                  0.00       0.00
clock network delay (ideal)                            0.50       0.50
decoder/mem_addr_I_reg_3_/CK (DFFRX2)                  0.00       0.50 r
decoder/mem_addr_I_reg_3_/Q (DFFRX2)                   0.26       0.76 r
decoder/add_53/A[1] (HW3_DW01_inc_0)                   0.00       0.76 r
decoder/add_53/U1_1_1/CO (ADDHX1)                      0.17       0.93 r
decoder/add_53/U1_1_2/CO (ADDHX2)                      0.13       1.07 r
decoder/add_53/U1_1_3/CO (ADDHX2)                      0.14       1.20 r
decoder/add_53/U1_1_4/CO (ADDHX4)                      0.10       1.31 r
decoder/add_53/U1_1_5/CO (ADDHX2)                      0.13       1.44 r
decoder/add_53/U1_1_6/CO (ADDHX4)                      0.10       1.54 r
decoder/add_53/U1_1_7/CO (ADDHX2)                      0.13       1.67 r
decoder/add_53/U1_1_8/CO (ADDHX4)                      0.10       1.77 r
decoder/add_53/U1_1_9/CO (ADDHX2)                      0.13       1.90 r
decoder/add_53/U1_1_10/CO (ADDHX4)                     0.10       2.01 r
decoder/add_53/U1_1_11/CO (ADDHX2)                     0.13       2.13 r
decoder/add_53/U1_1_12/CO (ADDHX4)                     0.10       2.24 r
decoder/add_53/U1_1_13/CO (ADDHX2)                     0.10       2.34 r
decoder/add_53/U1_1_14/CO (ADDHXL)                     0.20       2.54 r
decoder/add_53/U1_1_15/CO (ADDHXL)                     0.21       2.75 r
decoder/add_53/U1_1_16/CO (ADDHXL)                     0.21       2.97 r
decoder/add_53/U1_1_17/CO (ADDHXL)                     0.21       3.18 r
decoder/add_53/U1_1_18/CO (ADDHXL)                     0.21       3.40 r
decoder/add_53/U1_1_19/CO (ADDHXL)                     0.21       3.61 r
decoder/add_53/U1_1_20/CO (ADDHXL)                     0.21       3.83 r
decoder/add_53/U1_1_21/CO (ADDHXL)                     0.21       4.04 r
decoder/add_53/U1_1_22/CO (ADDHXL)                     0.21       4.26 r
decoder/add_53/U1_1_23/CO (ADDHXL)                     0.23       4.49 r
decoder/add_53/U1_1_24/CO (ADDHX1)                     0.19       4.68 r
decoder/add_53/U1_1_25/CO (CMPR22X2)                   0.14       4.82 r
decoder/add_53/U1_1_26/CO (CMPR22X2)                   0.12       4.94 r
decoder/add_53/U1_1_27/CO (ADDHX2)                     0.12       5.06 r
decoder/add_53/U1_1_28/CO (ADDHX2)                     0.11       5.17 r
decoder/add_53/U1/Y (XOR2X2)                           0.09       5.26 r
decoder/add_53/SUM[29] (HW3_DW01_inc_0)                0.00       5.26 r
decoder/mem_addr_I_reg_31_/D (DFFRX2)                  0.00       5.26 r
data arrival time                                                 5.26

clock CLK (rise edge)                                  5.00       5.00
clock network delay (ideal)                            0.50       5.50
clock uncertainty                                     -0.10       5.40
decoder/mem_addr_I_reg_31_/CK (DFFRX2)                 0.00       5.40 r
library setup time                                    -0.10       5.30
data required time                                                5.30
-----------------------------------------------------------------------------
data required time                                                5.30
data arrival time                                                -5.26
-----------------------------------------------------------------------------
slack (MET)                                                       0.03
```

e. Area report

```
****************************************
Report : area
Design : HW4
Version: N-2017.09-SP2
Date   : Sat Dec 12 23:34:38 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_

Number of ports:                          246
Number of nets:                           623
Number of cells:                          404
Number of combinational cells:            318
Number of sequential cells:                84
Number of macros/black boxes:               0
Number of buf/inv:                        116
Number of references:                      49

Combinational area:               3584.908788
Buf/Inv area:                     1227.220206
Noncombinational area:            2707.352913
Macro/Black Box area:                0.000000
Net Interconnect area:           48626.912201

Total cell area:                  6292.261701
Total area:                      54919.173902
```

f. Cycle time

```
1   cycle time: 5
```