Morten Sørensen

+47 940 59 660 | morsore@stud.ntnu.no | Linkedin | GitHub

Education

Norwegian University of Science and Technology — Trondheim, Norway
Master of Science in Electrical and Electronics Engineering — *Aug. 2023 – Jun 2028*

Experience

FPGA Engineer — September 2024 – Present
Orbit NTNU — *Trondheim, Norway*

- Developing FPGA-based system in SystemVerilog for reading data from sattelite IMU sensors through SPI.
- Developing Kalman filter module for sensor data processing.
- Utilizing AXI Stream interface for data transfer between modules.
- Deployment on Xilinx FPGAs, utilizing Vivado and Verilator for synthesis design verification.

Autonomous Systems Engineer — September 2023 – June 2024
Ascend NTNU — *Trondheim, Norway*

- Developed autonomous systems for detecting and avoiding collisions between autonomous drones.
- Utilized RRT* based algorithms for path planning and collision avoidance.

Seasonal worker – Part time — March 2023 – June 2023
Plantasjen — *Bergen, Norway*

Projects

FPGA-based 3D Graphics Processing Unit | *SystemVerilog, Vivado, Verilator, Git* — August 2024 – Present

- Working in a team to develop a FPGA based fixed pipeline GPU for 3D graphics rendering for a flight simulator in the subject TDT4295 Computer Design Project.
- Developing Vertex Shader, Vertex Post-Processor, Primitives Assembler and binner, Rasterizer and Fragment Shader in SystemVerilog based on previous experience with software-based rendering techniques.
- Utilizing AXI interfaces and FIFO streams for communication and data transfer between modules.
- Utilizing SPI for inter-chip communication
- Developing the requirements and spesifications for the system based on the constraints of the chosen Xilinx FPGA.
- Writing testbenches in C++ utilizing Verilator for fast simulation.

3D Rasterizer | *C/C++, Git* — May 2024 – September 2024

- Implemented a fully functioning 3D rasterizer in C from scratch
- Utilizing multithreading to increase performance
- Implemented Phong shading and perspective-correct texture sampling for realistic looking rendering

FPGA-based FIR Filter | *SystemVerilog, Vivado, AXI* — April 2024 – June 2024

- Developed a FIR filter in SystemVerilog for filtering data from on-chip ADC
- Utilized AXI interfaces for communication between ADC and FIR filter
- Deployment on Xilinx FPGAs, utilizing Vivado for synthesis and design verification

Competitions

Norwegian Informatics Olympiad – Finals — March 2023

International Mathematical Modeling Challenge — March 2023

- Represented Norway as a part of a team of 4 in IMMC 2023, where we got an Honorary Mention.

Cyberlandslaget – Finale — April 2023

- Finalist in the qualifier for the Norwegian national hacking team, who were set to compete in the European Cyber Security Challenge

Skills

Languages: Python, C/C++, VHDL, Verilog/SystemVerilog, ARM Assembly
Technologies: Vivado, Verilator, AXI
Developer Tools: Git, Linux, CMake, Valgrind, gdb
Soft Skills: Communication, Teamwork, Planning