Morteza Baradaran

434-257-3579
morteza@virginia.edu
Homepage - Linkedin
github.com/Morteza1814

85 Engineer's Way,
Rice Hall, Office:Rice 530
University of Virginia,
Charlottesville, VA 22904

Overview

My interests lie broadly in Computer Architecture, Bioinformatics, and Domain Specific Accelerators. I'm interested in exploring novel hardware and software techniques to enhance the performance, energy efficiency, and programmability of domain specific accelerators. I also have extensive experience in designing high-performance, energy-efficient embedded systems for core consumer products.

•**Current research highlights:** I am actively engaged in implementing a partial matching tool to align unidentified genomes within extensive Metagenomic datasets. To enhance this process, I am utilizing processing-in-memory accelerators, which greatly optimize the efficiency of large hash table processing during the filtering step. Furthermore, I am conducting a comprehensive comparison of the precision and performance of my technique with established state-of-the-art methods, including BWA. Notably, our tool not only improves the matching precision for partial matches, accommodating more edit distances, but also maintains comparable performance levels to BWA.

Notable Projects

Accelerating Unidentified Genome Partial Matching
Language: *C/C++, Python*
Goal: Accelerating Metagenomics Unidentified Genome Partial Matching using Processing in Memory
Links: https://github.com/Morteza1814/GenomePartialMatching

HashMem
Language: *C/C++*
Goal: Implementing a PIM-based Hashmap Accelerator
Links: https://github.com/Morteza1814/HashMemCPU

Energy Consumption Analysis of Instruction Cache Prefetching
Language: *C/C++*, **Framework:** *ChampSim, CACTI-7*
Goal: Evaluating the energy consumption of instruction cache prefetching techniques

Banking Integrated Card Personalization System (IPS)
Language: *C, C++, Java*
Goal: Developing a Banking Card Personalization System Capable of Acquiring Customers' data and Personalizing it for Various Types of Banking Cards

Automatic Train Control Systems for Metro and Urban Railway
Language: *C++*
Goal: Developing and Analyzing Metro & Urban Railway Signalling and Telecommunication Systems (i.e., ATC, ATP, etc)

Self-Service Ticketing System of Tehran Metro and Bus Rapid Transit Routes
Language: *C, C++*
Goal: Developing Firmware, Memory Management, and File Management of the POS Terminals for Tehran's Subway Ticketing System

National Electronic Passport Operating System
Language: *C++*
Goal: Design and Implementation of OS Components for ARM7 Chip including Memory management, File System, and IO management

Education

University of Virginia, Charlottesville, USA — Sep. 2021 - Now
Ph.D., Computer Science (Advisor: Prof. Kevin Skadron) — (GPA: 3.95)

Sharif University of Technology, Tehran, Iran — Sep. 2010 - June 2012
M.Sc., Computer Architecture (Advisor: Prof. H. Sarbazi-Azad)

Shahed University, Tehran, Iran — Sep. 2006 - June 2010
B.Sc., Computer Engineering

Work Experience

Informatics Services Corp, Tehran, Iran — Sep. 2018 - Aug. 2021
Senior Software Development Engineer: Design and Development of Debit and Credit Card Personalization Systems

TOSAN Group Corp, Tehran, Iran — June 2017 - Apr. 2018
Lead Software Engineer: POS Development for ticketing system of Tehran Metro (QR, contactless cards)

MAHARAN Co, Tehran, Iran — May 2015 - Feb. 2017
Software Engineer: Design & development of Automatic Train Control (ATC) and intermediate block system

National-ID Co, Tehran, Iran — Jul 2012 - Dec. 2013
Hardware Specialist: Smart Card OS Design and Implementation including Memory management, File system, and I/O

Skills

Programming Languages/APIs:
• C/C++, Java, Python, Bash, Assembly Programming (x86), Verilog

Simulators and Analyzers:
• Gem5 Architectural Simulator, Multi2Sim, ChampSim, CACTI, Synopsys Synthesis

Benchmarking and Performance Analysis:
• SPEC Benchmarks, PARSEC Benchmarks

Industry Software Skills:
• KEIL , Jet Brain (IntelliJ IDEA, Youtrack), Microsoft SQL Server, OOP, DevOps, Design Patterns, JUnit, Maven, Sonarqube

Practical Skills:
• Embedded System Design, Software Development, Operating System Implementation, SOC Design

Research Experience

University of Virginia, Charlottesville, USA, Sep. 2021 - Now
Graduate Research Assistant
Projects:
• Accelerating Unidentified Genome Partial Matching using Processing in Memory

Institute for Research in Fundamental Sciences (IPM), Tehran, Iran, Sep. 2019 - Aug. 2021
Graduate Research Assistant
Projects:
• Energy Consumption Analysis of Instruction Cache Prefetching Methods

Sharif University of Technology, Tehran, Iran, Sep. 2010 - June 2012
Graduate Research Assistant
Projects:
• Obtaining Better Processor Performance through a Shared Structure between Cache and BTB

Publications

• A. Shekar, **Morteza Baradaran**, S. Tajdari, and K. Skadron, "HashMem: PIM-based Hashmap Accelerator," in *Fifth International Workshop on Domain-Specific System Architecture (DOSSA-5)*, 2023

• **M. Baradaran**, A. Ansari, M. Sadrosadati, and H. Sarbazi-Azad, "Energy Consumption Analysis of Instruction Cache Prefetching," in **Submission**

• **M. Baradaran** and M. Zarei, "Theory of Automata and Machine Language," in *National Library of Iran, ISBN 978-600-6927-22-0, 2012-2013*

Courses

CS6501: Hardware Accelerators Spring 2023
University of Virginia

CS6501: Geometry of Data Fall 2022
University of Virginia

CS6316: Machine Learning Spring 2022
University of Virginia

CS6160: Theory of Computation Fall 2021
University of Virginia

CS6354: Computer Architecture Fall 2021
University of Virginia

Teaching Experience

Teaching Assistant, CS4414: Undergraduate Operating System Fall 2022
University of Virginia

References

Two references will be made available upon request.