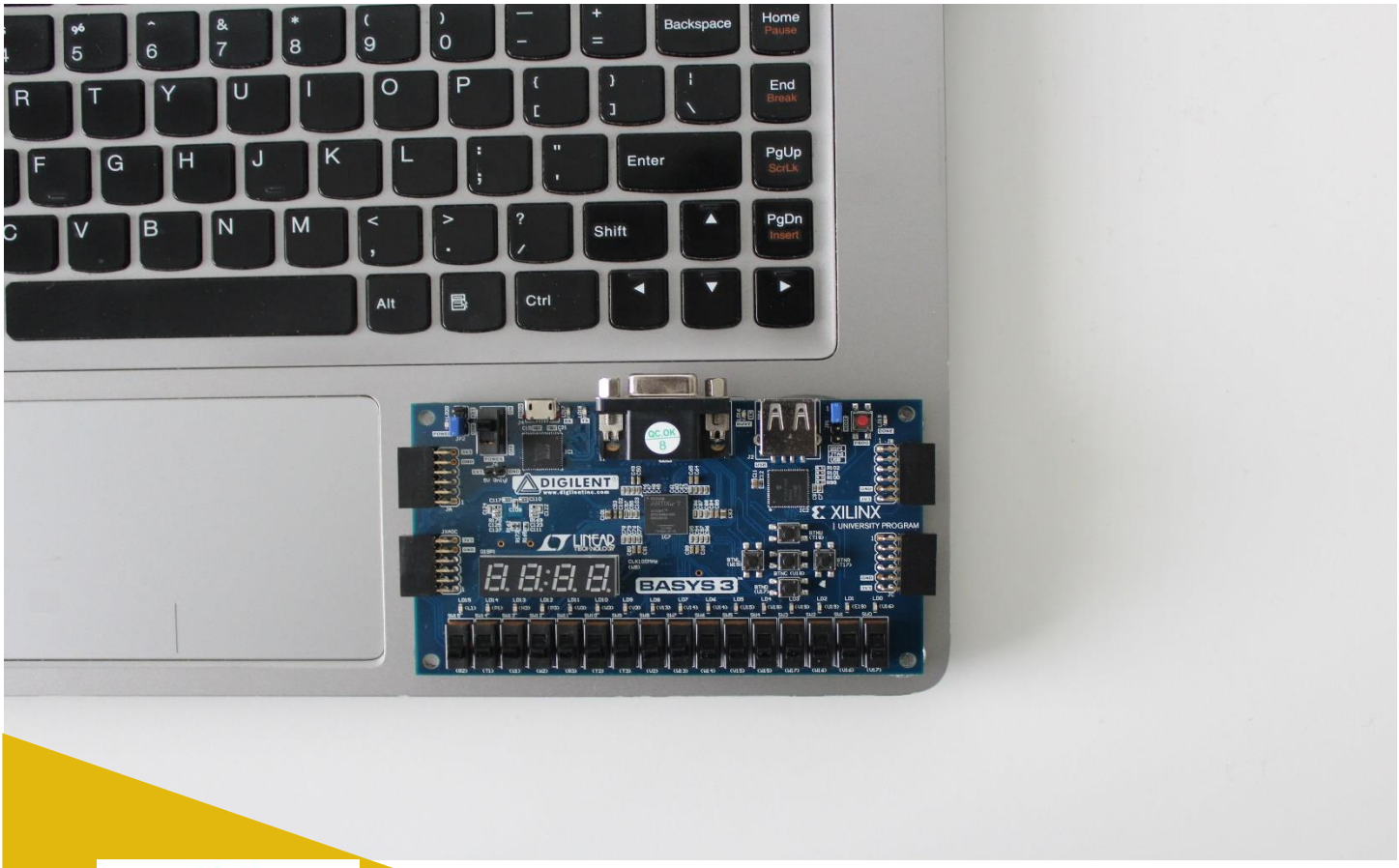
# FPGA Architecture

A briefing of the most important tips & considerations




SAMIM

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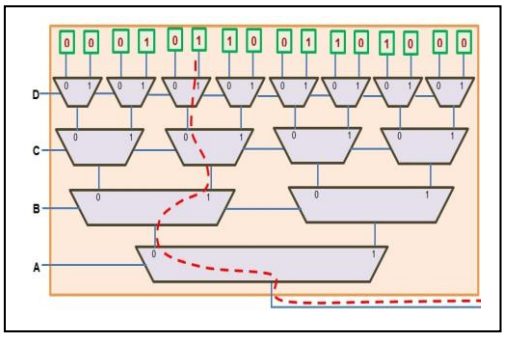
# Introduction to FPGA Architecture

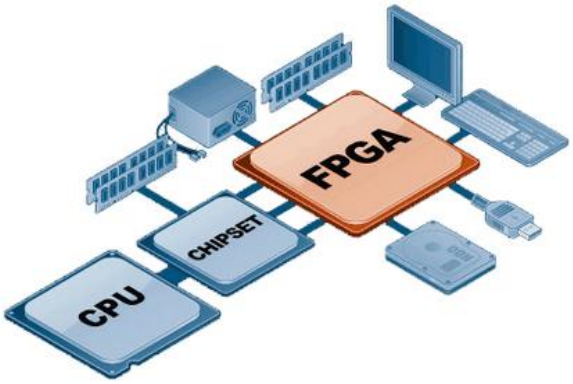
## Building blocks

The basic structure of an FPGA is composed of:

1. **Look-up table (LUT)**: This element performs logic operations. This element is able to implement **any logic function of N Boolean variables.**
2. **Flip-Flop (FF)**: This register element stores the result of the LUT. This element is **always paired with a LUT** to assist in logic pipelining and data storage
3. **Wires**: These elements connect elements to one another.
4. **Input/Output (I/O) pads**: These physically available ports get data in and out of the FPGA.




*Example of LUT hardware implementation (memory cells connected to multiplexers)*

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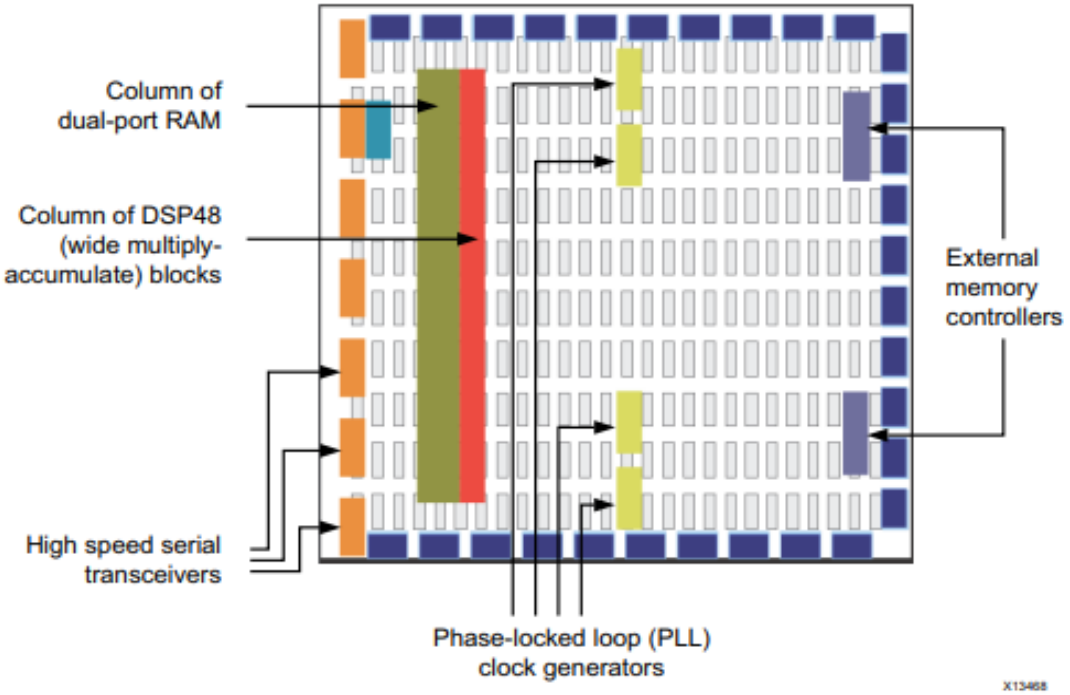
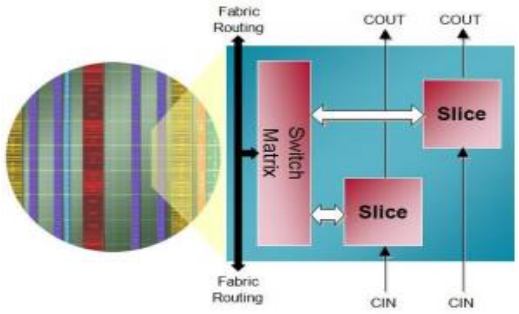



**Contemporary FPGA Architecture**

# Logic resources

Other than the blocks which are specified in the figure above, the main columns of FPGA architecture are formed by Configurable Logic Blocks (CLBs).

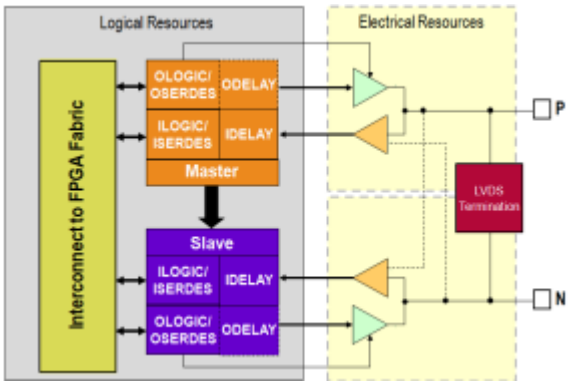
*Scheme of CLB, comprised of two slices & a switch matrix. Each slice is either capable of handling logic and memory (SLICEM) or just logic (SLICEL). Switch matrix connects the CLB to other FPGA resources.*



**Each slice has a variety of resources, the most important ones of which include:**

1. Four six-input LUTs: this can be treated as either two five-input LUTs with the same input ports, or one six-input LUT; in each of these scenarios the user is able to implement any logic function they wish.
2. Four flip-flops along with four additional latch/FFs. The FFs are connected to the output through a multiplexer, whereas additional FF/Latches are directly connected to the output, this in turn makes inferring latch in the output of VHDL codes possible.
3. Carry chains: Implements fast arithmetic addition/subtraction. Carry out is propagated vertically through four LUTs in a slice and then carry chain gets this result to the adjacent slice in the CLB just above.

SLICEM can be used in two different forms. It can be implemented as a 32-bit shift register which is connected to a 32-bit multiplexer that makes the register content addressable.
The other form which SLICEM comes in is as a distributed select-RAM, delivering the promised logic function of SLICEMs.

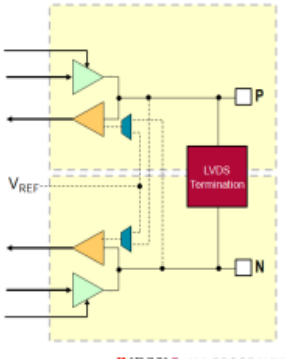



*I/O sources*

# I/O resources

Seven series FPGAs offer two general types of I/O banks, namely High Performance (HP) and High Range (HR). HP I/O port supports up to 1.8 volts and is the most suitable for delay management of output data as the ODELAY is only available in this type of I/O ports. It's also the better choice when dealing with a variable impedance at the I/O, since HP has the Digitally Controlled Impedance (DCI) capability. HR I/O port is obviously the better choice when dealing with a voltage-demanding I/O device. These pins are able to support voltages up to 3.3 volts. Note that as the technology evolves, the use case of high-powered devices decreases rapidly. Hence, the exclusion of HR I/O ports from some families of seven series FPGAs.

*P/N pins*
*available for both differential & single-ended signals.*



# Memory resources

FPGA has two types of memory; Block RAM (BRAM) and First In First Out (FIFO). BRAM comes in three different forms which are single port, dual port, and simple dual port. These forms only differ in number and arrangement of pins. In general, BRAM provides on-chip storage for a relatively large set of data. BRAM is capable of holding either 18 or 36 Kb arrays of data, but in case we need more storage capacity, there is the built-in cascade logic which allows us to cascade BRAMs and get capacities even more than 1Mb. FIFO is the more equipped version of BRAM which has four flags that tell us whether it's (almost) full or (almost) empty. FIFO is able to keep the input data in the same order and has separate synchronous read and write clocks. Remember that the write and read ports of FIFO are always of the same width.

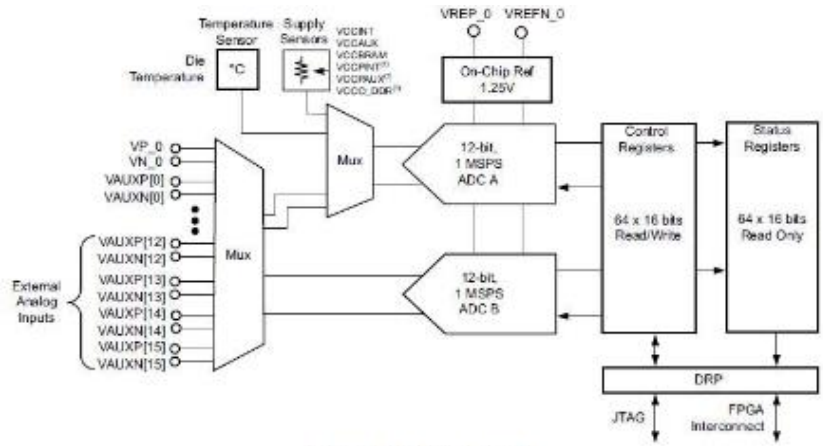



*Figure 1: XADC Block Diagram*

# XADC

XADC -Xilinx Analog to Digital Converter- is a high quality and flexible analog interface new to the 7-series. It has many interesting features that include but are not limited to: **customization using AMS** and **fast sampling**.

Analog Mixed Signal (AMS) helps with several methods that must be implemented in order for the data to be converted with better resolution. We tent to choose linearization, calibration, filtering, and DC balancing to serve that purpose. All these analog functions are within reach for ADC with the help of AMS.

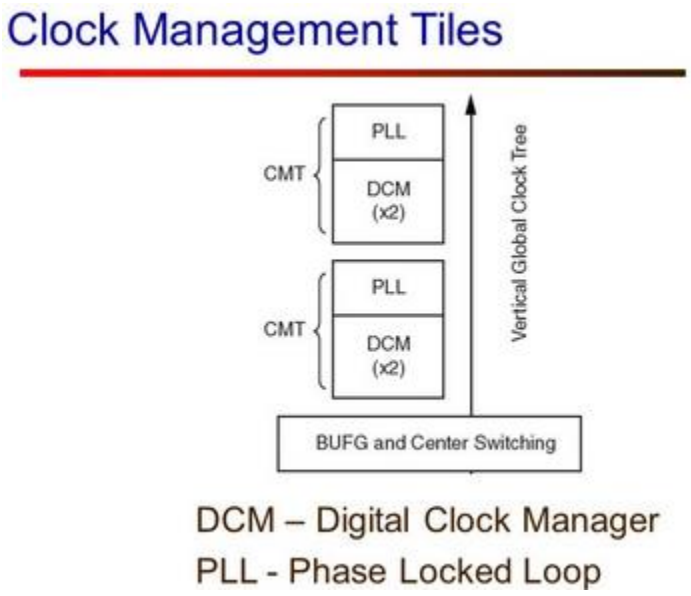
Fast sampling makes a couple of difficult tasks possible. Conversion time of 1 us with support for simultaneous sampling, flexible timing modes (self and externally triggered sampling modes), Separate track/hold amplifier for each ADC which ensures maximum throughput using multiplexed analog input channels, are a few examples. Interesting to know about that last task, when the ADC starts to convert an input voltage, the T/H is free to start pre-charging to the next voltage to be converted and it won't wait for the result of the first step of conversion.

# Clock

In each 7 series FPGA (except XC7S6 and XC7S15), 32 global clock lines have the highest fanout and can reach every flip-flop clock, clock enable, and set/reset, as well as many logic inputs. There are 12 global clock lines within any clock region driven by the horizontal clock buffers (BUFH). Each BUFH can be independently enabled/disabled, allowing for clocks to be turned off within a region, thereby offering control over which clock regions consume power. Global clocks are often driven from the Clock Management Tile (CMT), which can completely eliminate the basic clock distribution delay.

The architecture of the clock management unit includes:

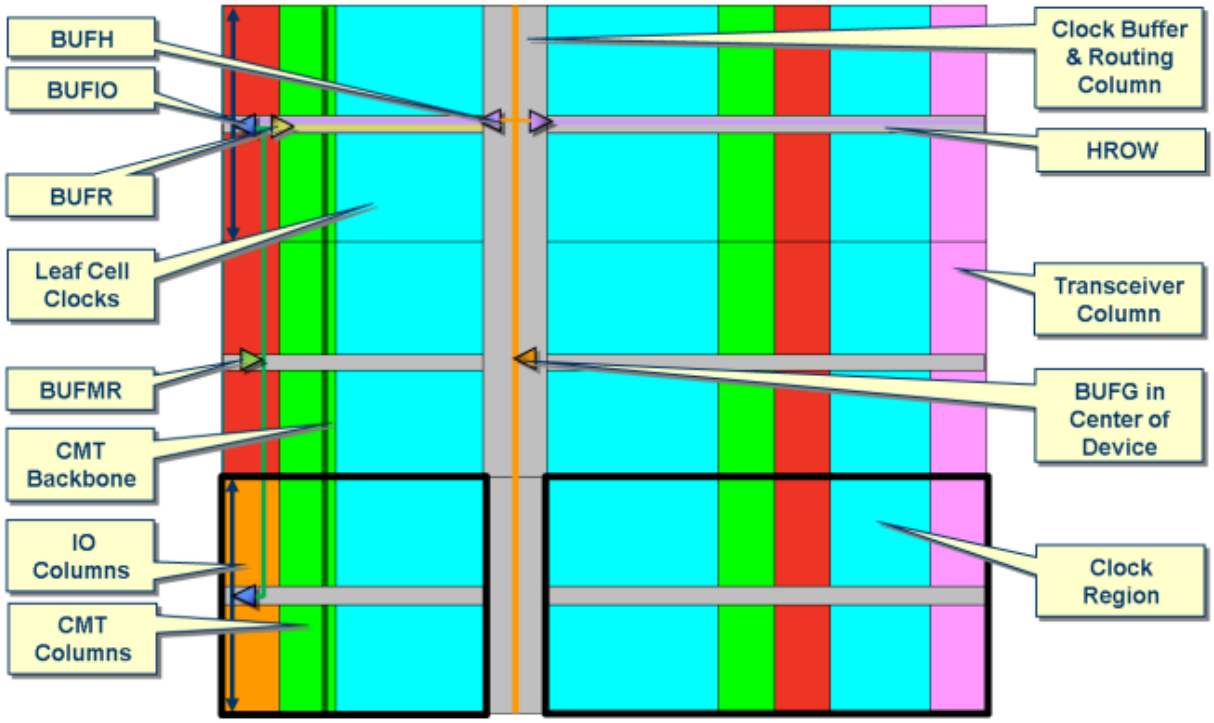
- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering




*each 7-series FPGA has up to 24 CMTs.*

*A PLL alongside with a DCM forms Mixed Mode Clock Manager (MMCM), which has the superiority of being able to handle digital clocks over PLL.*

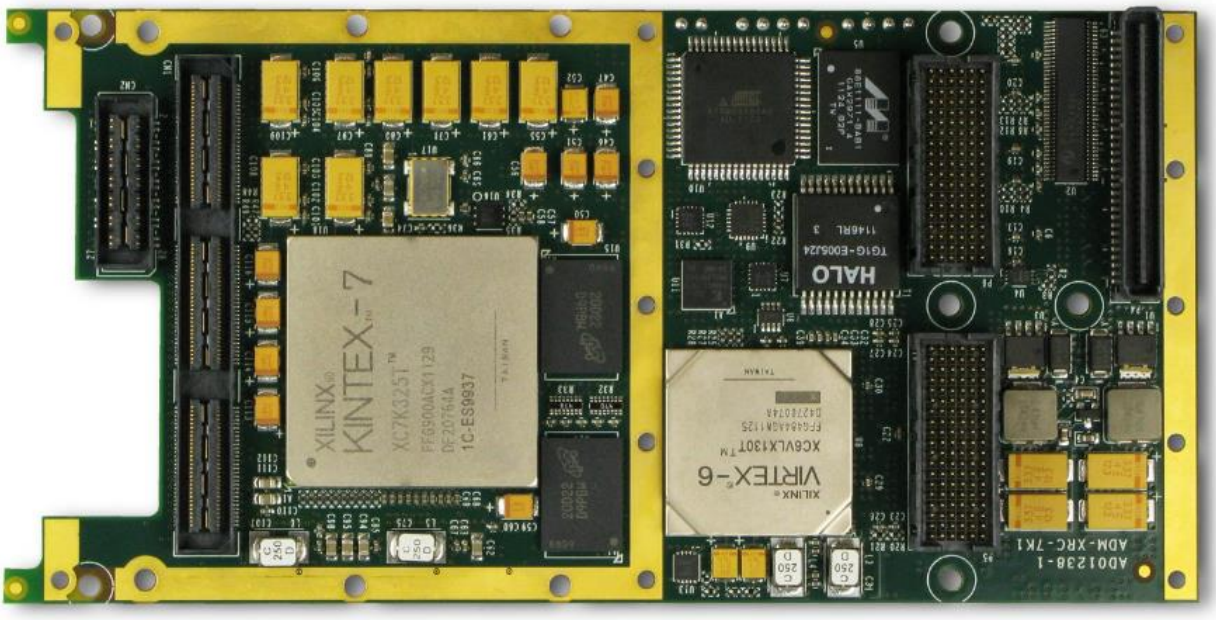
Regional clocks can drive all clock destinations in their region. A region is defined as an area that is 50 I/O and 50 CLB high and half the chip wide. 7 series FPGAs have between two and twenty-four regions. There are four regional clock tracks in every region. Each regional clock buffer can be driven from any of four clock-capable input pins, and its frequency can optionally be divided by any integer from 1 to 8.




*Die view of the clock buffers and rows*

About the figure above, bear in mind that:

- Global clock buffers (BUFGs) are in the middle of the chip.
- CMT columns which contain MMCMs and PLLs are immediately adjacent to the I/O columns.
- BUFRs are regional clock buffers.
- BUFHs run through the center of each clock region.
- Clocks are driven up and down from the center horizontal row (HROW) of each clock region.
- The BUFIO drive the I/O clock network in each bank.
- The BUFMR are dedicated buffers that allow clock inputs to drive the BUFIOs and BUFRs of **adjacent regions**.




Steve Jobs once said:

LEARN CONTINUALLY, THERE'S
ALWAYS "ONE MORE THING" TO LEARN!