

1. Description

1.1. Project

Project Name	Application_Firmware
Board Name	custom
Generated with:	STM32CubeMX 6.6.1
Date	12/05/2023

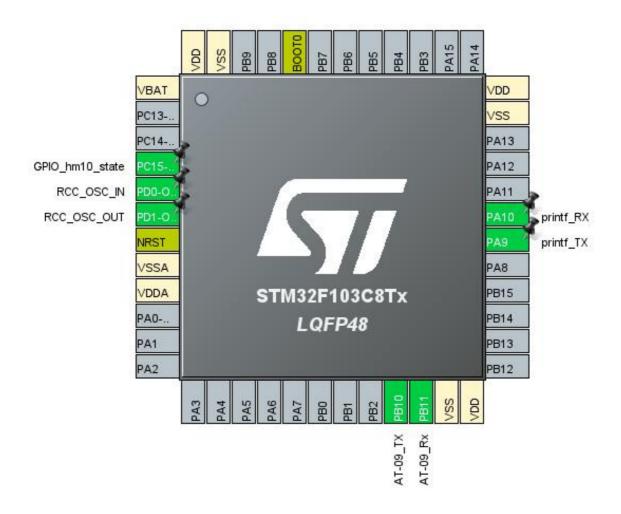
1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration

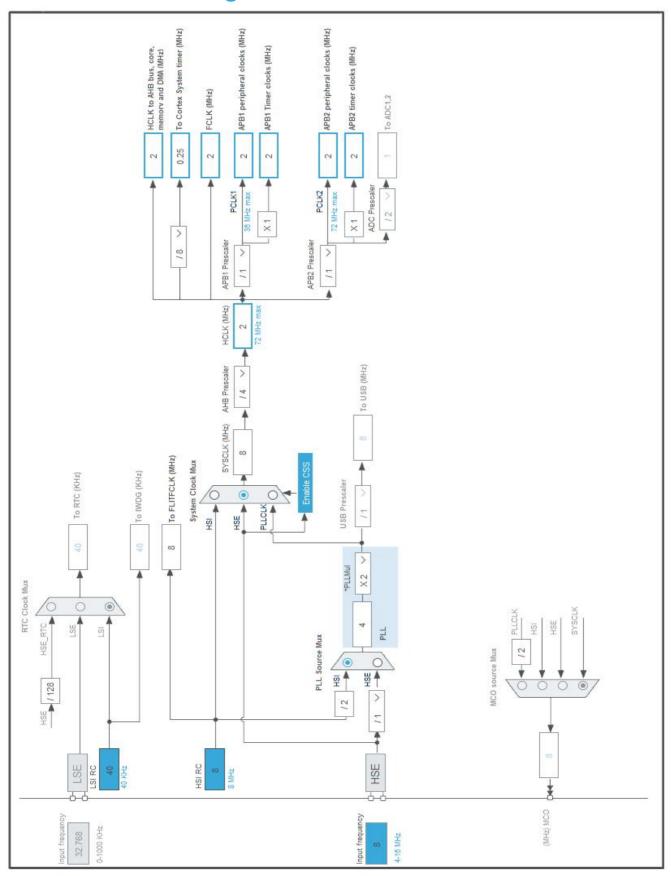


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
4	PC15-OSC32_OUT *	I/O	GPIO_Input	GPIO_hm10_state
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
21	PB10	I/O	USART3_TX	AT-09_TX
22	PB11	I/O	USART3_RX	AT-09_Rx
23	VSS	Power		
24	VDD	Power		
30	PA9	I/O	USART1_TX	printf_TX
31	PA10	I/O	USART1_RX	printf_RX
35	VSS	Power		
36	VDD	Power		
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value		
Project Name	Application_Firmware		
Project Folder	C:\Users\cmira\OneDrive\Escritorio\Bootloader Project		
Toolchain / IDE	STM32CubeIDE		
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.5		
Application Structure	Advanced		
Generate Under Root	Yes		
Do not generate the main()	No		
Minimum Heap Size	0x200		
Minimum Stack Size	0x400		

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_USART1_UART_Init	USART1
4	MX_USART3_UART_Init	USART3

7. Peripherals and Middlewares Configuration

7.1. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

7.2. SYS

Debug: No Debug

Timebase Source: SysTick

7.3. **USART1**

Mode: Asynchronous

7.3.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

7.4. **USART3**

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate **9600** *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PD0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	High *	printf_TX
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	n/a	printf_RX
USART3	PB10	USART3_TX	Alternate Function Push Pull	n/a	High *	AT-09_TX
	PB11	USART3_RX	Input mode	No pull-up and no pull-down	n/a	AT-09_Rx
GPIO	PC15- OSC32_OU T	GPIO_Input	Input mode	Pull-down *	n/a	GPIO_hm10_state

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true 15		0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
USART1 global interrupt	unused			
USART3 global interrupt	unused			

8.3.2. NVIC Code generation

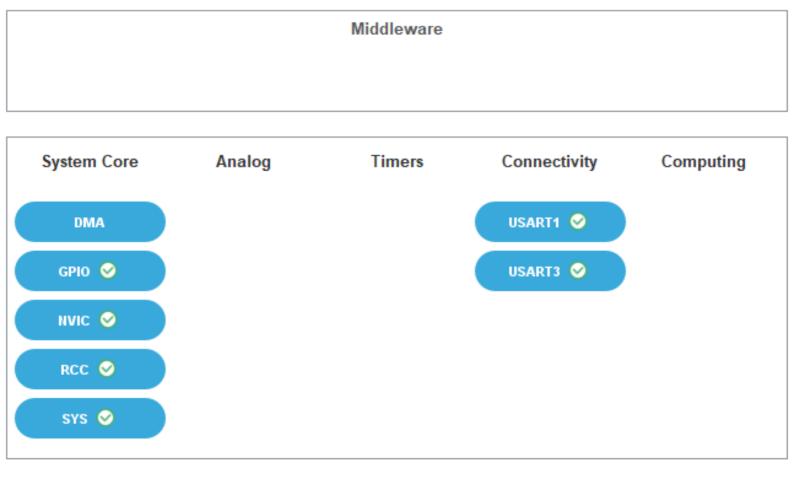
Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
	sequence ordening	Handlei	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f1_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32ibis.zip

System View https://www.st.com/resource/en/svd/stm32f1_svd.zip

Description

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- Application Notes https://www.st.com/resource/en/application_note/an3095-stevalisv002v1-stevalisv002v2-3-kw-gridconnected-pv-system-based-on-the-stm32f103xx-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an3108-stlm75-firmware-library-for-the-stm32f10x-stmicroelectronics.pdf
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