ABHINAV REDDY

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EDUCATION

Syracuse University Syracuse, NY
Master of Science in Computer Engineering Aug 2023 – May 2025
Kakatiya Institute of Technology & Science Warangal, India
Bachelor of Technology in Electronics and communication Aug 2019 – May 2023

EXPERIENCE

Syracuse University
Design & Verification Engineer Jun 2025 – Present

- Developing a UVM-based testbench to verify a 32-bit RISC-V processor core at the instruction level.
- Exploring cache coherence and memory hierarchy tests to align RISC-V verification with scalable SoC and IP design.
- Implementing monitors, scoreboards, and reusable sequences to validate ALU, control logic, and branching behavior.
- Performing constrained-random testing, assertion-based validation to catch edge-case bugs and track coverage progress.
- Using ModelSim and Verdi to debug RTL and waveform outputs, contributing to coverage closure efforts.
- Collaborating with academic project team to extend the verification plan and evaluate functional completeness.

Fabsilica
Design & Verification Engineer Jul 2022 – Jun 2023

- Contributed to SoC subsystem verification by developing modular UVM components for control and peripheral logic.
- Configured reusable environments to validate register interfaces, FSM behavior, and low-speed protocols.
- Tuned coverage models and implemented protocol-specific assertions to identify spec deviations early in the cycle.
- Debugged failing testcases using waveforms and logs, summarized findings for RTL feedback.
- Automated regression setup and log analysis using Python to improve simulation throughput.
- Engaged in peer reviews of test plans and implemented feedback to strengthen functional completeness.
- Built working knowledge of simulation flow, IP integration, and spec-to-test alignment under mentor guidance.

Defence Research and Development Organisation
Design & Verification Engineer Jan 2022 – Jun 2022

- Developed environment for control module verification using UVM, validated APB handshaking and FSM transitions.
- Implemented basic assertions and coverage bins to capture signal-level bugs and functional gaps.
- Collaborated with RTL designers during debug sessions to walk through waveforms and simulation anomalies.
- Participated in test sequence development for SoC initialization and protocol handshake phases.
- Supported FPGA-based design validation using Vivado; assisted in SPI IP configuration and bring-up.
- Authored daily debug summaries and verification logs to support documentation during internal reviews.
- Exposure to IP-level simulation flows and early-stage coverage-based testing under tight project deadlines.

TECHNICAL SKILLS

Design & Verification: UVM, RTL Design, FSMs, SoC Architecture, Assertion-Based Verification, Functional Coverage, Constrained Random Testing, Testbench Development, Coverage Closure, Simulation Automation
Languages & Scripting: SystemVerilog, Verilog, Python, C++, TCL, Perl
EDA & Debug Tools: Synopsys VCS, Cadence Xcelium, ModelSim, Verdi, Synplify, Vivado, Git
Protocols & Interfaces: APB, UART, SPI, I2C
Concepts & Analysis: Timing Analysis, CDC, Formal Verification, Regression Analysis, Debugging
Soft Skills: Analytical Thinking, Communication skills, problem-solving skills, Time Management, detail-oriented

PROJECTS

Instruction-Level UVM Verification of RISC-V Core Design Verification Intern – Syracuse University

- Developed a modular UVM testbench from scratch to verify a 32-bit RISC-V core, implementing directed and constrained-random instruction sequences, functional coverage models, assertions for pipeline behavior, and regression automation. **Tools & Tech:** SystemVerilog, UVM, ModelSim, Verilator, Git, RISC-V ISA

MESI-Based Multicore L1 Cache Verification Academic Project

- Built a modular UVM environment to verify L1 cache coherence using the MESI protocol under multicore access scenarios, applying randomized access patterns and functional coverage to improve verification completeness.
  Tools & Tech: SystemVerilog, UVM, ModelSim, Functional Coverage

HTAX Crossbar Functional Verification Academic Project

- Developed a layered UVM testbench to validate HTAX crossbar arbitration, routing, and data ordering across multi-initiator configurations using protocol-aware monitors, assertions, and randomized testing.
  Tools & Tech: SystemVerilog, UVM, Assertions, ModelSim

Design and Verification of 1x3 Packet Router

- Designed a 1x3 packet router in Verilog with FSM-based control logic and developed a layered UVM testbench to verify data integrity, routing correctness, and functional coverage through randomized and directed test scenarios.
  Tools & Tech: Verilog, SystemVerilog, UVM, ModelSim, FSM Design, Functional Coverage

APB Protocol Verification Using UVM

- Developed a modular UVM environment to verify APB protocol compliance, covering read/write transactions, wait states, error signaling, with protocol-aware monitors, assertions, functional coverage, and Python automation.
  Tools & Tech: SystemVerilog, UVM, ModelSim, Assertions, Functional Coverage, APB Protocol, Python

RTL Design of Floating Point Multiplication Unit

- Designed an IEEE-754 compliant floating-point multiplier unit, implementing sign, exponent, and mantissa logic with normalization, rounding, exception handling, and pipelined datapath control using SystemVerilog RTL.
  Tools & Tech: SystemVerilog, ModelSim, IEEE-754 Standard, RTL Simulation

FPGA-Based Dynamic Traffic Light Controller

- Designed a parameterized FSM-based traffic light controller in Verilog with dynamic timing logic, clock gating for power optimization, IDLE/SLEEP state transitions, synthesized design for FPGA deployment and functional validation.
  Tools & Tech: Verilog, FSM Design, Clock Gating, FPGA Implementation

FPGA-Based Secure IoT Communication

- Designed an AES encryption module in Verilog for secure MQTT communication, integrated with Python-based sensor simulation, synthesized and implemented on Artix-7 FPGA using Vivado for functional validation.
  Tools & Tech: Verilog, MQTT, Python, Artix-7 FPGA

HONORS AND AWARDS

Certifications: SystemVerilog for RTL Design and Functional Verification, Digital Design with Verilog HDL
Scholarship: 50% UG and 20% PG Merit Scholarships awarded for academic excellence (2019–2025)
Clubs and Societies: General Secretary – ECE Department Tech Fest, Kakatiya Institute of Technology & Science