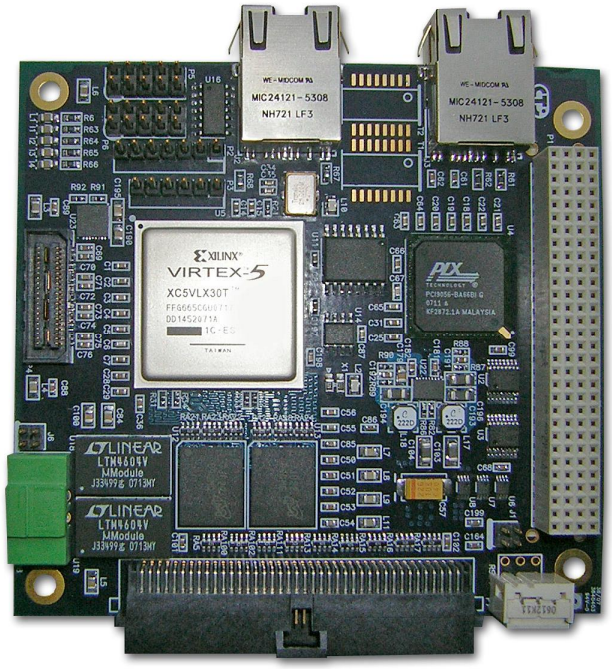
Connect Tech Inc.
Industrial Strength Communications

FreeForm/PCI-104

Hardware Modifications - Revision B to Revision C



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www.connecttech.com/support/support.asp. See the contact information section below for more information on how to contact us directly. Our technical support is always free.

Contact Information

We offer three ways for you to contact us:

Telephone/Facsimile
Technical Support representatives are ready to answer your call Monday through Friday, from 8:30 a.m. to 5:00 p.m. Eastern Standard Time. Our numbers for calls are:

Telephone:	800-426-8979 (North America only)
Telephone:	519-836-1291 (Live assistance available 8:30 a.m. to 5:00 p.m. EST, Monday to Friday)
Facsimile:	519-836-4878 (on-line 24 hours)

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You may contact us through the Internet. Our email and URL addresses are:

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Table of Contents

Introduction

This document lists the changes between hardware revision B and hardware revision C.
The following is a summary of changes:

- PCB requires only 5V over PCI-104; it previously required 3.3V and 5V
- A dedicated local bus oscillator was added to generate 50Mhz. A clock is no longer forwarded from FPGA to the PLX PCI 9056.
- The DDR2 FPGA pinout has been changed to increase timing margins
- The pinout of connector P4 (high-speed serial) has changed. The sideband signals have been relocated and 3.3V has been added.
- The orientation of connector P5 (RS-485 port 0) has rotated 180 degrees
- The Location of P8 (external power connector) has changed. The 3.3V enable signal has also been removed

Reference Design

The top level reference design contains a generic parameter which will correctly configure the FPGA for Revision B or Revision C. A separate constraint file UCF is created for Revision B and Revision C, which need to be added to the ISE project manually.

Local Clock Generation

Revision B

Pin	Signal Name
Y21	lb_lclkfb
A20	lb_lclko_loop
B21	lb_lclko_plx

Local clock generated in FPGA and forwarded to PLX bridge. Clock feedback to FPGA via pin Y21.

Revision C

Pin	Signal Name
Y21	lb_lclkfb
A20	
B21	

Dedicated oscillator generates local bus clock. Clock is driven to FPGA on pin Y21, which drives an internal global clock net.

DDR2 Pinout

Pin	Signal Name	Pin	Signal Name
AA9	ddr2_a<0>	AD21	ddr2_dq<0>
Y8	ddr2_a<1>	AD15	ddr2_dq<1>
AD8	ddr2_a<2>	AC21	ddr2_dq<2>
Y7	ddr2_a<3>	AD14	ddr2_dq<3>
AB9	ddr2_a<4>	AE13	ddr2_dq<4>
W9	ddr2_a<5>	AE22	ddr2_dq<5>
AC8	ddr2_a<6>	AD16	ddr2_dq<6>
AD6	ddr2_a<7>	AE17	ddr2_dq<7>
AA8	ddr2_a<8>	AF10	ddr2_dq<8>
V8	ddr2_a<9>	AE5	ddr2_dq<9>
AC7	ddr2_a<10>	AE12	ddr2_dq<10>
AB7	ddr2_a<11>	AF3	ddr2_dq<11>
AB6	ddr2_a<12>	AF4	ddr2_dq<12>
AC9	ddr2_a<13>	AF12	ddr2_dq<13>
AE7	ddr2_ba<0>	AF5	ddr2_dq<14>
AA5	ddr2_ba<1>	AF9	ddr2_dq<15>
V9	ddr2_ba<2>	AD24	ddr2_dq<16>
AE8	ddr2_cas_n	AE25	ddr2_dq<17>
AE11	ddr2_ck<0>	AC26	ddr2_dq<18>
AD11	ddr2_ck_n<0>	AC23	ddr2_dq<19>
AD18	ddr2_cke<0>	AB22	ddr2_dq<20>
AC22	ddr2_cs_n<0>	AC24	ddr2_dq<21>
AE16	ddr2_dm<0>	AE26	ddr2_dq<22>
AE6	ddr2_dm<1>	AD26	ddr2_dq<23>
AD25	ddr2_dm<2>	AD23	ddr2_dq<24>
AE18	ddr2_dm<3>	AE15	ddr2_dq<25>
AD19	ddr2_dqs<0>	AF24	ddr2_dq<26>
AF7	ddr2_dqs<1>	AF13	ddr2_dq<27>
AF20	ddr2_dqs<2>	AF14	ddr2_dq<28>
AF22	ddr2_dqs<3>	AF25	ddr2_dq<29>
AD20	ddr2_dqs_n<0>	AF15	ddr2_dq<30>
AF8	ddr2_dqs_n<1>	AF23	ddr2_dq<31>
AE20	ddr2_dqs_n<2>	AD13	ddr2_odt<0>
AE21	ddr2_dqs_n<3>	AA7	ddr2_ras_n
		AB5	ddr2_we_n

Pin	Signal Name	Pin	Signal Name
AA9	ddr2_a<0>	AC21	ddr2_dq<0>
Y8	ddr2_a<1>	AD15	ddr2_dq<1>
AD8	ddr2_a<2>	AC23	ddr2_dq<2>
Y7	ddr2_a<3>	AE13	ddr2_dq<3>
AB9	ddr2_a<4>	AD14	ddr2_dq<4>
W9	ddr2_a<5>	AE22	ddr2_dq<5>
AE8	ddr2_a<6>	AD16	ddr2_dq<6>
AD6	ddr2_a<7>	AD21	ddr2_dq<7>
AA8	ddr2_a<8>	AF10	ddr2_dq<8>
V8	ddr2_a<9>	AE5	ddr2_dq<9>
AC7	ddr2_a<10>	AE12	ddr2_dq<10>
AB7	ddr2_a<11>	AF3	ddr2_dq<11>
AB6	ddr2_a<12>	AF4	ddr2_dq<12>
AD10	ddr2_a<13>	AF12	ddr2_dq<13>
AE7	ddr2_ba<0>	AF5	ddr2_dq<14>
AA5	ddr2_ba<1>	AF9	ddr2_dq<15>
V9	ddr2_ba<2>	AC26	ddr2_dq<16>
AC9	ddr2_cas_n	AE26	ddr2_dq<17>
AE11	ddr2_ck<0>	AC24	ddr2_dq<18>
AD11	ddr2_ck_n<0>	AD24	ddr2_dq<19>
AC8	ddr2_cke<0>	AE25	ddr2_dq<20>
W8	ddr2_cs_n<0>	AB22	ddr2_dq<21>
AE16	ddr2_dm<0>	AD26	ddr2_dq<22>
AE6	ddr2_dm<1>	AD25	ddr2_dq<23>
AE17	ddr2_dm<2>	AD23	Ddr2_dq<24>
AE18	ddr2_dm<3>	AE15	Ddr2_dq<25>
AD19	ddr2_dqs<0>	AF25	ddr2_dq<26>
AF7	ddr2_dqs<1>	AF13	ddr2_dq<27>
AF20	ddr2_dqs<2>	AF14	ddr2_dq<28>
AF22	ddr2_dqs<3>	AF24	ddr2_dq<29>
AD20	ddr2_dqs_n<0>	AF15	ddr2_dq<30>
AF8	ddr2_dqs_n<1>	AF23	ddr2_dq<31>
AE20	ddr2_dqs_n<2>	AD9	ddr2_odt<0>
AE21	ddr2_dqs_n<3>	AA7	ddr2_ras_n
		AB5	ddr2_we_n

Hardware Description

Connector Pinouts

High-speed Serial (P4)

The sideband LVCMOS signals (HSS) have been rearranged so that when two FreeForm units are connected:

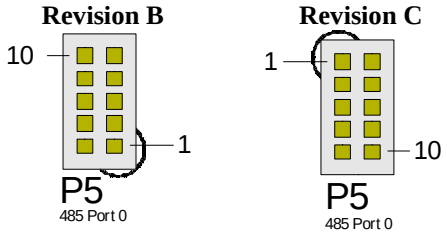
HSS_USER_IO(0) maps to HSS_USER_IO(2)
HSS_USER_IO(1) maps to HSS_USER_IO(3)

Also, 3.3V pins replace the GND pins; this is because the connector has embedded GND blades.

Revision B		Revision C	
Pin	**Signal**	**Pin**	**Signal**
1	MTGRXN0_112	1	MTGRXN0_112
3	MTGRXP0_112	3	MTGRXP0_112
2	MTGTXN0_112	2	MTGTXN0_112
4	MTGTXP0_112	4	MTGTXP0_112
5	GND	5	HSS_USER_IO(0)
7	GND	7	HSS_USER_IO(1)
6	HSS_USER_IO(0)	6	HSS_USER_IO(2)
8	HSS_USER_IO(1)	8	HSS_USER_IO(3)
9	MTGRXN1_112	9	MTGRXN1_112
11	MTGRXP1_112	11	MTGRXP1_112
10	MTGTXN1_112	10	MTGTXN1_112
12	MTGTXP1_112	12	MTGTXP1_112
13	GND	13	3.3V
15	GND	15	3.3V
14	GND	14	3.3V
16	GND	16	3.3V
17	MTGRXN0_114	17	MTGRXN0_114
19	MTGRXP0_114	19	MTGRXP0_114
18	MTGTXN0_114	18	MTGTXN0_114
20	MTGTXP0_114	20	MTGTXP0_114
21	GND	21	3.3V
23	GND	23	3.3V
22	HSS_USER_IO(2)	22	3.3V
24	HSS_USER_IO(3)	24	3.3V
25	MTGRXN1_114	25	MTGRXN1_114
27	MTGRXP1_114	27	MTGRXP1_114
26	MTGTXN1_114	26	MTGTXN1_114
28	MTGTXP1_114	28	MTGTXP1_114

RS-485 Headers (P5)

The orientation of the connector has changed. The pinout remains the same.



External Power Connector (P8)

The connector no longer enables 3.3V regulation – it is always enabled.

Revision B		Revision C	
Pin	**Signal**	**Pin**	**Signal**
1	5V	1	5V
2	3.3 enable (connect to 5V)	2	
3	GND	3	GND
4	VIO (connect to 5V)	4	VIO (connect to 5V)

Specifications

	Revision B	Revision C
Power Requirements	+3.3V DC and +5V DC, in PCI-104 stack +5V DC stand-alone Current requirements are configuration dependant.	+5V DC, in PCI-104 stack +5V DC stand-alone