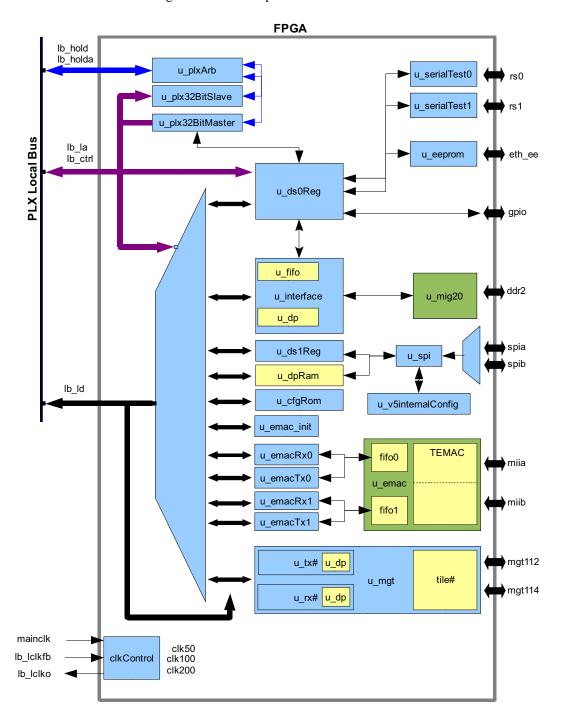
FPGA Block Diagram

The following FPGA block diagram summarizes the organization and connectivity of the VHDL modules in the reference design. Each block is labeled with its instance name, as listed in the module hierarchy. For information on each module/design file refer to the previous sections.



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