CoE 4DM4 Lab #2 Report
Demonstrated Lab 2 on November 10, 2017
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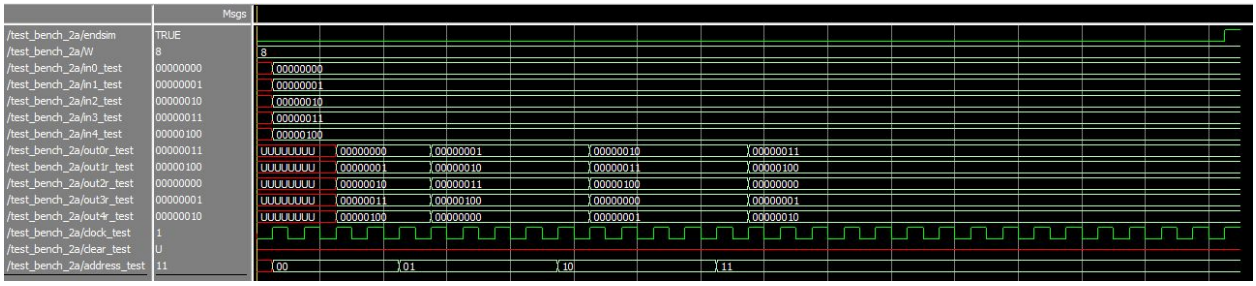
Part A: The Single Router Node

The single router node is an extension of our lab 1, where we included couple more components. Running our testbench of the Single Router Node, we see the correct operation of the Router Node. The correct 'cyclic-shift' occurs.



Some of the screenshots of the resources used in the router as well as our FPGA used to test:

Family	Cyclone V
Device	5CGXFC7C7F23C8

Logic utilization (in ALMs)	41 / 56,480 (< 1 %)
Total registers	80
Total pins	84 / 268 (31 %)

Maximum clock frequency/rate of our design is of the system is:

Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	611.62 MHz	580.05 MHz	clock	limit due to minimum period restriction (tmin)

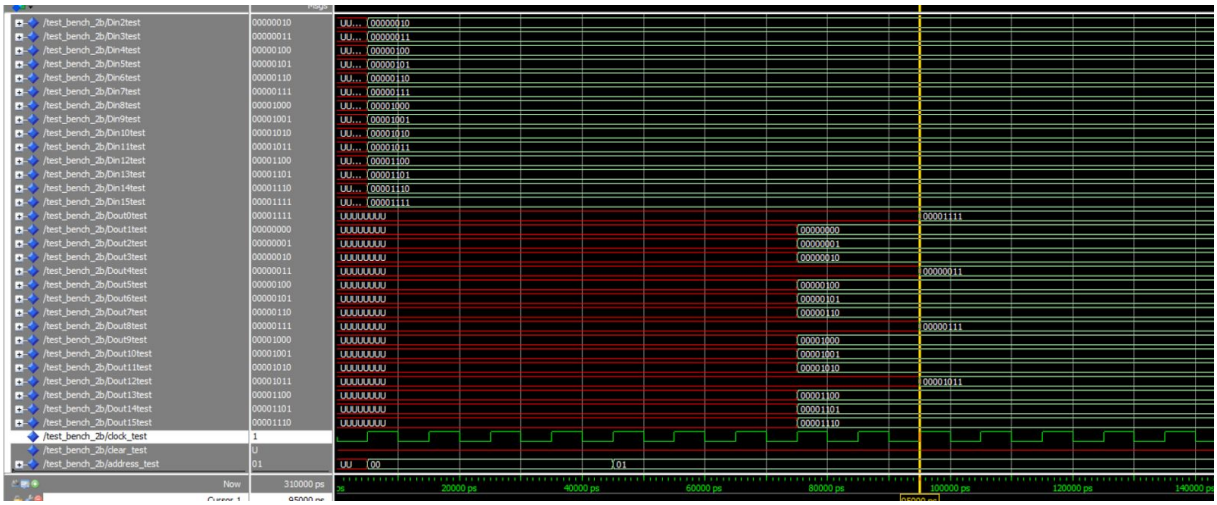
The result makes sense because in our lab 1 design of the crossbar switch, we had very similar numbers (Max clock was 616.52 MHz, and restricted max clock was 580.05 MHz). Lab 1 and or Lab 2a is very similar in the scale of the circuit.

Part B: 16-node Toroid Network-on-Chip with 4 rows and 4 columns.

For part B the first thing needed was to create the 16 nodes from having a single working node from part A and lab1. This was done by using the component routerNode (and afterwards routerNode_at_first_col as well) and by using the port map function which created all 16 nodes from the component base..

After this it was necessary to configure the behaviour of the nodes by using several declared signals assigning them values so that they behave according to the drawings of the lab instructions.

We recognized that these 16 nodes acted in two specific ways. First we had all of the nodes of our first column (node 0,4,8 and 12) and then we had all of the other nodes. To take this into account we created two different entities for both of these cases as well as two different components and LUTs to represent these different behaviours. The component names are “routerNode” for the default case and “routerNode_at_first_col” for the other case while the first LUT was named “LUT.vhd” and the second LUT is was named “LUIT_for_first_col”. These components refer to the entities “routerNode.vhd” and “routerNode_at_first_col.vhd”.



Below are the results we obtain for our design in lab2b. Note due to a larger design, a larger FPGA was required to compile the design.

Resource usage:

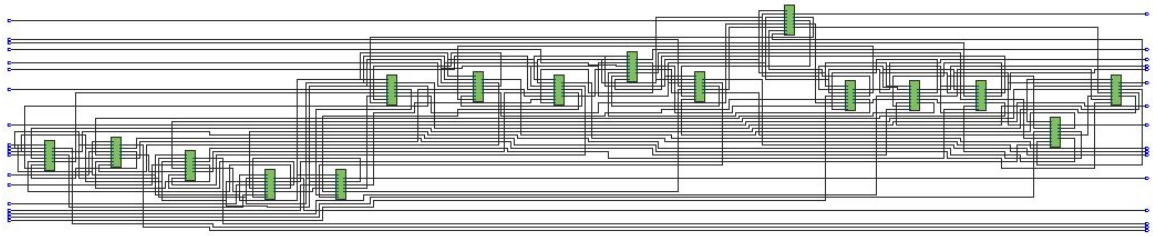
Family	Cyclone V
Device	5CGXFC9E7F35C8

Logic utilization (in ALMs)	217 / 113,560 (< 1 %)
Total registers	576
Total pins	260 / 616 (42 %)

Maximum clock frequency/rate of our design for lab2b is:

	Fmax	Restricted Fmax	Clock Name	Note
1	723.59 MHz	541.13 MHz	clock	limit due to high minimum pulse width violation (tch)

The circuit layout of the design is:



How it is mapped in the actual FPGA:

A changing color gradient represents percent utilization, with minimum utilization at the left and maximum utilization at the right.

Resource	Color Gradient	Resource	Color Gradient	Resource	Color Gradient
Background		I/O Pin		Registers	
Selection		DSP Block		User Assigned Lo...	
Highlight		Logic Element		Fitter Placed Logi...	
Rollover		HPS Interface Bl...		Red/Black Fence ...	
Block Border		HPS Peripheral Bl...		Error overlapping...	
Connection		HPS Block		Security Routing ...	
Path		Wire		Clock Regions	
Bundle		Differential Pin P...		Virtual IO	
LAB		Location Assignm...		Routing Utilization	
Memory